Fuji Power MOSFET

PowerMOSFET

Application Note

June-2014
Fuji Electric Co.,Ltd.

WARNING

1. This Catalog contains the product specifications, characteristics, data, materials, and structures as of June 2014.
2. The contents are subject to change without notice for specification changes or other reasons. When using a product listed in this Catalog be sure to obtain the latest specifications.

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4. The products introduced in this Catalog are intended for use in the following electronic and electrical equipment which has normal reliability requirements.
   - Computers
   - OA equipment
   - Communications equipment (terminal devices)
   - Measurement equipment
   - Machine tools
   - Audiovisual equipment
   - Electrical home appliances
   - Personal equipment
   - Industrial robots etc.

5. If you need to use a product in this Catalog for equipment requiring higher reliability than normal, such as for the equipment listed below, it is imperative to contact Fuji Electric Systems Co., Ltd. to obtain prior approval. When using these products for such equipment, take adequate measures such as a backup system to prevent the equipment from malfunctioning even if a Fuji's product incorporated in the equipment becomes faulty.
   - Transportation equipment (mounted on cars and ships)
   - Trunk communications equipment
   - Traffic-signal control equipment
   - Gas leakage detectors with an auto-shut-off feature
   - Emergency equipment for responding to disasters and anti-burglary devices
   - Safety devices
   - Medical equipment

6. Do not use products in this Catalog for the equipment requiring strict reliability such as the following and equivalents to strategic equipment (without limitation).
   - Space equipment
   - Aeronautic equipment
   - Nuclear control equipment
   - Submarine repeater equipment

7.

8. If you have any question about any portion in this Catalog, ask Fuji Electric Co., Ltd. or its sales agents before using the product. Neither Fuji Electric Co., Ltd. nor its agents shall be liable for any injury caused by any use of the products not in accordance with instructions set forth herein.

Contents

Note:

- The contents of this document are subject to change without prior notice because of product improvement, etc.
- The applications and the parts constants listed in this document is for assisting the design, and does not take the variation of parts and operating conditions into consideration. When integrating our products into your design, take the variation of these parts and operating conditions into consideration.

1. Structure and features of the device

1-1. Structure and features of the device

Just as the name suggests, a Power MOSFET is a semiconductor device in a metal-oxide semiconductor (MOS) structure operating due to the field effect. Of the two types of Power MOSFET (vertical and horizontal types), the vertical type has a feature that current is fed over the entire chip and the resistance per unit chip area (ON resistance, which is the most important characteristics of the MOSFET) can be minimized. Compared with conventional bipolar transistors, the Power MOSFET has the following advantages:

1) Since it is a voltage-controlled device, drive power is low.
2) Since it is a unipolar device, high-speed switching is allowed.
3) Since the temperature coefficient of the current is negative, no secondary breakdown occurs, which facilitates parallel operation.

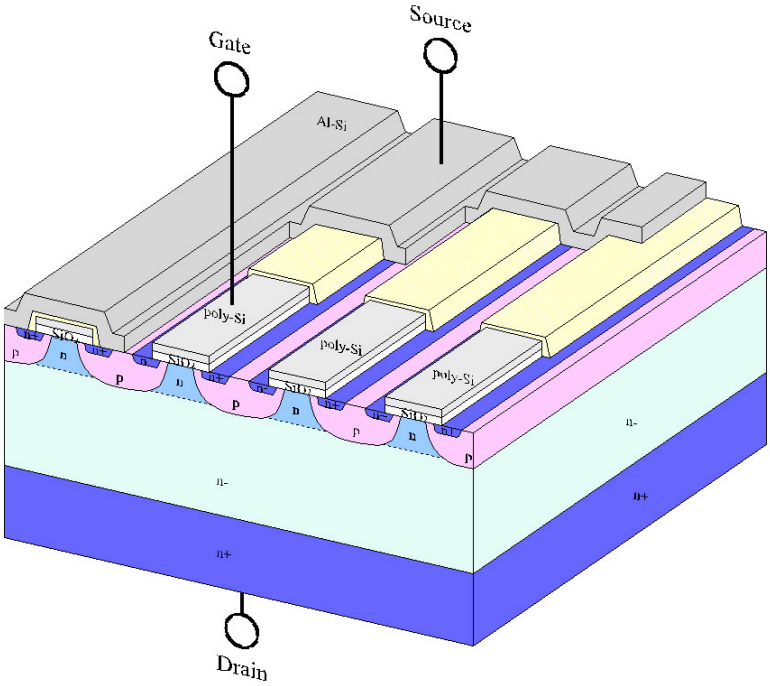


Fig.1-1 Basic structure of the Power MOSFET

Figure 1-2 shows the cross-sectional view of a SuperFAP series chip, whereas Fig. 1-3 shows that of a conventional chip. The SuperFAP series feature the following:

1) Reduced turnoff power dissipation
2) Reduced gate charge
3) Low RonA

The SuperFAP series contributes to the reduction of power dissipation, improvement of efficiency, and downsizing.

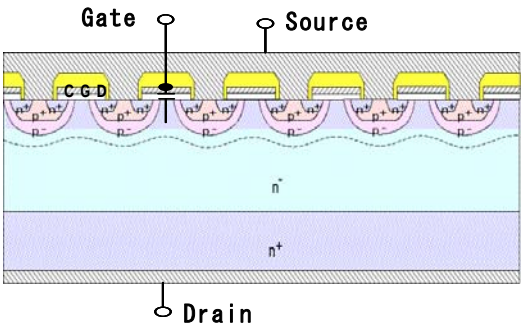


Fig.1-2 Cross-sectional view of a SuperFAP series chip

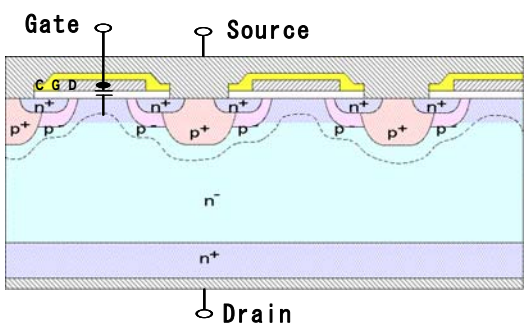


Fig.1-3 Cross-sectional view of a conventional chip

1-2. Power MOSFET of Fuji Electric Co., Ltd.

Since 1982, Fuji Electric Co.,Ltd. has been importing Power MOSFET elements from Siemens AG in the Federal Republic of Germany, assembling them, and providing the assemblies to the market. Fuji has also established an integrated production system ranging from wafer process to assembly through technical partnership with Siemens entered in 1986, and started mass-producing Power MOSFETs. We then focused on improving the properties to achieve ultrahigh-speed switching and high avalanche capacity, and are now providing our products mainly in the field of switching power supplies. Figure 1-4 shows the Power MOSFET series developed by us.

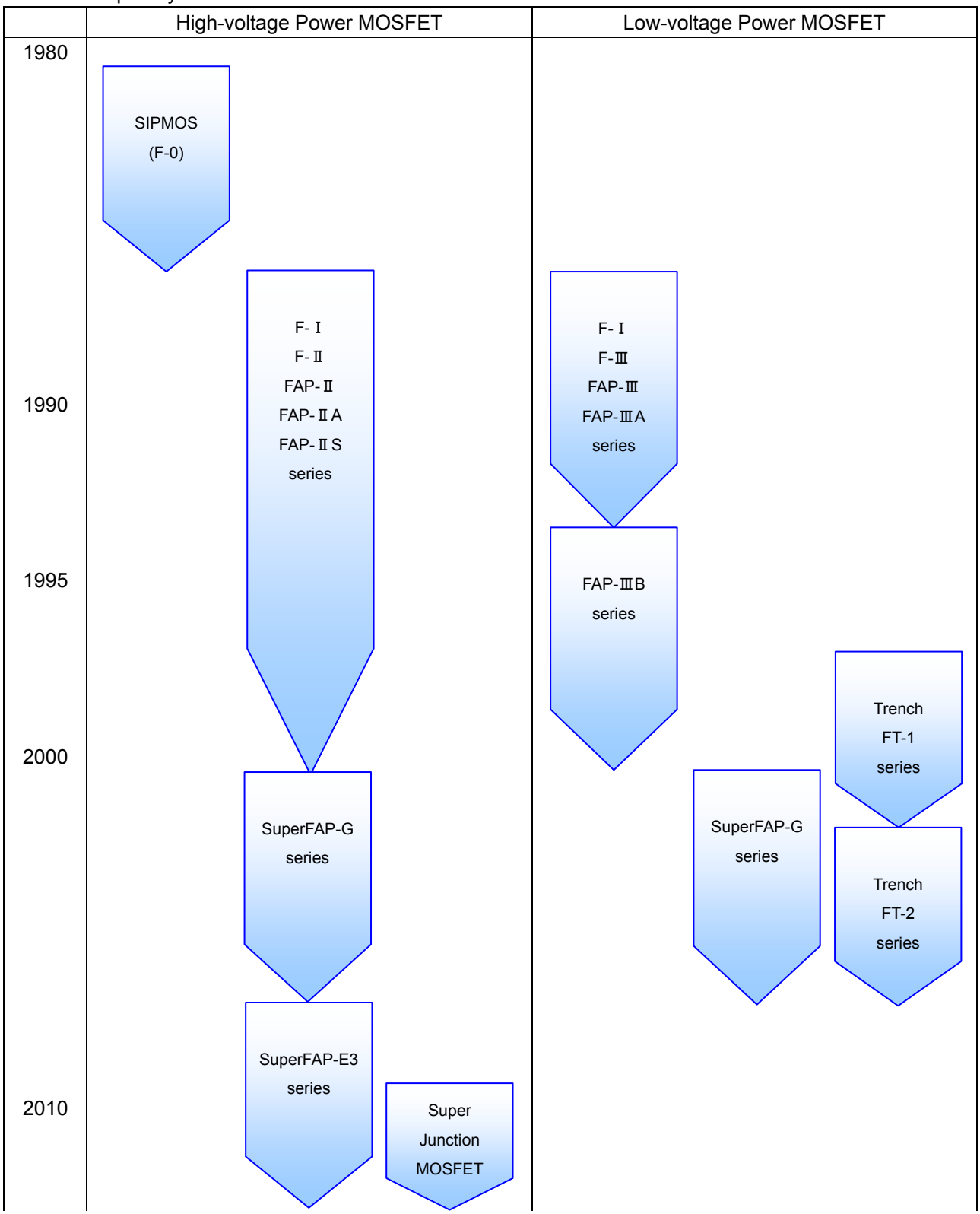
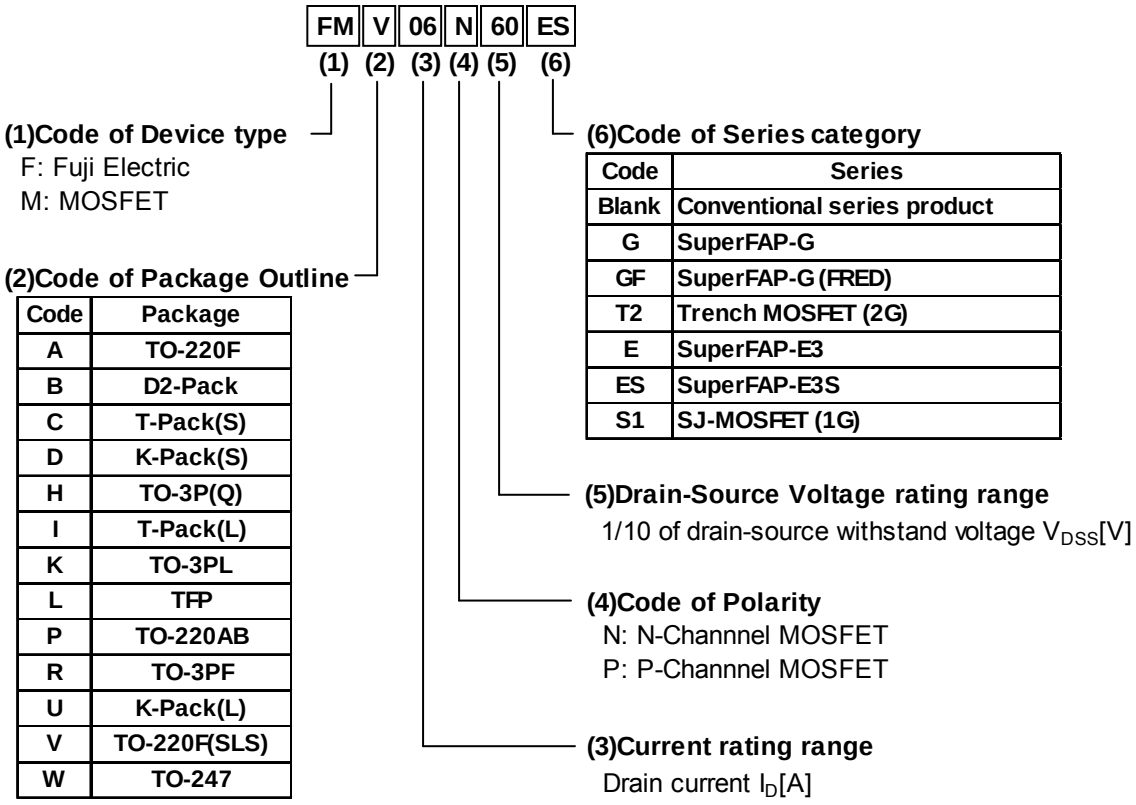


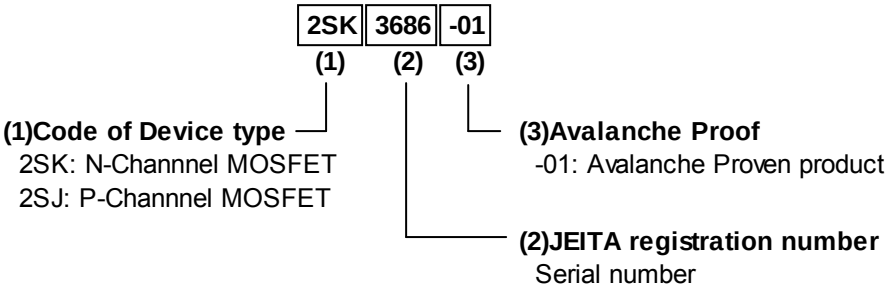
Fig.1-4 Fuji Power MOSFET series

1-3. Code symbols of Fuji Power MOSFET



Code	Package
A	TO-220F
B	D2-Pack
C	T-Pack(S)
D	K-Pack(S)
H	TO-3P(Q)
I	T-Pack(L)
K	TO-3PL
L	TFP
P	TO-220AB
R	TO-3PF
U	K-Pack(L)
V	TO-220F(SLS)
W	TO-247

Code	Series
Blank	Conventional series product
G	SuperFAP-G
GF	SuperFAP-G (FRED)
T2	Trench MOSFET (2G)
E	SuperFAP-E3
ES	SuperFAP-E3S
S1	SJ-MOSFET (1G)



2. Terms and characteristics

2-1. Description of terms (Absolute maximum rating, electrical characteristics)

2-1-1. Absolute maximum rating

(Reference example) Excerpt from the specification of the FMV06N60ES

5.Absolute Maximum Ratings at Tc=25°C (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	600	V	
	V_{DSX}	600	V	V_{GS}=-30V
Continuous Drain Current	I_D	± 6	A	
Pulsed Drain Current	I_{DP}	± 24	A	
Gate-Source Voltage	V_{GS}	± 30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	I_{AR}	6	A	Note *1
Non-Repetitive Maximum Avalanche Energy	E_{AS}	313.7	mJ	Note *2
Repetitive Maximum Avalanche Energy	E_{AR}	3.7	mJ	Note *3
Peak Diode Recovery dV/dt	dV/dt	3.8	kV/μs	Note *4
Peak Diode Recovery -di/dt	-di/dt	100	A/μs	Note *5
Maximum Power Dissipation	P_D	2.16	W	Ta=25°C
		37		Tc=25°C
Operating and Storage	T_{ch}	150	°C	
Temperature range	T_{stg}	-55 to +150	°C	
Isolation Voltage	V_{ISO}	2	kVrms	t=60sec,f=60Hz

Note *1 : Tch≤150°C, See Fig.1 and Fig.2
Note *2 : Stating Tch=25°C, I_{AS}=2.4A, L=99.8mH, Vcc=60V, R_G=50Ω, See Fig.1 and Fig.2
E_{AS} limited by maximum channel temperature and avalanche current.
See to 'Avalanche Energy' graph of page 9/15.
Note *3 : Repetitive rating : Pulse width limited by maximum channel temperature.
See to the 'Transient Themal impeadance' graph of page 9/15.
Note *4 : I_F≤-I_D, -di/dt=100A/μs, Vcc≤BV_{DSS}, Tch≤150°C.
Note *5 : I_F≤-I_D, dv/dt=3.8kV/μs, Vcc≤BV_{DSS}, Tch≤150°C.

Term	Symbol	Definition and description
Drain-Source Voltage	V_{DSS}	Maximum voltage value permitted between the drain and the source in a state where the gate and the source are short-circuited.
Continuous Drain current	I_D	Maximum DC current value permitted to the drain terminal determined based on the maximum power dissipation and the maximum ON resistance (Tch=150deg.) . (including forward current rating of parasitic diodes)
Pulsed Drain Current	$I_{D\ pulse}$	Maximum peak value of the drain current permitted at the time of pulse operation at pulse width and duty ratio specified in the “area of safe operation” of the characteristic curve. Specified as 4 times the continuous drain current.
Gate-Source Voltage	V_{GS}	Maximum voltage value permitted between the gate and the source. Maximum permitted voltage value of the gate oxide film.
Repetitive and Non-Repetitive Maximum Avalanche Current	I_{AR}	Maximum permitted current at the occurrence of an avalanche. Forward current value of the avalanche parasitic diode.
Maximum Avalanche Energy **Non-Repetitive** **Repetitive**	 E_{AS} E_{AR}	Maximum permissible power at the occurrence of an avalanche.
Peak Diode Recovery dV/dt	dv/dt	Rate of change of the maximum permissible D-S voltage during reverse recovery operation of the parasitic diode
Peak Diode Recovery –di/dt	-di/dt	Rate of change of the maximum permissible D-S current during reverse recovery operation of the parasitic diode
Maximum Power Dissipation **Independent use state (Ta=25deg.)** **Infinite heat dissipated state (Tc=25deg.)**	P_D	Maximum power dissipation value permitted to the MOSFET.
Channel temperature	T_{ch}	Chip temperature range in which MOSFET operation is permitted
Storage temperature	T_{stg}	Temperature range allowing storage or transportation of the MOSFET without being subjected to electric load
Isolation Voltage	V_{ISO}	Applicable to full-mold packages only

* Derating is required for some absolute maximum rating items depending on conditions such as case temperature.

2-1-2. Electrical characteristics (Static Ratings)

(Reference example) Excerpt from the specification of the FMV06N60ES

6.Electrical Characteristics at Tc=25°C (unless otherwise specified)

Static Ratings

Description	Symbol	Conditions		min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250 μA V_{GS}=0V		600	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	I_D=250 μA V_{DS}=V_{GS}		3.2	3.7	4.2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=600V V_{GS}=0V	T_{ch}=25℃	-	-	25	μA
		V_{DS}=480V V_{GS}=0V	T_{ch}=125℃	-	-	250	
Gate-Source Leakage Current	I_{GSS}	V_{GS}= ±30V V_{DS}=0V		-	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	I_D=3A V_{GS}=10V		-	1.03	1.20	Ω

Term	Symbol	Definition and description
Drain-Source Breakdown Voltage	BV_{DSS}	Breakdown voltage between the drain and the source (= Reverse voltage of the parasitic diode). Voltage value between the drain and the source measured with specified drain current fed, in a state where the gate and the source are short-circuited.
Gate Threshold Voltage	$V_{GS(th)}$	Gate voltage value allowing the drain current to start flowing. Gate source voltage value measured by feeding specified drain current and applying specified drain source voltage.
Zero Gate Voltage Drain Current	I_{DSS}	Current between the drain and the source when the gate voltage is 0V (= Drain leakage current). Drain current value measured by applying specified drain-source voltage in a state where the gate and the source are short-circuited.
Gate-Source Leakage Current	I_{GSS}	Gate leakage current value measured by applying specified gate-source voltage in a state where the drain and the source are short-circuited.
Drain-Source On-State Resistance	$R_{DS(on)}$	Resistance between the drain and the source measured by applying specified gate-source voltage and feeding specified drain current.

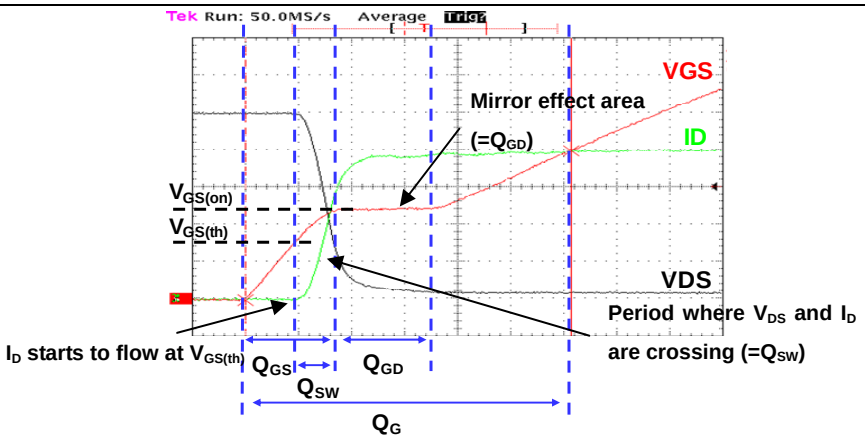
* Unless otherwise specified, the above characteristics are exhibited when at Tc=25deg.

2-1-3. Electrical characteristics (Dynamic Ratings)

(Reference example) Excerpt from the specification of the FMV06N60ES

Dynamic Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	g_{fs}	I_D=3.0A V_{DS}=25V	2.5	5	-	S
Input Capacitance	Ciss	V_{DS}=25V	-	950	1425	pF
Output Capacitance	Coss	V_{GS}=0V	-	100	150	
Reverse Transfer Capacitance	Crss	f=1MHz	-	7.5	11	
Turn-On Time	td(on)	V_{cc}=300V I_D=3.0A	-	29	43.5	ns
	tr	V_{GS}=10V R_{GS}=27Ω	-	15	22.5	
Turn-Off Time	td(off)	See Fig.3 and Fig.4	-	75	113	
	tf		-	16	24	
Total Gate Charge	Q_G	V_{cc}=300V I_D=6A	-	31	46.5	nC
Gate-Source Charge	Q_{GS}	V_{GS}=10V	-	10.5	15.8	
Gate-Drain Charge	Q_{GD}	See Fig.5	-	8	12	
Gate-Drain Crossover Charge	Q_{SW}		-	4.5	6.75	

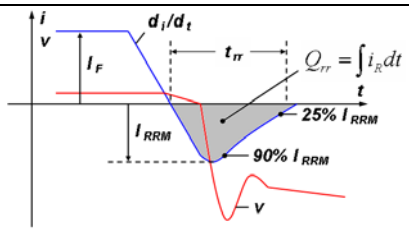
Term	Symbol	Definition and description
Forward Transconductance	g_{fs}	Rate of change of the drain current against the specified change in gate-source voltage measured by applying specified drain-source voltage and feeding specified drain current. Represents the degree of ease of feeding current. Equivalent to hFE of bipolar transistors.
Input Capacitance	Ciss	Characteristic value of the parasitic capacitance measured between gate and source terminals at specified gate-source and drain-source voltage and measuring frequency, in a state where the drain and the source are alternately short-circuited.
Output Capacitance	Coss	Characteristic value of the parasitic capacitance measured between drain and source terminals at specified gate-source and drain-source voltage and measuring frequency, in a state where the gate and the source are alternately short-circuited.
Reverse Transfer Capacitance	Crss	Characteristic value of the parasitic capacitance measured between the drain and the gate at specified gate-source voltage and measuring frequency in a state where source terminal is grounded.
Turn-On Delay Time	td(on)	Delay time of drain voltage with respect to the gate voltage measured between 10% value of gate-source voltage and 90% value of drain-source voltage.
Turn-On Time	tr	Time required for drain voltage measured between 90% value and 10% value of the drain-source voltage to decrease.
Turn-Off Delay Time	td(off)	Delay time of drain voltage with respect to the gate voltage measured between 90% value of gate-source voltage and 10% value of drain-source voltage.
Turn-Off Time	tf	Time required for the drain voltage measured between 10% value and 90% value of drain-source voltage to increase.
Total Gate Charge	Q_G	Gate charge required to turn on the MOSFET
Gate-Source Charge	Q_{GS}	
Gate-Drain Charge	Q_{GD}	
Gate-Drain Crossover Charge	Q_{SW}	

2-1-4. Electrical characteristics (Parasitic diode)

(Reference example) Excerpt from the specification of the FMV06N60ES

Reverse Diode

Description	Symbol	Conditions	min.	typ.	max.	Unit
Avalanche Capability	I_{AV}	L=6.39mH Tch=25℃ See Fig.1 and Fig.2	6	-	-	A
Diode Forward On-Voltage	V_{SD}	I_F=6A V_{GS}=0V T_{ch}=25℃	-	0.90	1.35	V
Reverse Recovery Time	trr	I_F=6A V_{GS}=0V -di/dt=100A/μs, Tch=25℃	-	0.4	-	μs
Reverse Recovery Charge	Qrr	See Fig.6	-	3.3	-	μC

Term	Symbol	Definition and description
Avalanche Capability	I_{AV}	Drain current value resistant to the switching of unclamped inductance. Since the current is fed at the parasitic pn contact (parasitic diode structure), the avalanche capacity is displayed as parasitic diode characteristics. Same as avalanche current at absolute maximum rating.
Diode Forward On-Voltage	V_{SD}	Forward voltage between the source and the drain measured by feeding forward current I_F to the parasitic diode at gate voltage VGS=0V and chip temperature Tch=25deg. When forward bias voltage is applied to the gate terminal, current is fed to the parasitic diode and the MOSFET. Consequently, this value decreases (Synchronous rectification).
Reverse Recovery Time	trr	Time required for reverse recovery current of parasitic diode to vanish under specified measurement conditions. The same switching characteristics as diodes for input bridge. Slow compared with fast recovery diodes. FRED type is high-speed parasitic diode. 
Reverse Recovery Charge	Qrr	

2-1-5. Electrical characteristics (Thermal resistance)

(Reference example) Excerpt from the specification of the FMV06N60ES

7.Thermal Resistance

Description	Symbol	min.	typ.	max.	Unit
Channel to Case	Rth(ch-c)			3.38	℃/W
Channel to Ambient	Rth(ch-a)			58.0	℃/W

Term	Symbol	Definition and description
Thermal Resistance (Channel to Case)	$R_{th(ch-c)}$	Thermal resistance from the channel to the surface of the case of the device (heat sink mounting surface). The characteristics depend on package and chip sizes. The larger the chip size, the smaller the thermal resistance. Use this value to calculate thermal resistance at the time of mounting the heat sink.
Thermal Resistance (Channel to Ambient)	$R_{th(ch-a)}$	Thermal resistance from the channel to the ambient. Thermal resistance from the chip to the ambient not affected by temperature increase measured in an independent state where heat sink, etc. are not mounted. The characteristics become a unique value depending on packages. Thermal resistance in a state mounted to specified substrate may be adopted for SDM packages, etc.

3. Circuit design and device characteristics

3-1. Drain-Source Breakdown Voltage : BV_{DSS}

The drain-source breakdown voltage BV_{DSS} for guaranteeing rated voltage is specified in min. value. To ensure safety in circuit operation with respect to this guaranteed value, a margin is allowed for actual value. However, since the drain-source breakdown voltage and ON resistance is in a trade-off relation, by decreasing the margin as far as possible, the ON resistance is decreased.

The dependence of the drain-source breakdown voltage on temperature exhibits positive temperature dependence, and generally increases at the rate of 10%/100deg.

3-2. Gate Threshold Voltage : $V_{GS(th)}$

The gate threshold voltage is the gate-source voltage V_{GS} allowing the MOSFET to start feeding current.

Figure 3-1 is a temperature characteristics chart of the gate-source threshold voltage $V_{GS(th)}$. The gate-source threshold voltage has different negative temperature coefficient (-5mV to -7mV/deg.) depending on products, and decreases under the high-temperature condition, namely the actual operating conditions. Consequently, when designing a drive circuit, it is necessary to check the temperature characteristics chart of the gate-source threshold value listed in the data sheet to prevent malfunction from occurring due to external noise, etc.

Figure 3-2 is a chart demonstrating the transmission characteristics of the gate voltage V_{GS} and the drain current I_D. In the MOSFET, the current fed by the gate voltage is limited. Consequently, when designing a drive circuit, it is necessary to check the transmission characteristics chart of the gate voltage and drain voltage listed in the data sheet to set a gate voltage that can feed sufficient drain current. If the gate voltage is set low to minimize drive power dissipation, required drain current cannot be fed, and consequently required output cannot be obtained. In addition, increase in ON dissipation may result in a breakdown.

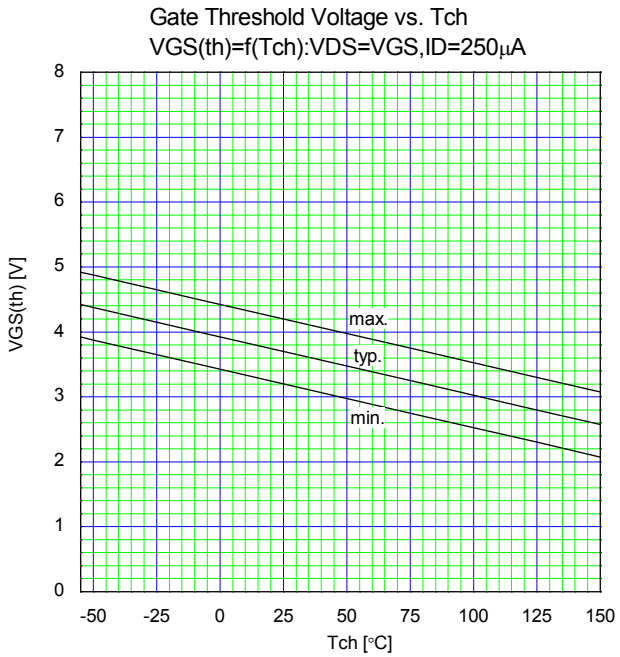


Fig.3-1 $V_{GS(th)}$ temperature characteristics chart

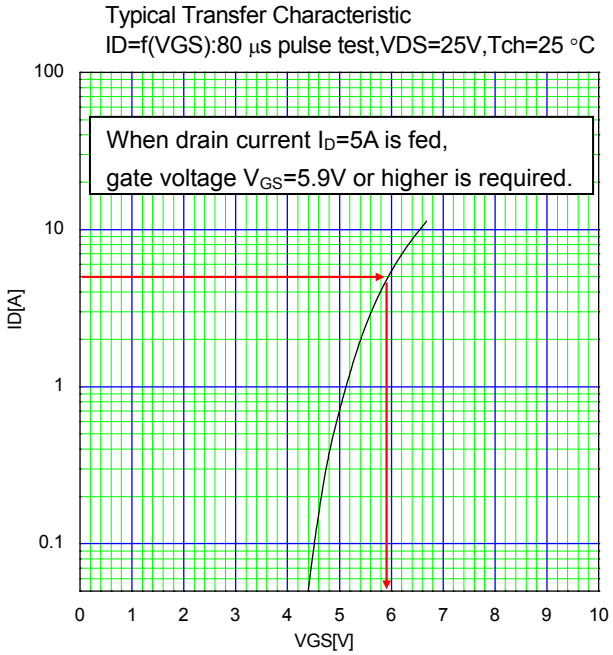


Fig.3-2 V_{GS}-I_D transmission characteristics chart

3-3. Zero Gate Voltage Drain Current (Drain Leakage Current) : I_{DSS}

The zero gate voltage drain current is a leakage current between the drain and the source. The drain leakage current has positive temperature characteristics. The dissipation from I_{DSS} is expressed by $P(I_{DSS})=V_{DS} \times I_{DSS}$ when the MOSFET remains OFF. However, within normal operating range, the value is negligibly small compared with the ON dissipation (dissipation generated by $R_{DS(on)}$).

3-4. Maximum Power Dissipation : P_D

Figure 3-3 is a chart showing the reduction curve of the maximum power dissipation P_D at the case temperature Tc under the condition of absolute maximum rating of the channel temperature Tch=150deg.

In designing, it is essential not to allow the power dissipation P_D to be exceeded at the assumed maximum case temperature Tc.

Note that the power dissipation P_D listed in the brochure and the data sheet is the value calculated from the heat resistance between the channel and the case $R_{th(ch-c)}$ in a state where the device is mounted to an infinite radiator plate.

The power dissipation in actual operation is calculated from the thermal resistance and ambient temperature, with the thermal resistance of the heat sink to be mounted and contact thermal resistance taken into consideration.

Power dissipation on the data sheet:

Infinite heat dissipated state

$$P_D = \frac{Tch(\max) - Tc}{Rth(ch-c)} \ [W]$$

Power dissipation in actual operation:

(Example) State in which a heat sink is mounted

$$P_D = \frac{Tch(\max) - Ta}{Rth(ch-c) + Rth(c-f) + Rth(f-a)} \ [W]$$

$R_{th(c-f)}$: Contact thermal resistance with the heat sink

$R_{th(f-a)}$: Thermal resistance of the heat sink

Ta : Ambient temperature

Tc : Case temperature

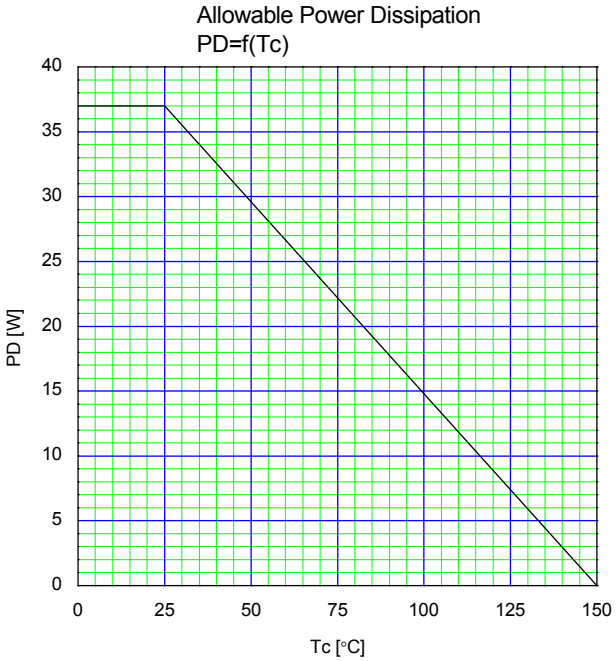


Fig.3-3 Power dissipation P_D temperature characteristics chart

3-5. Thermal Resistance (Channel to Case) : $R_{th(ch-c)}$

The thermal resistance value listed in the brochure or the data sheet is the thermal resistance in steady state. When preparing thermal design of devices that perform pulse operation such as switching power supply, or calculating the temperature increase due to pulse surge, it is necessary to find the thermal resistance at any given time from the transient thermal impedance characteristics chart (Fig.3-4) listed in the data sheet, or to use a calculated value.

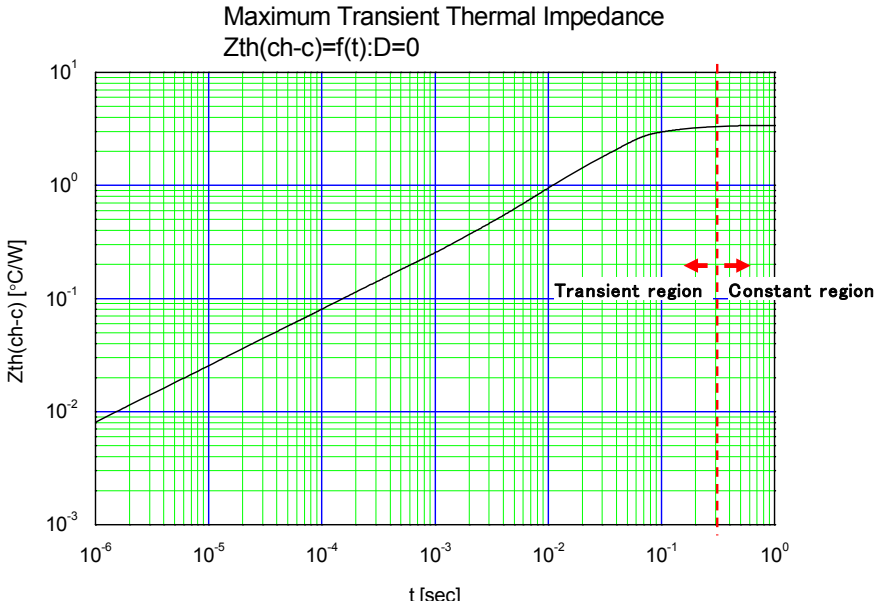


Fig.3-4 Transient resistance characteristics chart

3-6. Area of safe operation (ASO)

Figure 3-5 shows the area of safe operation of the FMV06N60ES.

The area of safe operation, which is used to judge the feasibility of use of a Power MOSFET in an application circuit, is divided into the following 4 areas, each of which is restricted by different conditions.

Area [1]: Area restricted by drain current I_D, and pulse drain current I_{DP}

Area [2]: Area (1) restricted by the maximum power dissipation P_D

Area [3]: Area (2) restricted by the maximum power dissipation P_D (at t=1ms to DC only)

Normally, the ASO breakdown tolerance is determined by power dissipation and thermal resistance, and when t=1ms or longer, the breakdown tolerance decreases in high-voltage region due to local current crowding phenomenon. Consequently, a phenomenon similar to secondary breakdown in bipolar transistors occurs.

Area [4]: Area restricted by drain-source voltage V_{DSS} (withstand voltage)

The ASO chart listed in the data sheet applies to an ideal condition in which the case temperature Tc=25deg. and Duty=0 (Single pulse), and does not exhibit the operation condition of actual switching power supply circuits, etc. Consequently, the chart cannot be used for the review of feasibility of use without making modifications. The chart must be derated according to the actual operating conditions (case temperature Tc, operating frequency f, ON width t, etc.)

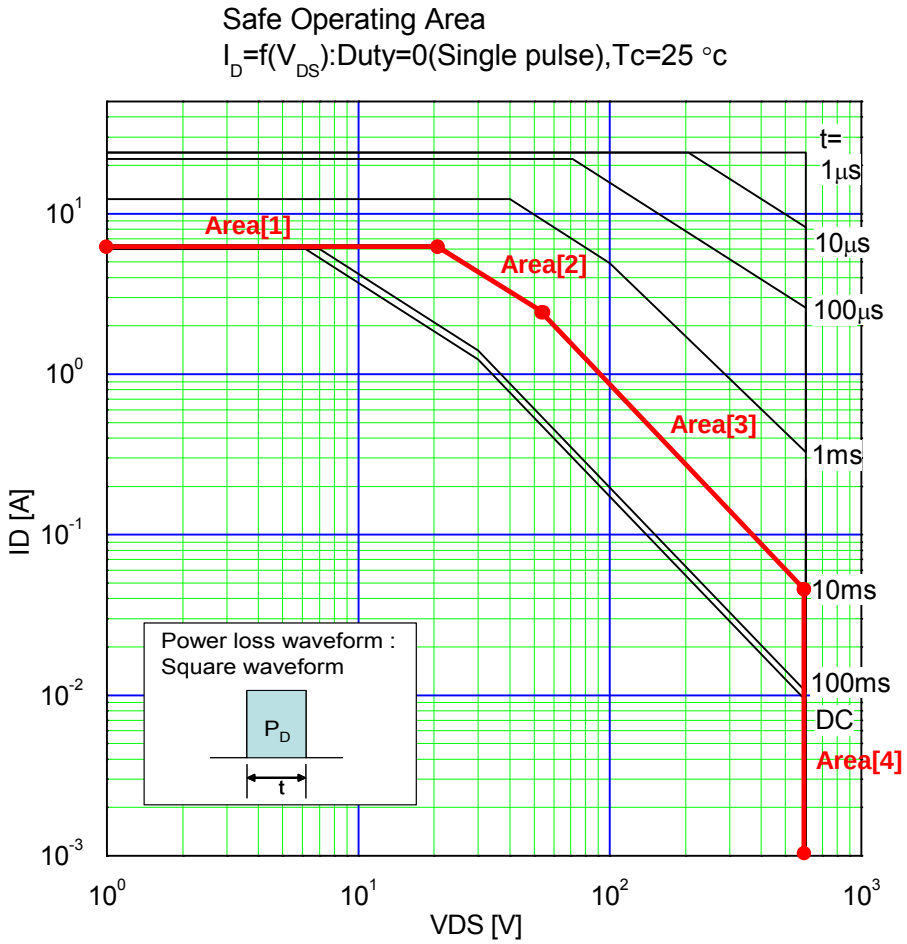


Fig.3-5 ASO chart of the FMV06N60ES (Condition: Duty=0, Tc=25deg.)

3-7. Drain-Source On-state Resistance : $R_{DS(on)}$

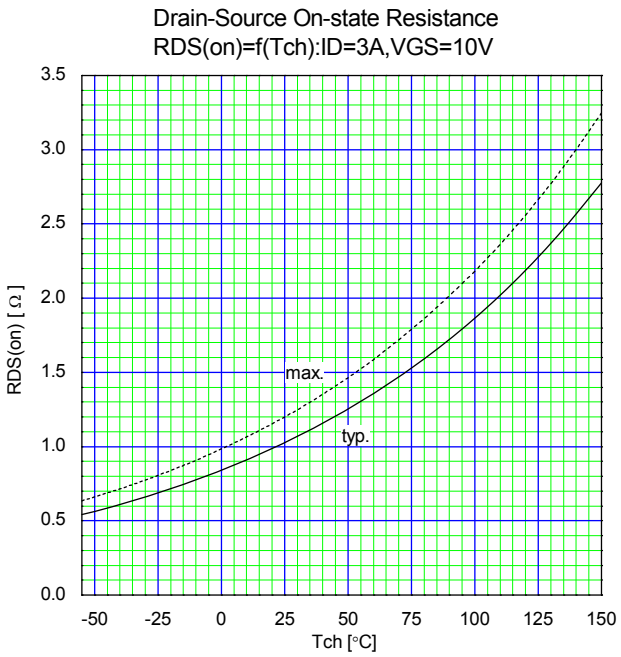


Fig.3-6 ON resistance - channel temperature

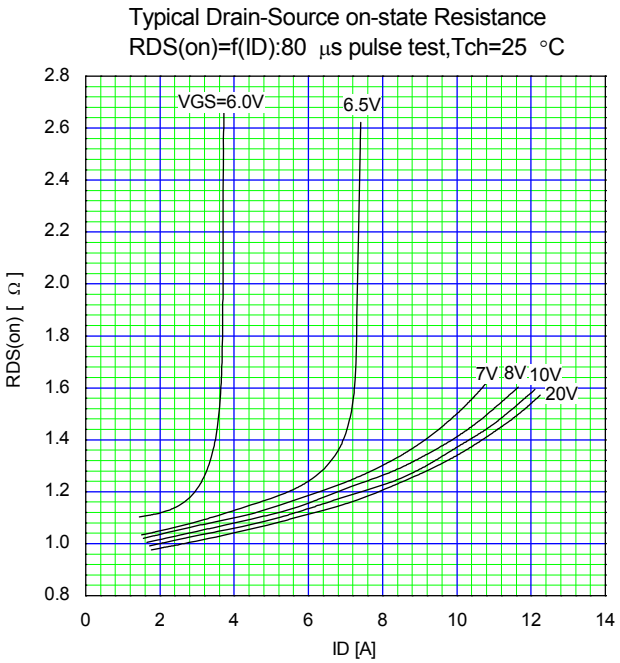


Fig.3-7 ON resistance - drain current (standard value)

Figure 3-6 is a temperature characteristics chart of ON resistance $R_{DS(on)}$ of the FMV06N60ES.
The ON resistance is the most important characteristics for determining the ON dissipation, and is determined by the typ. value and the max. value at the case temperature Tc=25deg. in the characteristics table. The ON resistance has positive temperature characteristics, and in the power dissipation calculation/design in actual operation, the max. value of $R_{DS(on)}$ at the channel temperature Tch=150deg. is read from Fig.3-6 and used as the worst condition. The MOSFET has self-stabilizing function when connected in parallel. When two of more devices are connected in parallel, even if current is fed concentrated on a device having low resistance value due to variation of ON resistance, the device temperature increases due to heat loss, and the resistance value of the device heated due to positive temperature characteristics of the variation of the ON resistance increases, thus decreasing current. Consequently the balance of the current fed through each device is maintained without causing thermal runaway to occur.
Figure 3-7 is a ON resistance $R_{DS(on)}$ - drain current I_D characteristics chart. The ON resistance depends on drain current and gate-source voltage, and the higher the gate-source voltage, the smaller the ON resistance. We therefore recommend the use under the condition where the gate-source voltage is 10V or higher.

3-8. Capacitance characteristics Ciss, Crss, Coss

Figure 3-9 illustrates a simplified equivalent circuit of an N-channel MOSFET. The gate-drain capacitance, namely mirror capacitance, greatly affects the switching characteristics. If the drain-source voltage becomes equal to or smaller than the gate-source voltage, the mirror capacitance surges to approximately 10 times the value of the time when it is larger than the gate-source voltage, as shown in Fig.3-10.

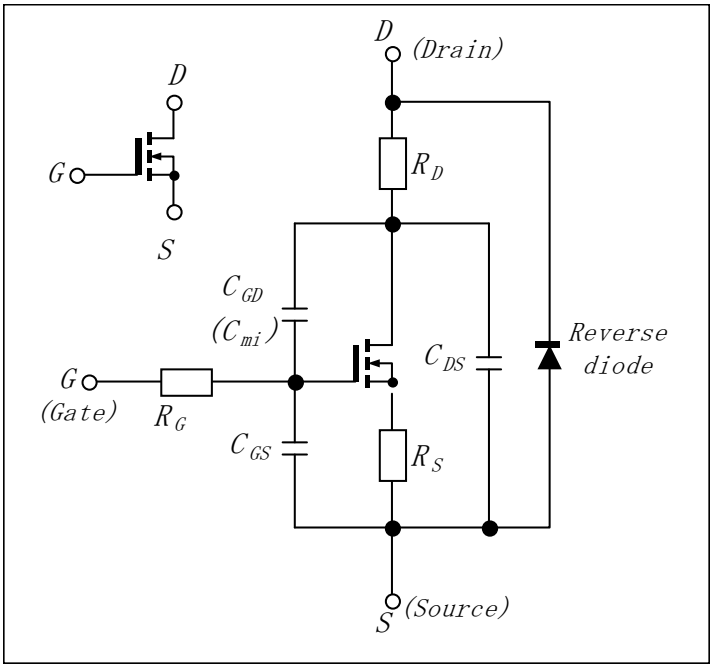


Fig.3-9 Symbols and equivalent circuit of an N-channel MOSFET

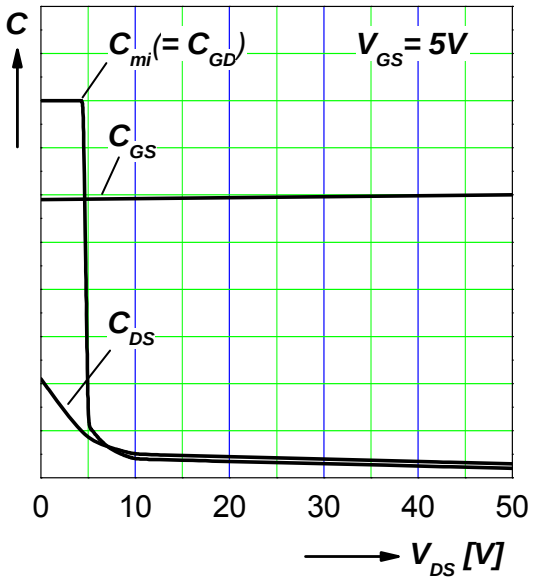


Fig.3-10 Capacitance and drain-source voltage

Figure 3-11 is a chart showing the capacitance characteristics of the FMV06N60ES. Each capacitance of the Power MOSFET has the relations shown below:

Input capacitance: $Ciss \approx Cmi + C_{GS}$
Reverse transfer capacitance: $Crss \approx Cmi$
Output capacitance: $Coss \approx Cmi + C_{DS}$

The reverse transfer capacitance of the SuperFAP series is designed to remain small to ensure significantly improved switching characteristics.

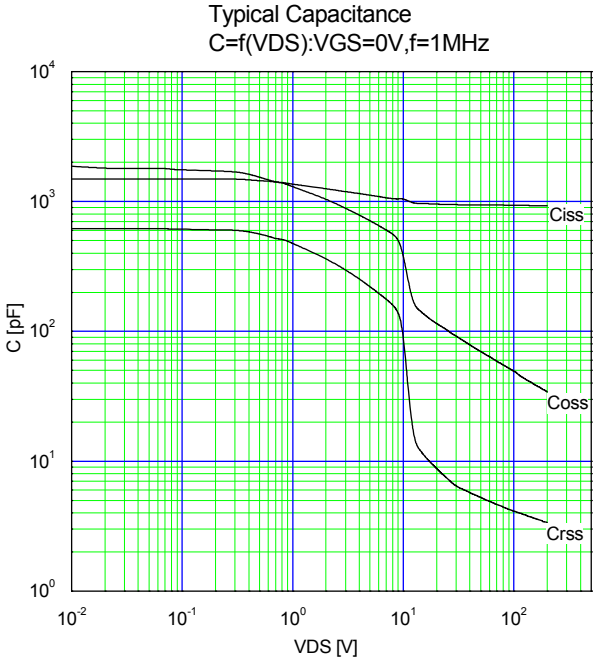


Fig.3-11 Capacitance and drain-source voltage (standard value)

3-9. Total Gate Charge : Qg

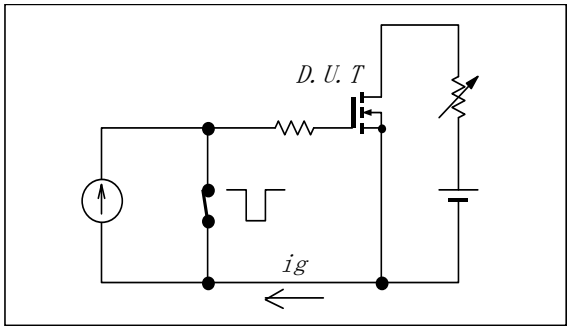


Fig.3-12 Gate charge measurement circuit

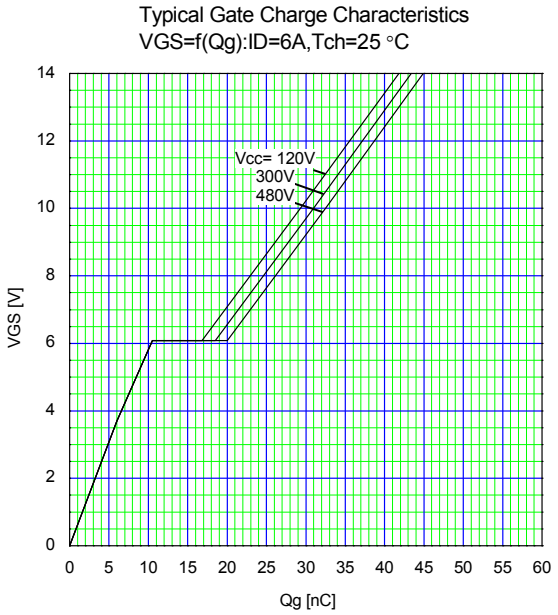


Fig.3-13 Input gate charge (standard)

Figure 3-12 illustrates a gate charge Qg measurement circuit, and Fig. 3-13 illustrates the input gate charge characteristics of the FMV06N60ES. In this measurement, the gate is charged with constant current (ig), and the temporal change of the drain-source voltage (V_{DS}) and gate-source voltage (V_{GS}) is observed.
By charging the gate with constant current (ig), the time axis can be read as the quantity of electric charge Qg only by multiplying time by ig.

3-10. Switching characteristics

Since the MOSFET is a voltage-controlled device, drive current is not required when ON or OFF state is maintained. Meanwhile, each time switching operation is performed, charging/discharging current of the input capacitance is fed.

(1) Resistance load switching characteristics

Figure 3-14 illustrates the switching operation waveforms against resistance load.

(1-1) Turn ON process

Period t0-t1:

The MOSFET is driven at time t0. The gate-source voltage increases with the progress of charging of input capacitance Ciss from the internal resistance Ri of the drive circuit. The gate path resistance Rg is compared with Ri and ignored.

Period t1-t2:

When threshold voltage value is reached at time t2, the MOSFET starts conducting. The drain-source voltage decreases with the increase of the load resistance voltage drop. The drain current increases in the period t1-t2. The mirror capacitance, which is still small at this time, is discharged due to the change in drain-source voltage. The gate-source voltage increases along the transmission characteristics curve.

Period t2-t3:

At time t2, the drain-source voltage V_{DS} becomes equal to the gate-source voltage V_{GS}. The effect of mirror capacitance that has grown very large appears here. In period t2-t3, the MOSFET operates as a mirror integration circuit. Namely, the gate-source voltage remains the same, whereas the gate charging current is fed via the mirror capacitance to further decrease the drain-source voltage.

Period t3-t4:

At time t3, the drain-source voltage reaches the final point of the analog area (mirror effect region) of the output characteristics curve. In period t3-t4, the input capacitance Ciss is charged up to the level of the drive voltage. The channel resistance further decreases. At timed t4, the ON resistance $R_{DS(on)}$ (value obtained by dividing the drain-source voltage by the drain current) of the MOSFET reaches the lowest value.

(1-2) Turn OFF process

Period t5-t6:

The turn off process is started by switching the drive voltage to 0 at time t5. The charge accumulated in the input capacitance Ciss, which is at the maximum value at this time, is discharged via the internal resistance Ri of the drive circuit, and the gate-source voltage decreases to the value that allows the drain current to pass through the resistance area of the output characteristics curve.

Period t6-t7:

When time t6 is reached, the ON resistance increases slightly.

The MOSFET operates again as a mirror integrator during the period t6-t7. Namely, the gate drive current is fed via the mirror capacitance, which is still large, with the gate-source voltage maintained at a constant level, and the drain-source voltage increases.

Period t7-t8:

At time t7, the gate-source voltage becomes equal to the drain-source voltage. The mirror capacitance decreases to a small value. The mirror capacitance, which has decreased, is charged, and the drain-source voltage surges during period t7-t8. The drain current decreases in response to the voltage drop of the load resistance, and the gate-source voltage also decreases.

Period t8-t9:

The threshold voltage is reached at time t8, and the MOSFET is interrupted completely. Finally, during the period t8-t9, the input capacitance is discharged down to the level of the drive voltage.

Since the MOSFET does not have accumulation time, its switching time is determined only by the charging and discharging of the input capacitance. Since the internal resistance Ri of the drive circuit can be selected freely, the switching time of the MOSFET can be adjusted within a wide range.

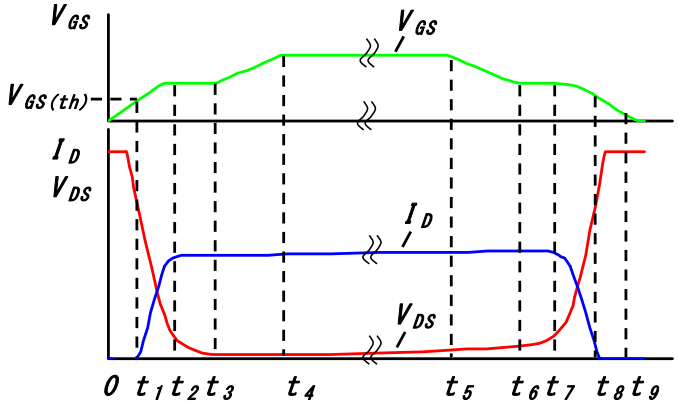


Fig.3-14 Switching characteristics against resistance load

(2) Switching characteristics of the induction load with a flywheel diode

Assume that in the initial state, the MOSFET is interrupted and current is fed to the induction load and the flywheel diode. (See Fig. 3-15.)

(2-1) Turn ON process

Period t0-t1:

At time t0, the MOSFET is driven via rectangular wave voltage. (See Fig. 3-16.) The gate-source voltage increases with the progress of the charging process of the input capacitance Ciss by the internal resistance Ri of the drive circuit.

Period t1-t2:

At time t1, the threshold voltage is reached. During period t1-t2, the drain current increases in proportion to the gate-source voltage, whereas the drain-source voltage is maintained at the operation voltage level due to characteristics of the diode.

Period t2-t3:

At time t2, the transistor carries the entire load current. Since the reverse recovery current of the diode is added to the load current in the subsequent period t2-t3, the drain current further increases.

Period t3-t4:

At time t3, namely at the polarity reversing point of the reverse recovery current of the diode, the drain current reaches the maximum value. Up to that time, the drain-source voltage remains at the same level as the operating voltage. The gate-source voltage reaches a value capable of conducting the peak current generated in the transistor.

In the period t3-t4, the drain-source voltage decreases, and the reverse voltage of the diode increases by the same amount. In normal cases, the drain-source voltage decreases at the same rate as the mirror capacitance is discharged depending on the gate drive voltage, and the gate-source voltage must be maintained at a constant level as in the following period t4-t5 (mirror integrator).

However, in the period t3-t4, the change in drain current resulting from the decrease in reverse recovery current of the diode affects the switching process. If the drain current decreases, the gate source capacitance is discharged via the mirror capacitance. The gate-source voltage decreases to the value sufficient to conduct the drain current. Consequently, sharp drain-source voltage waveforms are generated during this period.

Due attention should be paid to the process in which a change is caused in the drain-source voltage in the period t3-t4. If the MOSFET is driven at low resistance, the drain current increase rate is high, and the change in commutation current of the flywheel diode also increases. Consequently, high reverse recovery current of the diode is generated, which reaches the maximum value and then decreases suddenly. Note that the sharp change in the reverse recovery current of the diode resulting in dissipation may cause excessive voltage increase within the circuit, thus resulting in an overvoltage breakdown.

(2-2) Turn OFF process

Period t8-t9:

The turn OFF process is started at time t8. At time t9, the gate-source voltage decreases to the value allowing the drain current to pass through the resistance area of the output characteristics curve.

Period t9-t10:

In the period t9-t10, the transistor operates as a mirror integrator having a large mirror capacitance.

Period t10-t11:

After the drain-source voltage exceeds the gate-source voltage at time t10, the transistor operates as a mirror integrator having a small mirror capacitance.

Period t11-t12:

The flywheel diode is conducted at time t11, and the drain-source voltage is maintained at a constant level. The drain current decreases in proportion to the gate-source voltage.

Period t12-t13:

When the gate-source voltage is decreases to the threshold voltage at time t12, the drain-source voltage reaches 0.

In the period t12-t13, the input capacitance is discharged to 0.

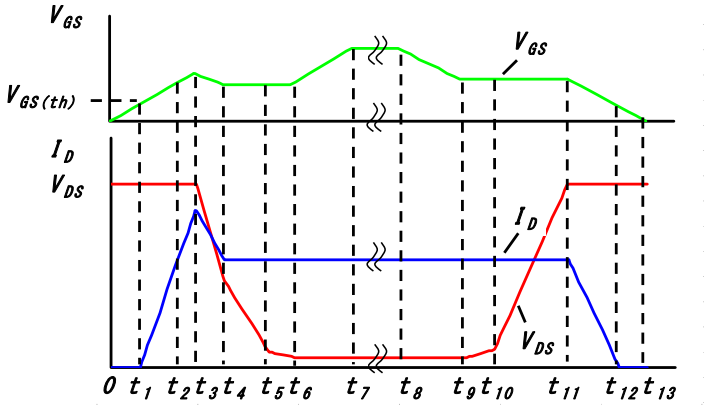


Fig.3-15 Current characteristics at the time of induction load switching

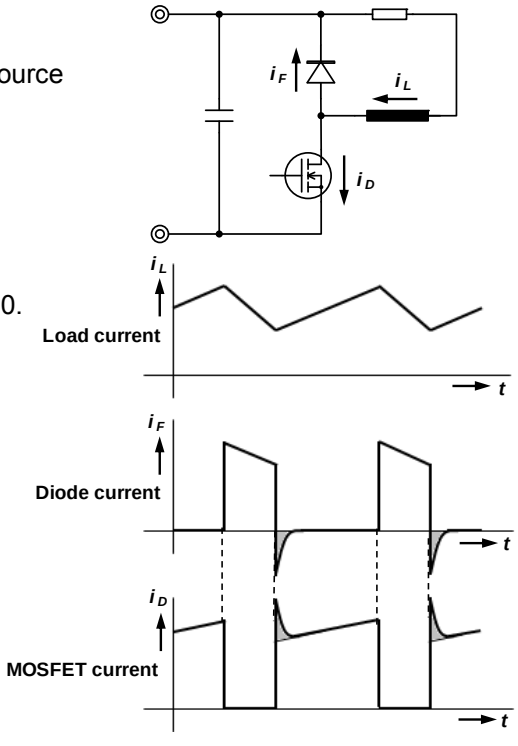


Fig.3-16 Switching characteristics of induction load with flywheel diode

3-11. Derating

Even if you use products within the conditions of the absolute maximum ratings, reliability of products are reduced at the high load conditions close to the absolute maximum ratings. Please apply derating factors as shown in Table 3-1.

Table 3-1 lists the recommended derating factors for 3 hours continuous operation per 1 day over the 10 years.

Table 3-1 Derating condition for the continuous operating
(Case of 3 hours continuous operation per 1 day over the 10 years)

Description	Symbol	Derating Condition
Operating Temperature	Tch	Tch × 80%
Drain-Source Voltage	V_{DS}	V_{DS} × 80%
Continuous Drain Current	I_D	I_D × 80%
Maximum Power Dissipation	P_D	P_D × 50%

4. Circuit design and mechanism of breakdown

4-1. Avalanche breakdown

4-1-1. What is avalanche breakdown?

When an inductance load such as transformer is subjected to high-speed switching using a Power MOSFET, excessive surge voltage may be applied, the withstand voltage of the Power MOSFET may be exceeded, and the breakdown area may be entered. The avalanche breakdown is defined as a mode in which due to avalanche operation the channel temperature Tch and avalanche current I_{AR} exceed the absolute maximum rating, resulting in breakdown.

(1) Mechanism of avalanche breakdown.

Figure 4-1 shows the cross-sectional structure of the MOSFET.
A bipolar transistor exists parasitically within the MOSFET.
If overvoltage is applied to the MOSFET, and the withstand voltage of the device is exceeded, avalanche current is fed.
The major flows of the avalanche current is as follows:

[1] Drain - Rzd - Vzd – Source

[2] Drain - Rzb - Vzb - Rb - Source

First of all, the avalanche current flows by the route of [1] when the avalanche happens. The avalanche voltage increase by generation of heat because of the avalanche current, and the avalanche current begins to flow to the route of [2]. The potential difference is caused by this current in Rb and heat is generated. The resistance of Rb increase by generation of heat, and V_{BE} of a parasitic bipolar transistor decrease. The current that flows in Vzb divides into Rb and V_{BE} when the potential difference in Rb higher than V_{BE} of a parasitic bipolar transistor, and a parasitic bipolar transistor malfunctions. Therefore, the current crowding happens in the part where the avalanche was caused, and MOSFET breakdown.

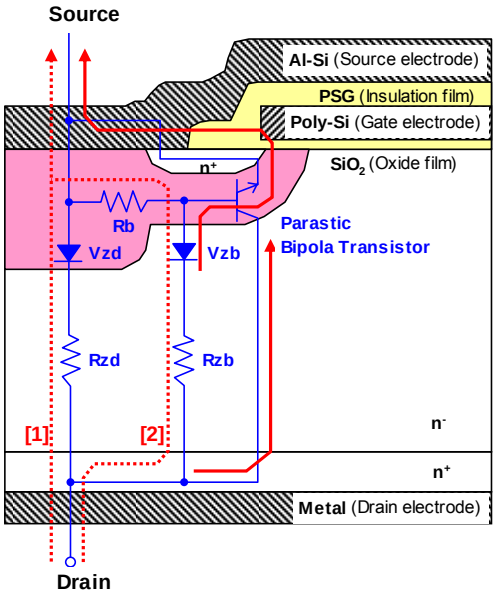


Fig.4-1 Cross-sectional structure of the MOSFET

(2) Technology for increasing the resistance to avalanche breakdown

Generally, to improve the resistance to avalanche breakdown of the MOSFET, the base Rb of the parasitic bipolar transistor is decreased, and a cell structure not allowing concentration of electric field is adopted. The SuperFAP series adopts the following techniques to increase the avalanche capacity.

[1] Adopting a structure where by arranging a simple spherical p diffusion layer carefully, concentration of electric field is loosened to eliminate local concentration of avalanche current

[2] Adopting a structure where by arranging a simple spherical p diffusion layer carefully, the entire area of pn diode is increased, and avalanche permissible current per unit area is increased

[3] Adopting a structure where by forming a high-concentration p+ diffusion layer inside the channel p diffusion layer, the base resistance Rb of the parasitic bipolar transistor is decreased and the operation of the parasitic bipolar transistor is suppressed

(3) Measurement of the avalanche capacity

Figure 4-2 illustrates a circuit for measuring the avalanche capacity of the MOSFET, and Fig.4-3 illustrates the measured waveform. If a voltage exceeding $V_{GS(th)}$ is biased to the gate of the MOSFET, drain current I_D starts to flow within the MOSFET via an inductance L. At this time, the drain current I_D flows within the channel area. If the gate voltage of the MOSFET decreases to $V_{GS(th)}$ or lower, the drain current I_D decreases, whereas the drain voltage V_{DS} surges. The drain voltage V_{DS} increases until it reaches the withstand voltage of the device, and is cramped. The residual energy accumulated in the inductance L continues flowing as drain current I_D. At this time, since the channel area is interrupted, the drain current flows as avalanche current. The capacity of the MOSFET of consuming the energy accumulated in the inductance L is defined as the avalanche capacity.

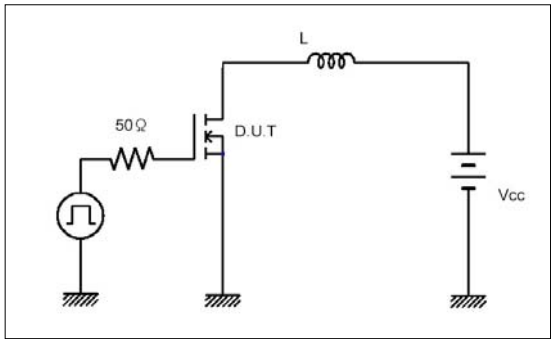


Fig.4-2 Avalanche capacity measurement circuit

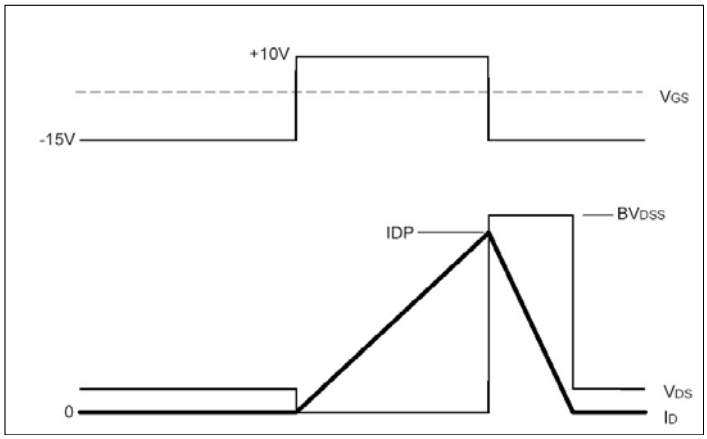


Fig.4-3 Avalanche waveform

(4) How to guarantee the avalanche capacity

The SuperFAP series defines the avalanche capacity using the following items:

[1] Avalanche current I_{AR}

Permissible current at occurrence of an avalanche.

Generally, permissible avalanche current decreases with the increase of temperature, which is why temperature derating is provided in some cases. The SuperFAP series do not provide temperature derating, and guarantee is made in the same temperature range.

[2] Avalanche energy E_{AS}

The permissible avalanche energy at single pulse at the specified power voltage and under inductance condition. Since it is restricted by channel temperature, the permissible energy varies depending on the operating temperature conditions.

(5) Feasibility of use under avalanche condition

The following must be satisfied when using the MOSFET for actual avalanche operation:

[1] The current value at the time of avalanche is the lower than the guaranteed avalanche current.

[2] The channel temperature falls within the guarantee range (normally Tch≤150deg.).

The channel temperature in [2] must be considered even when avalanche operation is not performed. Since power dissipation increases under avalanche operation, more attention should be paid.

Figure 4-4 illustrates the waveform at turn OFF in actual avalanche operation. There may be a case in which even if the voltage at turn OFF exceeds the maximum rated withstand voltage V_{DS}, avalanche current may not be fed due to high withstand voltage of the device. In such cases, power dissipation calculation should be made assuming that avalanche is occurring during the period in which the maximum rated withstand voltage V_{DS} of the device is exceeded.

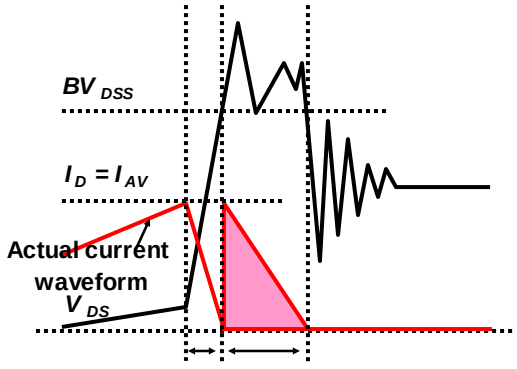


Fig.4-4 Typical waveform at avalanche operation

4-2. ASO breakdown

ASO breakdown is classified into overcurrent, overpower, and overvoltage breakdowns.

4-2-1. Overcurrent breakdown

Due to short circuit of loads, etc., current exceeding the area restricted by the drain current I_D and pulsed drain current I_{DP} in ASO is fed, causing the device to heat up and resulting in breakdown or melting of the internal wiring of the package, which is defined as overcurrent breakdown.

4-2-2. Overpower breakdown

If the drain current I_D and the drain-source voltage V_{DS} are simultaneously applied, power dissipation exceeding the area restricted by the maximum power dissipation P_D in ASO is generated, thus causing the device to heat up excessively, which is defined as overpower breakdown.

4-2-3. Overvoltage breakdown

If a large surge voltage exceeding the area restricted by the drain-source voltage V_{DSS} (withstand voltage) in ASO is applied due to high-speed switching of an inductance load such as transformer, and thus the breakdown area is entered, the device is heated abnormally, resulting in breakdown or avalanche breakdown, which is defined as overvoltage breakdown.

4-3. Diode breakdown

4-3-1. What is diode breakdown?

In a bridging circuit using a drain-source parasitic diode, sharp change in voltage (dv/dt) and/or current (di/dt) during reverse recovery operation of the parasitic diode causes the parasitic bipolar transistor of the MOSFET to arc and large current to be fed, thus resulting in uncontrollable state and breakdown, which is defined as diode breakdown.

4-3-2. Mechanism of diode breakdown

If voltage is applied in reverse direction in a state in which current is fed to the parasitic diode (voltage is applied between D and S), the parasitic diode performs reverse recovery operation. A part of this recovery current is fed through the Rb of the parasitic bipolar transistor via route [2] in Fig.4-5 as in the case of an avalanche. In this case, the charging current to the parasitic capacitance Cds (=Cvzd+Cvzb) via the recovery dv/dt is also fed to the Rb of the parasitic bipolar transistor. Due to the composite effect of these two currents, potential difference is generated in the Rb, and consequently parasitic bipolar transistor (between B and E) is biased. When current starts to flow from the drain through the parasitic bipolar transistor to the source, the temperature of the parasitic bipolar transistor increases, causing the resistance value of the Rb to increase and parasitic bipolar transistor threshold voltage VEB to decrease, which further causes the parasitic bipolar transistor to be biased, current is concentrated, thus resulting in a breakdown of the MOSFET. To prevent this from occurring, restrictions are imposed on the recovery di/dt affecting the recovery current and the recovery dv/dt affecting the charging current.

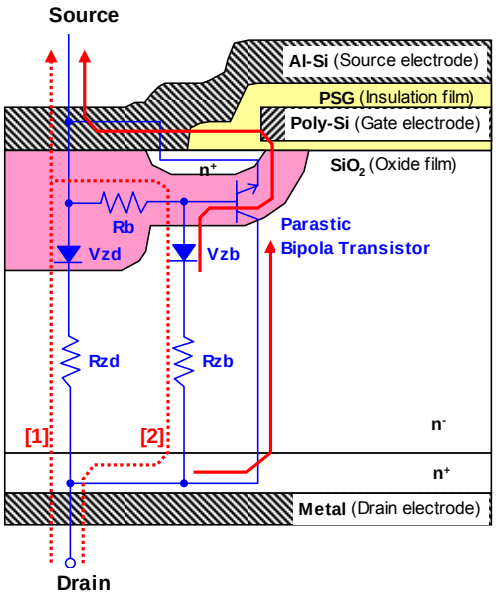


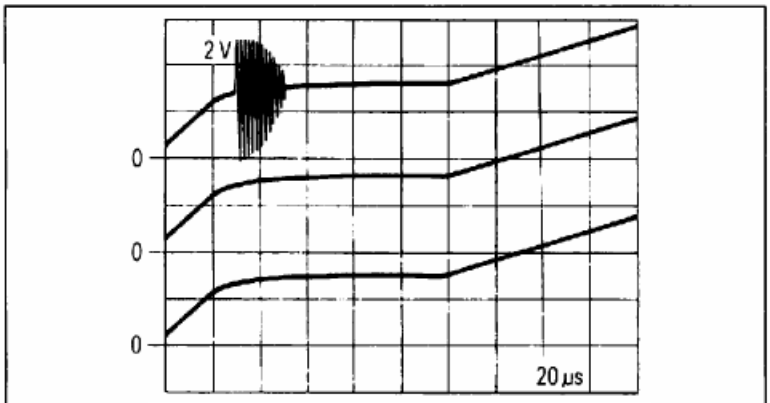
Fig.4-5 Current route at avalanche breakdown

4-4. Breakdown due to parasitic oscillation

As a result of directly connecting gate terminals (without inserting gate resistance Rg in between) when connecting devices in parallel, or sudden change in the drain-source voltage or current at the time of turn ON/OFF, parasitic oscillation occurs at the gate. Due to this parasitic oscillation, the gate-source voltage V_{GS} may exceed the rated voltage V_{GS}, or the device may malfunction due to the parasitic oscillation of the gate, thus resulting in thermal breakdown, which is called a breakdown due to parasitic oscillation.

The gate breakdown that occurs due to static electricity or parasitic oscillation is in two modes: One is thorough breakdown, namely short circuit between the gate and the source or between the drain and the source [1], and the other is halfway operation in which the impedance between the gate and the source decreases whereas the leakage current between the drain and the source increases [2]. Under normal operating conditions, the trace of breakdown increases due to short circuit between the drain and the source in mode [1], and in mode [2] the operation by voltage whose VGS is lower than prescribed causes malfunction to occur and leakage current to increase, thus resulting in ASO breakdown. It is therefore difficult to judge the occurrence of gate breakdown from the trace of the breakdown.

Figure 4-6 shows parasitic oscillation waveform when the gates of the MOSFET are directly connected in parallel. This oscillation occurs when the drive voltage reaches the threshold voltage of the MOSFET and the drain current starts to flow.



Top: Each gate is connected directly.
Center: A 10Ω resistance is connected to each gate in series.
Bottom: A ferrite bead is connected to each gate in series.

Fig.4-6 Change in gate-source voltage at parallel switching

This oscillation occurs because of extremely high forward transconductance of the MOSFET. The resonance circuit consists of an external circuit, inductance of each MOSFET itself, and the parasitic capacitance. The voltage generated due to this oscillation exceeds the maximum gate-source voltage value in many cases, thus breaking the device. It is therefore recommended to connect a resistance of 4.7Ω or higher to each gate of the MOSFET connected in parallel.

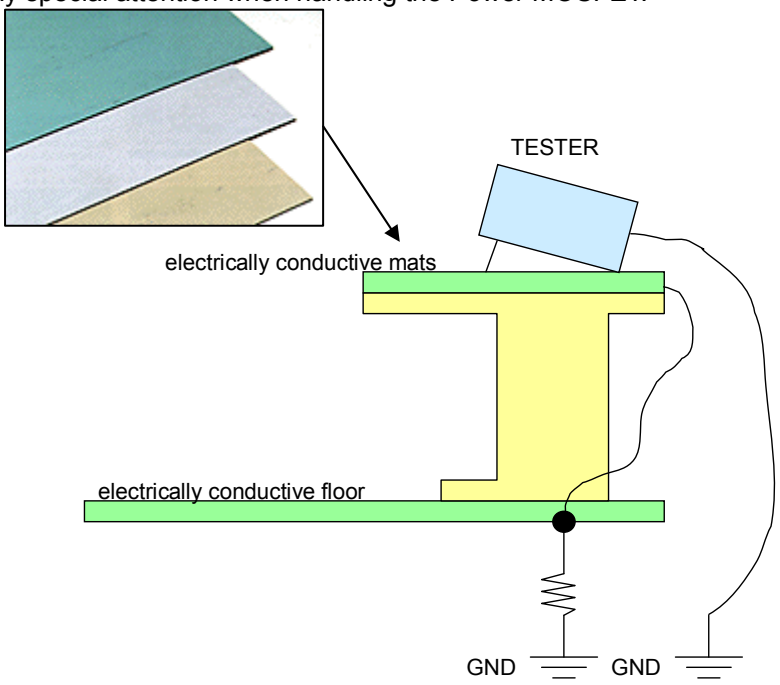
4-5. Electrostatic breakdown

4-5-1. What is electrostatic breakdown?

If static electricity or surge voltage is applied to the gate terminal of the MOSFET through human body or experimental devices, the resistance to static electricity at the gate terminal is exceeded, thus resulting in a breakdown, which is defined as electrostatic breakdown.

4-5-2. Prevention of electrostatic breakdown of the Power MOSFET (measures)

Compared with small-signal MOSFET and MOS IC, the Power MOSFET has significantly higher oxide film resistance. However, since damage may occur due to static electricity as in the case of these MOS products, pay special attention when handling the Power MOSFET.



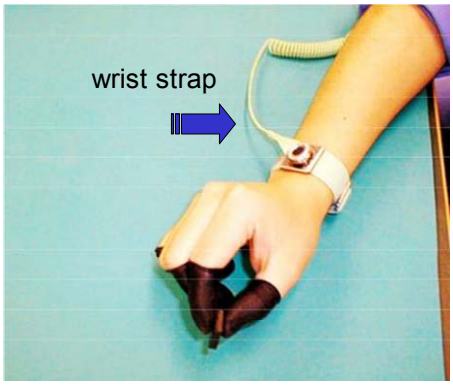


Fig.4-7 Example of measures against breakdown by static electricity

(1) How to discharge static electricity from an electrostatic body

When making a workbench protected against static electricity, proper use of an electrically conductive table mat, wrist strap, and floor mat allows static electricity built up to be removed. The speed of removing the charge is determined based on the resistance on the capacitance route of the conductive body. Figure 4-8 shows an equivalent circuit in which the conductive body has capacitance C and the route resistance of R.

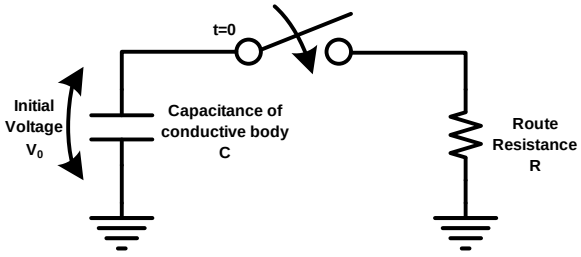


Fig.4-8 Equivalent circuit for static electricity discharge

The voltage of the conductive body is expressed by the following formula as the function of time t:

$$V = V_{0\exp}\left(-\frac{t}{RC}\right)$$

V = Voltage [V] of the charged body at time t
V_0 = Initial voltage [V] of the charged body
t = Second
C = Capacitance [F] of the charged body
R = Route resistance [Ω]

<Example>
Assume that the static electricity level of a worker is decreased to 100V or lower within one second according to technical material TB57-1 of the Electric Industries Association of Japan (EIAJ). Substitute the following into the above formula:

V = 100V (safe voltage)

V_0 = 10kV (Initial voltage of the human body or charged body)

t = 1sec. (Longest permissible time for achieving the safe voltage of 100V)

C = 200pF (Average of human capacitance 100pF to 400pF)

R = Maximum permissible resistance [Ω] to the ground

$$100 = 1 \times 10^{4} \cdot \exp\left(-\frac{1}{200 \times 10^{-2} \cdot R} \right)$$

$R \approx 1.09 \times 10^{9}\Omega$ = 1090 MΩ

can thus be obtained. From this calculation, it is found that if the resistance from the table mat, floor mat, or wrist strap to the ground is $10^{9}\Omega$ or lower, discharge to obtain safe voltage, 100V, can be performed within one second, and the parts can thus be protected against electrostatic breakdown.

- About the breakdown value of a device due to electrostatic discharge

Table 4-1 lists the voltage range in which various devices may result in breakdown due to electrostatic discharge from workers.

Table 4-1 Breakdown voltage by device

Type	Voltage range [V]
MOSFET	100 ~ 200
Junction FET	140 ~ 10000
C MOS	250 ~ 2000

5. Thermal design

5-1. Concept of heat dissipation

(1) Transient thermal impedance and steady thermal resistance

The heat dissipation treatment of power dissipation that occurs at the channel of a Power MOSFET is performed by mounting the MOSFET to a cooling body, or by the device itself. Figure 5-1 simulates the heat radiation route in the former case in an electrically equivalent circuit.

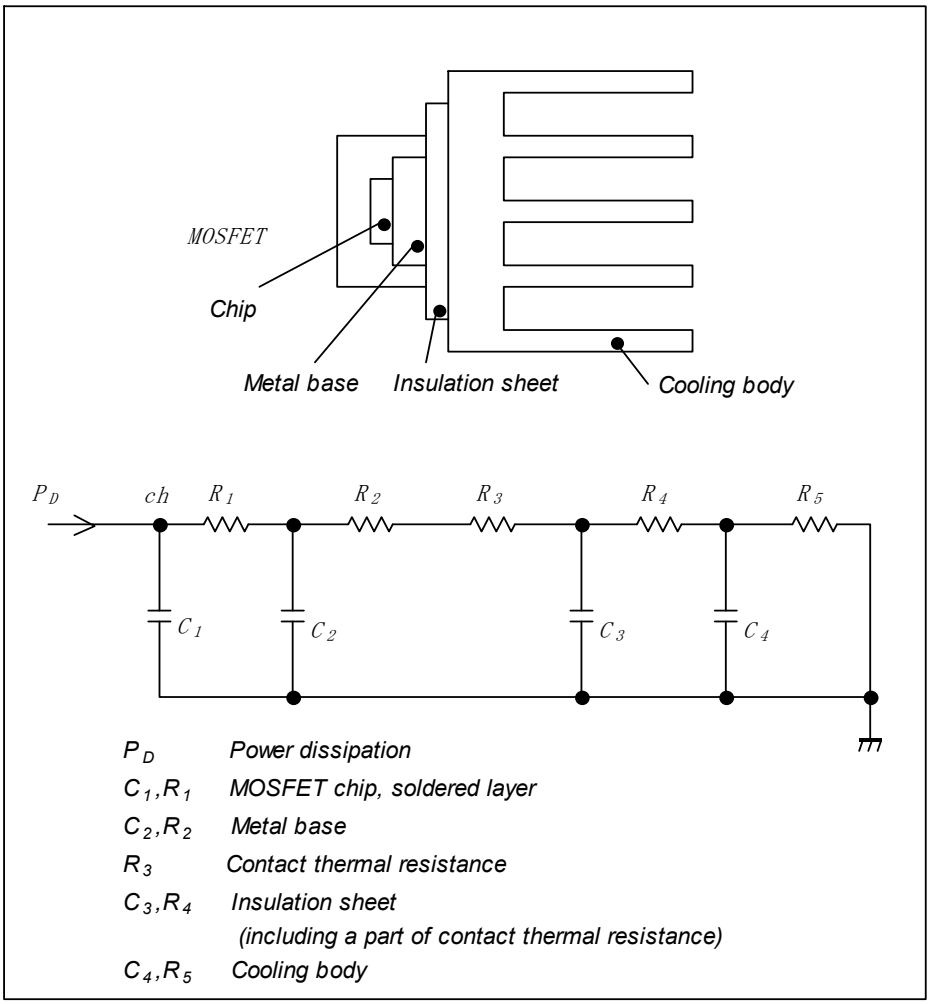


Fig.5-1 Electric equivalent circuit showing thermal behavior

In the equivalent circuit in Fig.5-1, the transient thermal impedance is the thermal resistance within the time range affected by the thermal capacitances C1 to 4, and is the function of time. As the transient thermal impedance characteristics of each device, the maximum value is displayed on the data sheet, which is equivalent to D ≈ 0. The transient thermal impedance of the cooling body is found by the following formula:

$$Rf(t) = R_{f-a}\left(1-\varepsilon^{-\frac{t}{\tau f}}\right)$$

where, $\tau f = R_{f-a} \cdot V \cdot \gamma \cdot C$

Rf-a	: Cooling body steady thermal resistance [deg./W]
t	: Time [S]
τf	: Thermal time constant of the cooling body [S]
V	: Cooling volume [cm^3]
γ	: Specific gravity [g/cm^3]
C	: Specific heat [W• S/g• deg.]

Table 5-1 lists the specific gravity of materials required for this calculation, and Fig.5-2 illustrates the steady thermal resistance of an aluminum cooling plate (coated in black).

Table 5-1 Specific gravity and specific heat of each material

Material	Specific gravity γ [g/cm^3]	Specific heat [W• S/g• deg.]
Aluminum	2.71	0.895
Copper	8.96	0.383

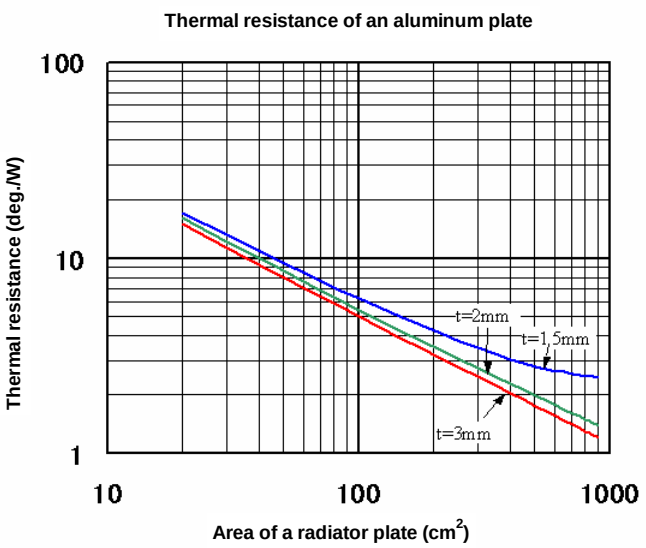


Fig.5-2 Steady thermal resistance of the aluminum cooling plate

Meanwhile, since the steady thermal resistance is not affected by thermal capacitance at all, the channel temperature can be found easily.

$$Tch = Ta + (Rch\text{-}c + Rc\text{-}i + Ri + Ri\text{-}f + Rf\text{-}a) \cdot P_D$$

Tch : Channel temperature
Ta : Ambient temperature
$R_{ch\text{-}c}$: Thermal resistance between channel and case (MOSFET thermal resistance)
R_i : Insulation sheet
$R_{c\text{-}i}$, $R_{i\text{-}f}$: Contact thermal resistance
$R_{f\text{-}a}$: Thermal resistance of cooling body
P_D : Generated power dissipation

5-2. Transient thermal impedance characteristics of the device

The specification of the MOSFET lists the transient thermal impedance characteristics of the device to assist thermal designing. Figure 5-3 illustrates the transient thermal impedance characteristics of the FMV06N60ES. For example, assume a single pulse having pulse width of 1 ms, and the permissible power dissipation P_D in the case in which the device is mounted to a cooling body of 5deg./W under Ta=40deg. condition can be calculated by using the following formula:

$$P_D = \frac{Tch(\max) - Ta}{Rthf\text{-}a + Rth(1ms)} = \frac{150℃ - 40℃}{5℃/W + 0.15℃/W} \approx 21.4\ [W]$$

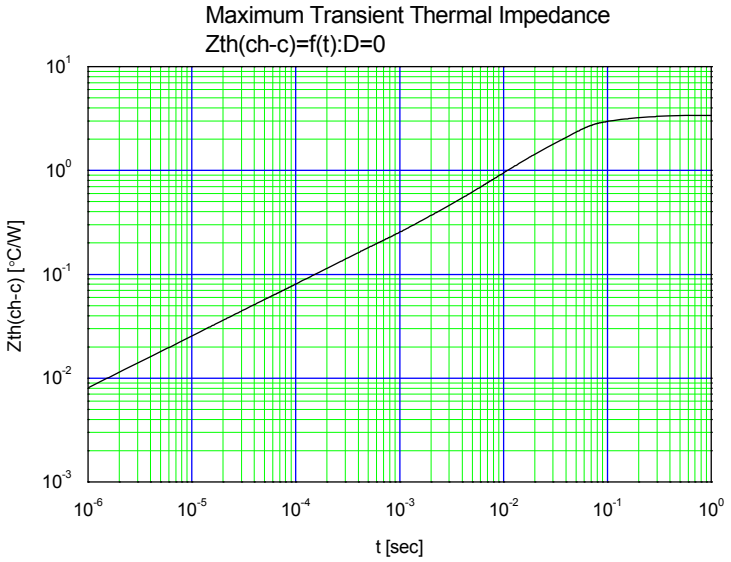


Fig.5-3 Transient thermal impedance characteristics of the FMV06N60ES

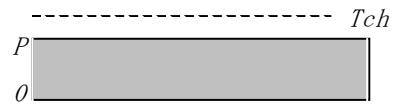
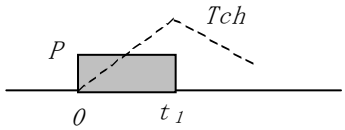
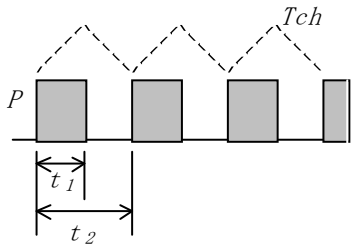
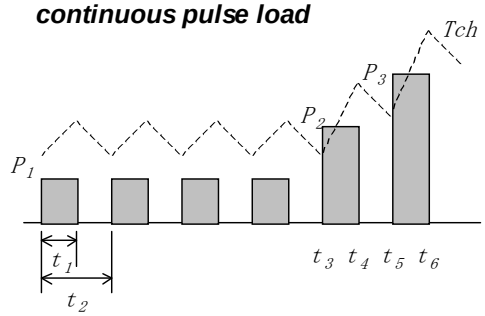
5-2. Calculation of channel temperature

When using a MOSFET, it is essential that the channel temperature fall within the maximum rating under the operating condition. It is therefore necessary to find the channel temperature based on the operating waveforms, thus verifying whether the MOSFET can be used or not.

(1) Calculation of channel temperature for rectangular wave power dissipation

Table 5-2 lists the channel temperature calculation formulae for continuous load, single pulse load, continuous pulse load, and irregular pulse load following the continuous pulse load.

Table 5-2. Channel temperature calculation formula

Load	Channel temperature calculation formula
Continuous load 	$Tch = Ta + P \cdot Rthch\text{-}a$
Single pulse load 	$Tch = Ta + P \cdot Rth(t1)$
Continuous pulse load 	$Tch = Ta + P\left\{\frac{t_1}{t_2} \cdot Rthch\text{-}a + \left(1 - \frac{t_1}{t_2}\right) \cdot Rth(t_1 + t_2) - Rth(t_2) + Rth(t_1)\right\}$
Irregular pulse load following continuous pulse load 	$Tch = Ta + P_1 \cdot \left\{\frac{t_1}{t_2} \cdot Rthch\text{-}a + \left(1 - \frac{t_1}{t_2}\right) \cdot Rth(t_1 + t_2) - Rth(t_2)\right\} + P_2 \cdot \{Rth(t_6 - t_3) - Rth(t_6 - t_4)\} + P_3 \cdot Rth(t_6 - t_5)$

(2) Calculation of channel temperature for complicated power dissipation waveforms

If the MOSFET has a complicated power dissipation waveform, the channel temperature can be calculated by converting the waveform into a rectangular wave as shown in the dotted line in Fig.5-4, and based on the concept of superposition.

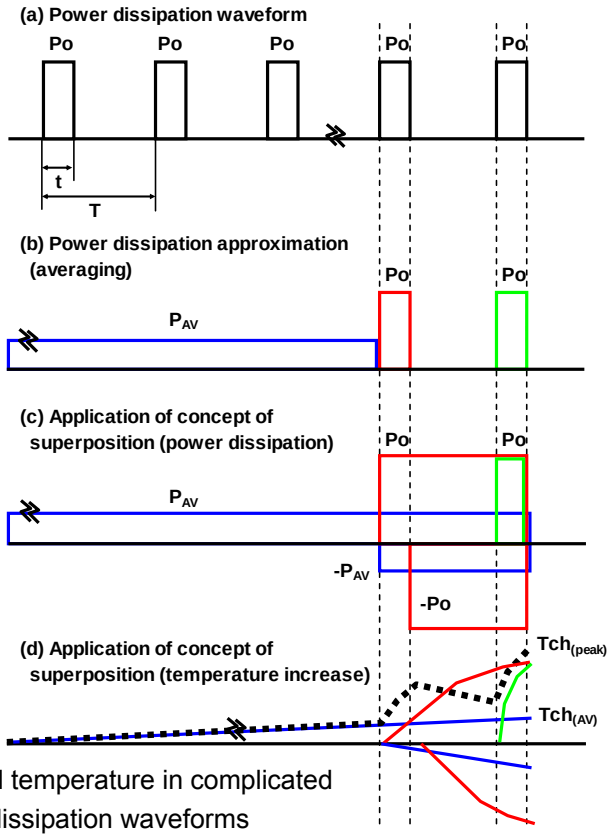


Fig.5-4 Channel temperature in complicated power dissipation waveforms

(3) Specific channel temperature calculation

To calculate the channel temperature of the MOSFET, the following are required:

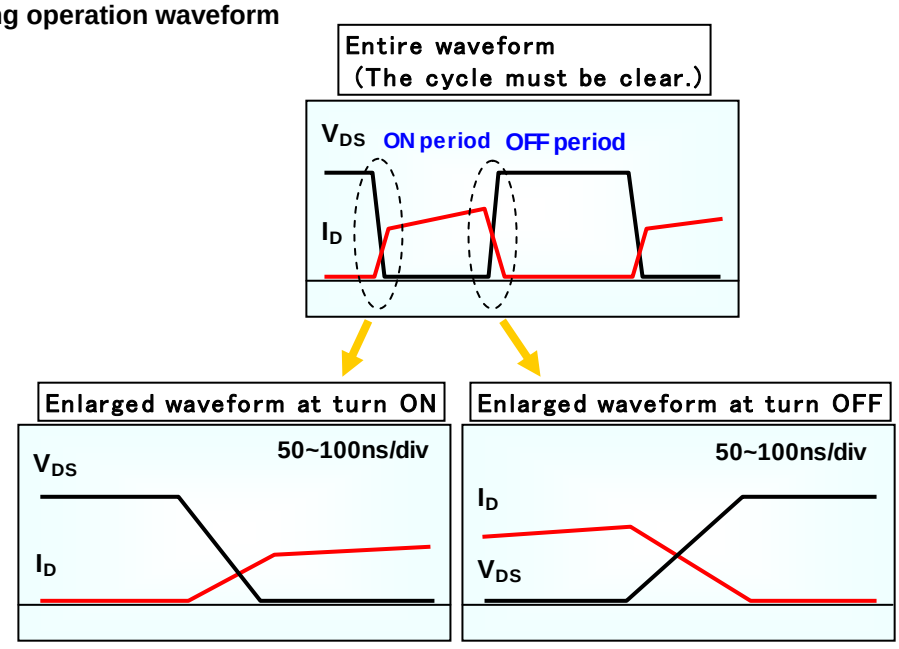
(a) Waveform for one cycle (VDS, ID, and cycle T must be clear.)

(b) Expansion of turn ON/OFF waveform

(c) Operating condition (case temperature Tc, etc.)

The steps for calculating channel temperature are shown below.

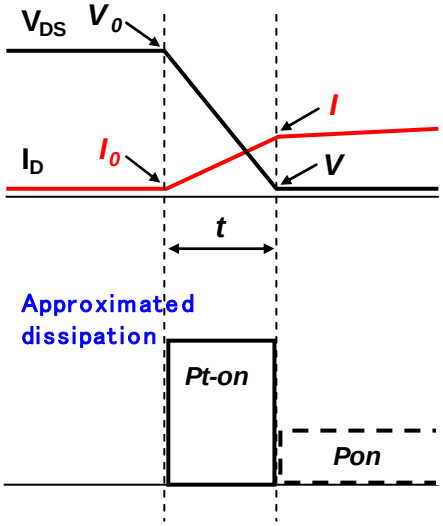
[1] Obtaining operation waveform



* If turn ON dissipation and turn OFF dissipation can be ignored, the waveform need not be obtained.

[2] Approximation of operation waveform

Operation waveform at turn ON



Power dissipation is calculated by the following formula:

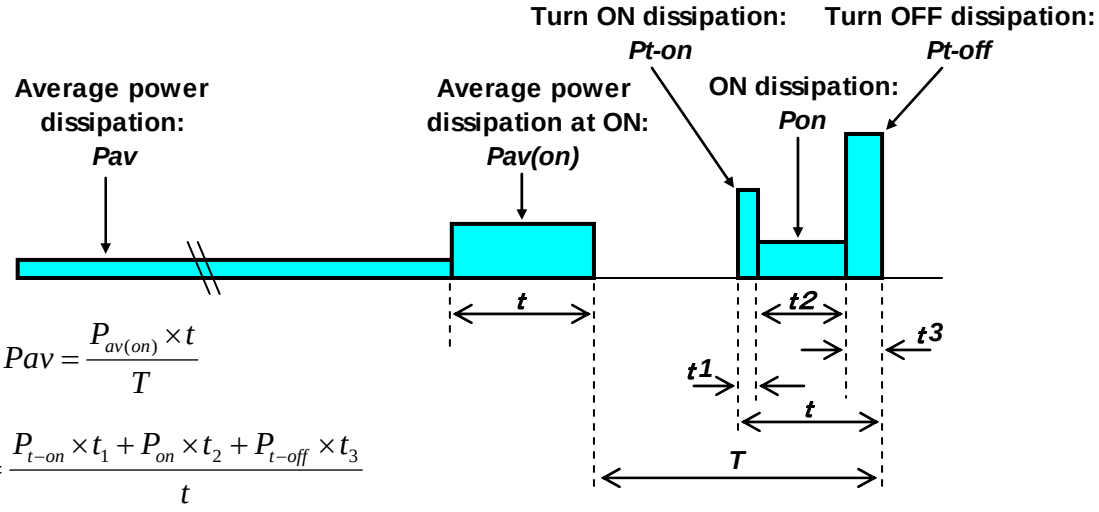
$$\alpha = -\frac{I_0 - I}{t}$$

$$\beta = -\frac{V_0 - V}{t}$$

$$P_S = \int_0^t (\alpha t + I_0)(\beta t + V_0)dt$$

$$P = \frac{P_S}{t}$$

If the power dissipation for the turn ON period is calculated using the above formula, the result of the calculation "P" is expressed as "Pt-on."



$$Pav = \frac{P_{av(on)} \times t}{T}$$

$$P_{av(on)} = \frac{P_{t-on} \times t_1 + P_{on} \times t_2 + P_{t-off} \times t_3}{t}$$

* If the turn ON dissipation and turn OFF dissipation can be ignored, they need not be taken into consideration.

[3] Calculation of transient thermal impedance

The transient thermal impedance value at each time can be read from the transient thermal impedance chart in Fig.5-5. Note, however, that if the pulse width is 1 ms or shorter, the value can be found by using the following formula:

Example: In the case of pulse width of (Ta)

$$Rth_{(ch-c)(Ta)} = Rth_{(ch-c)(1ms)} \times \sqrt{\frac{Ta}{0.001}}$$

$Rth_{(ch-c)(1ms)}$: Duty=0, Transient thermal impedance value at 1ms

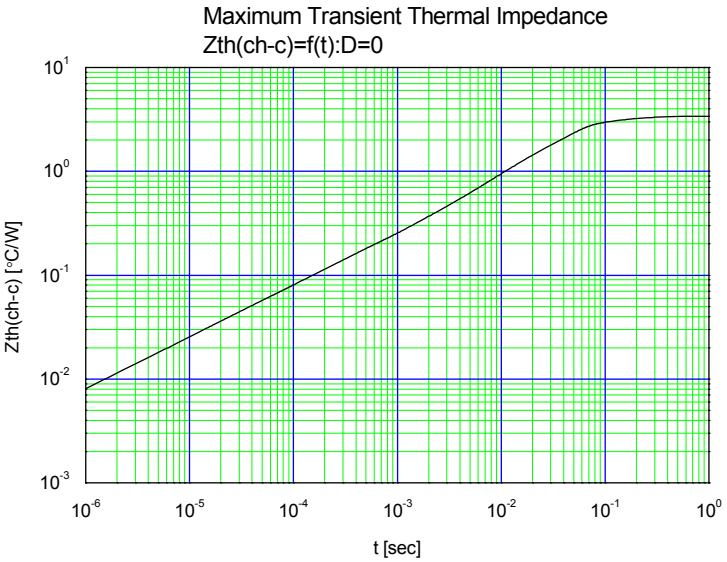
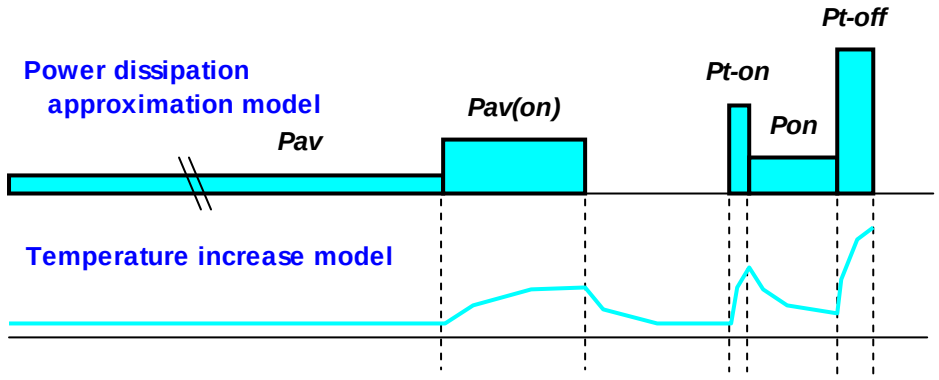


Fig.5-5 Transient thermal impedance chart

[4] Calculation of channel temperature



Channel temperature increase calculation formula :

$$\Delta T_{ch-c} = P_{av} \times Rth_{(ch-c)} + \left(P_{av(on)} - P_{av}\right) \times Rth_{(T+t)} - P_{av(on)} \times Rth_{(T)}$$
$$+ P_{t-on} \times Rth_{(t)} + \left(P_{on} - P_{t-on}\right) \times Rth_{(t2+t3)} + \left(P_{t-off} - P_{on}\right) \times Rth_{(t3)}$$

* If turn ON dissipation and turn OFF dissipation can be ignored, they need not be taken into consideration.

6. Cautions in mounting and handling

To ensure safe operation over a long period of time, follow the precautions on handling shown below.

(1) Soldering

When a semiconductor device is soldered, the temperature of the lead exceeds the maximum rated storage temperature. Since quality assurance regarding the resistance against soldering is applicable to the level shown below, perform soldering within the listed range.

(a) Recommended mounting condition

Categories	Packages	Methods				
		Wave Soldering (Full dipping)	Wave Soldering (Only terminal)	Infrared Reflow	Air Reflow	Soldering iron (Re-work)
Through-Hole	TO-3PL	Unable	Possible	Unable	Unable	Limited to 1time
	TO-3P	Unable	Possible	Unable	Unable	Limited to 1time
	TO-247	Unable	Possible	Unable	Unable	Limited to 1time
	TO-3PF	Unable	Possible	Unable	Unable	Limited to 1time
	TO-220	Unable	Possible	Unable	Unable	Limited to 1time
	TO-220F	Unable	Possible	Unable	Unable	Limited to 1time
	T-Pack(L)	Unable	Possible	Unable	Unable	Limited to 1time
	K-Pack(L)	Unable	Possible	Unable	Unable	1time
Surface Mount	T-Pack(S)	Unable	Unable	Possible	Possible	Unable
	T-Pack(SJ)	Unable	Unable	Possible	Possible	Unable
	K-Pack(S)	Unable	Unable	Possible	Possible	Unable
	TFP	Unable	Unable	Possible	Possible	Unable

- Through-Hole Package

Soldering temp.	Immersion time
260±5 deg.	10±1 sec
350±10 deg.	3.5±0.5 sec

- Surface Mount Package

Number of times(Reflow)	Twice
Soldering Temp. & Time	≥230 deg., ≤50sec
Package surface Peak Temp. & Time	≤260 deg., ≤10sec

(b) The immersion depth of the lead should be up to 1 to 1.5 mm from the device main unit.

(c) Be careful not to let the device main unit be immersed in soldering liquid when mounting the device by the solder flow method.

(d) When using a flux, it is desirable to use rosin series flux, and not chlorine series flux.

(e) Recommended reflow

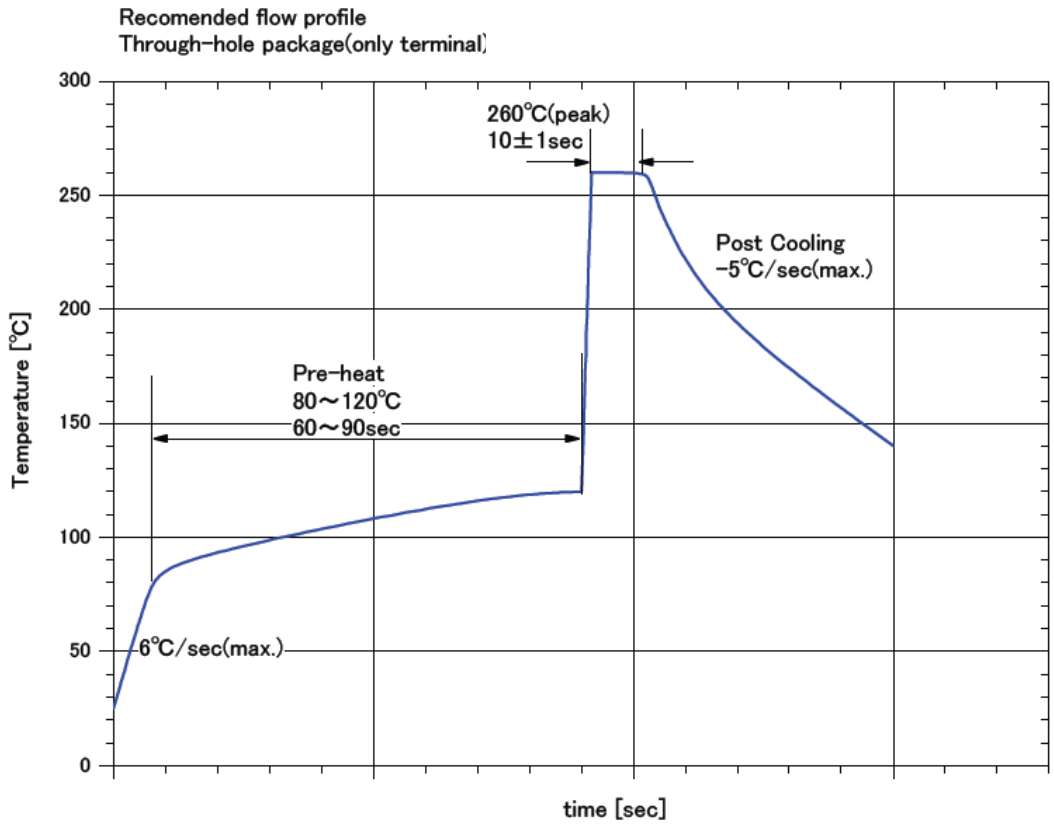


Fig.6-1 Recommended reflow profile (through hole/Pb-free solder specification)

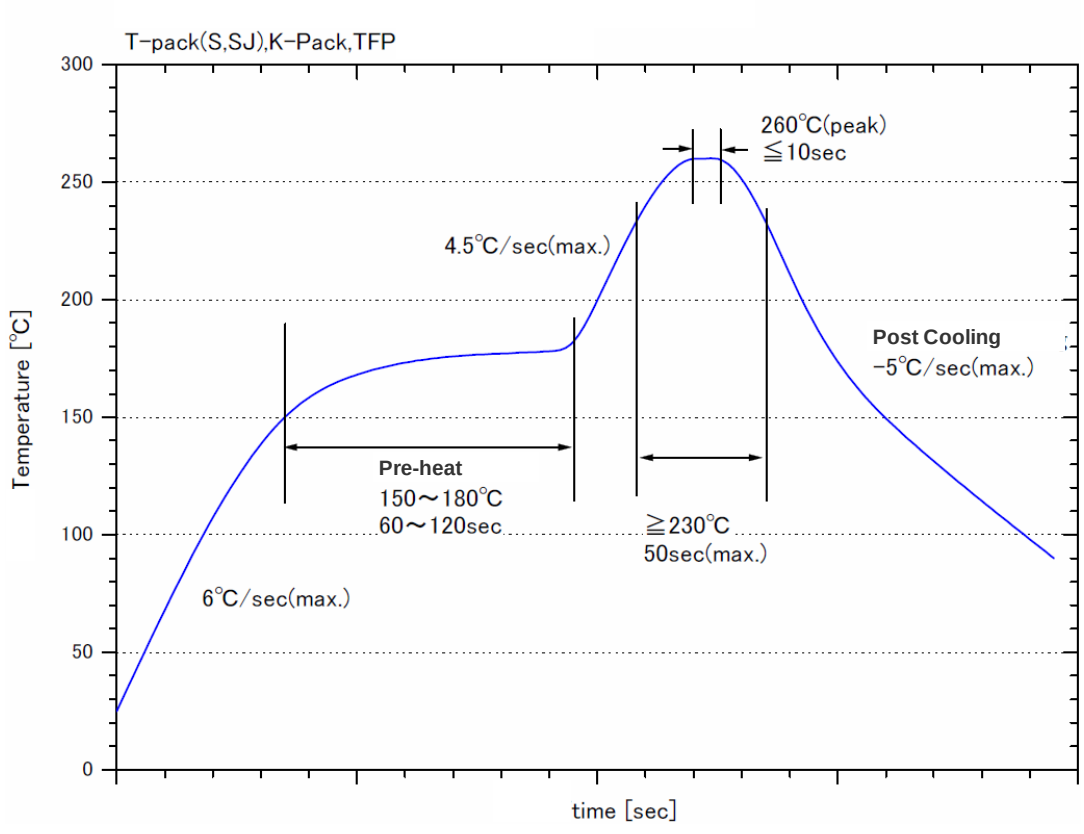


Fig.6-2 Recommended reflow profile (SMD/Pb-free solder specification)

(2) Processing and mounting of through hole terminal
Handling of lead wire of resin-sealed power transistor
(a) Stress to the lead wire
If stress of more than necessary is applied to the electrode lead of a semiconductor device, the internal chips and external package may be damaged. To prevent this from occurring, keep the load applied in the direction shown in Fig.6-3 to 1kg or lower.

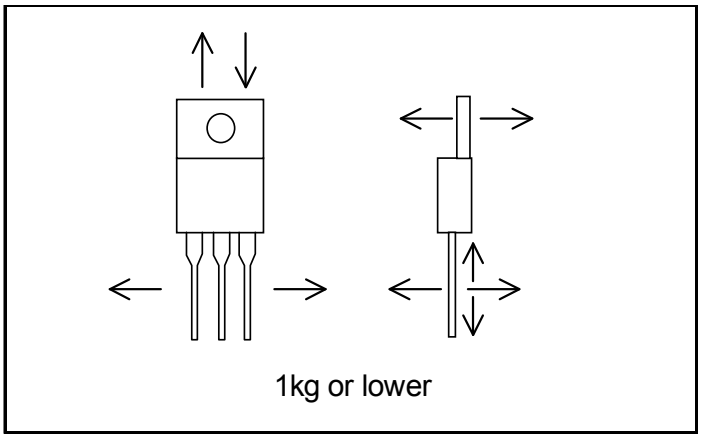


Fig.6-3 Stress to the lead wire

(b) Caution in molding a lead
If there is no other choice but to mold a lead for convenience of parts layout, pay attention to the following:

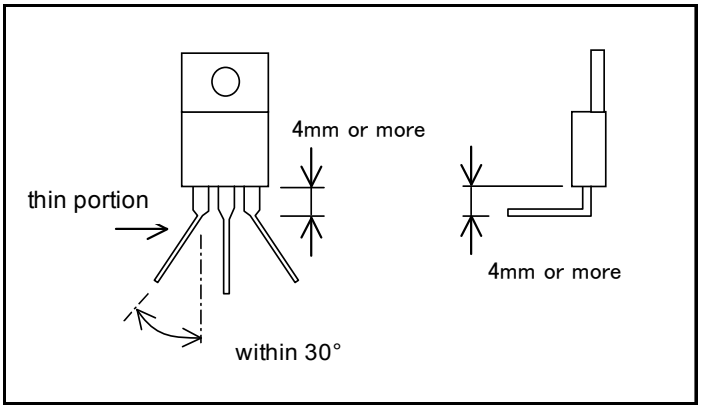


Fig.6-4 Cautions in molding a lead

•Provide an exclusive jig that does not allow stress shown in Fig.6-4 to be applied.
•When bending the lead in the horizontal direction, bend it at the thin portion or at the part 4 mm or more away from the transistor main unit, and keep the bending angle within 30°.
•When bending the lead at the right angle against the type displaying surface, bend it at the portion 4 mm or more away from the transistor main unit.
•Molding should be performed only once at a place, and do not perform re-molding or restore the original shape.

(c) Insertion into the printed board
When inserting a lead to the printed board, coincide the interval of lead wires and that of insertion holes to prevent excessive stress from being applied to the root portion of the leads.
To prevent the lead soldered to the printed board from being forcibly bent to mount it to a radiator plate, perform mounting work first and then perform soldering.

(3) Washing (Common to through hole and SMD)

When soldering is performed using a flux, washing with solvent is required in general. In this case, pay attention to the following:

(a) Solvent

•Do not use flammable, toxic, or corrosive solvents.

•Never use a trichloroethylene series solvent because it contains chlorine.

(b) Washing method

It is desirable to perform washing by immersing the portion to be washed. If ultrasonic washing is to be performed, set the frequency, avoiding the resonance point (several tens of kHz), and pay attention not to let the device or printed board to directly contact the oscillation source.

(4) Mounting to a radiator plate

(a) If the fastening torque of the screw for mounting is too low, the thermal resistance increases. On the contrary, if it is too high, the device may be deformed, thus resulting in a failure.

Consequently, it is recommended to fasten the screws at the torque listed in Table 6-1.

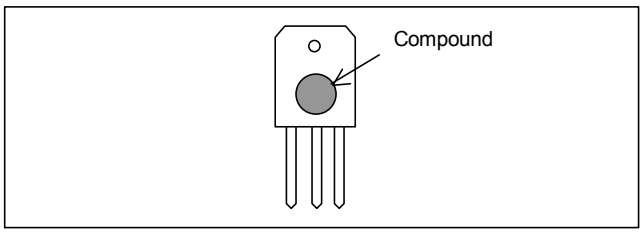
Table 6-1. Semiconductor device fastening torque

Package	Diameter of mounting hole	Screws used	Optimum fastening torque (N•cm)
TO-220AB	φ3.6	M3	30-50
TO-220F	φ3.2	M3	30-50
TO-3P	φ3.2	M3	40-60
TO-247	φ3.2	M3	40-60
TO-3PF	φ3.2	M3	40-60
TO-3PL	φ3.2	M3	60-80

(b) It is recommended to apply a compound thinly and uniformly to improve the thermal conductivity between the semiconductor device main unit and the radiation plate, thus improving heat dissipation effect.

(c) Application of thermal compound

As a method for allowing a thermal compound to exist between the device and a cooling body, a compound is applied uniformly to the device, which is then mounted to the cooling body. However, in the case of small products such as the TO220 package, the application work is cumbersome. As a method for filling the gap between the device and the cooling body with a compound, apply an appropriate amount of compound to the case immediately below the semiconductor device chip-mounting portion in a shape of a point, and fasten the device to the cooling body with screws, and the compound expands, filling the gap, and a compound layer containing few air bubbles can thus be formed easily.



<Small package such as TO3P>

(d) We recommend the processing accuracy of ±50 μm for the device mounting surface of the radiator plate.

(e) When fastening one device with screws at 2 positions, pay special attention to fasten the screws uniformly.

(f) Surface flatness ≤ ±30 μm

(g) Surface roughness ±10 μm

(h) Do not taper threaded holes.

(5) Cautions in storage and transportation

(a) Storage

(i) It is desirable that semiconductor devices be stored in a place of normal temperature and humidity. Avoid storing the devices in a place of temperature and humidity far away from the normal values, which are approximately 5 to 35deg. and 45 to 75% respectively. When storing molded type power transistors in an area that becomes extremely dry in winter, humidification by a humidifier is required. If tap water is used for humidification, chlorine contained in it may cause corrosion of the leads of the device. To prevent this from occurring, use pure water or boiled water for humidification.

(ii) Avoid storing semiconductor devices in a place where corrosive gas is generated or subjected to much dust.

(iii) Avoid storing semiconductor devices in a place subjected to sharp temperature change. Otherwise condensation may occur to the devices. Store the devices in a place having minimum temperature change.

(iv) Pay attention not to apply load to semiconductor devices during storage. In particular, if they are stored, stacked on top of each other, unexpected load may be applied.

(v) Store the semiconductor devices with each terminal kept unprocessed to avoid occurrence of corrosion, which may result in insufficient soldering at the time of processing.

(vi) Contain the devices in a container that does not take static electricity easily, or the one used for the delivery of the product.

(vii) All the shelves for storage should be made of a metal. Be sure to ground them.

(b) Transportation

(i) Be careful not to have impact on the devices by dropping them, etc.

(ii) When transporting large number of devices in boxes, place the devices by inserting a soft spacer to prevent the contact electrode surface, etc. from being damaged.

(iii) When transporting Fuji Power MOSFET, take measures against static electricity using a conductive bag or aluminum foil to prevent static electricity to build up between the gate and the source.

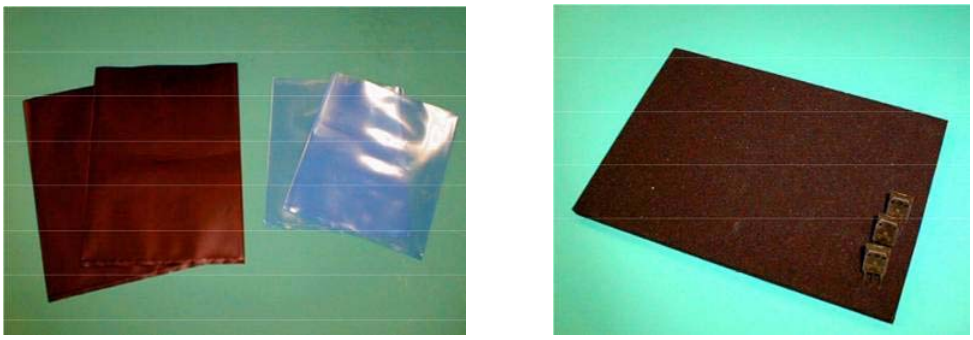


Fig.6-5 Conductive bag (left) and conductive foam (right)

(c) Work environment

(i) The person who handles the Power MOSFET should use a body earth. As a body earth, wear a wrist strap, copper ring, etc., mount a resistance of approximately 1MΩ, and ground it to prevent electric shock.

(ii) Spread a conductive floor mat, tablemat, etc. in a place for handling the Power MOSFET, and be sure to perform grounding.

(iii) When using a measuring device such as curve tracer, also ground the measuring device.

(iv) Before performing soldering, ground the soldering bath to prevent the leak voltage from the soldering iron or bath from being applied to the Power MOSFET.

Be sure to follow the cautions described above to prevent an electrostatic breakdown of the device.

7. Application to switching power supply

7-1. Advantages of Power MOSFET

Feature	Advantage		Disadvantage	
		For users		For users
Power-controlled devaice	• Small drive power • Simple drive circuit	•Saved energy and improved efficiency •Compact and reduced cost •Lower number of parts	•High drive voltage	• Difficulty in applying to low-voltage driving
Majority carrier device	•High switching speed •Excellent radiofrequency characteristics •High resistance to breakdown •Resistant to thermal runaway	•Higher device performance allowed (high-accuracy control etc.) •Downsizing of peripheral devices resulting from higher frequency (transformer, capacitance) •Saved energy and improved efficiency •Improved device reliability •Facilitated heat dissipation design	•Larger ON resistance of high-voltage devices than that of bipolar transistors •Increased ON resistance resulting from temperature increase	• Large power dissipation in low-frequency application (A large radiator plate is required.) •Consideration required for heat dissipation design

Major advantages of the MOSFET include not only high switching speed but also excellent radiofrequency characteristics and independence of switching time of the temperature. By achieving higher frequency of the switching frequency using these advantages, downsizing of radiofrequency transformers and the LC on the secondary side is allowed.

In addition, with the increase of operation frequency, the switching loss (OFF dissipation in particular) becomes dominant, and the effect of the defect of large ON resistance decreases, which is an essential point for selecting devices.

Other features are summarized in the following table:

Item	Feature	Advantage in application
Area of safe operation (ASO)	•Independent of gate reverse bias voltage	•No need of considering reverse bias ASO
Voltage-controlled type	•Low drive power •Simple drive circuit	•No consideration is needed in designing a drive circuit when a large load current range is required for the power supply as in the case of pulse load such as motors
Positive ON resistance temperature characteristics	•Easy parallel connection	

7-2. Points to keep in mind when designing a gate drive circuit

(1) Drive circuit

(a) The drive power dissipation is calculated from Ciss based on the gate charge amount Qg.

Generally, in designing a Power MOSFET drive circuit, the drive power dissipation can be found using the following formula:

Drive power dissipation: $Pd = f \cdot Ciss \cdot (V_{GS})^2$

where,

f : Operation frequency
V_{GS} : Gate-source voltage
t : Switching time

The input capacitance Ciss in this formula in the data sheet is the value obtained with V_{DS} fixed, and the value obtained by substituting this value into the formula deviates from the actual power dissipation. The reason for this is that a gate-drain capacitance C_{GD}, which is a mirror capacitance, exists in the Ciss, C_{GD} is the function of the drain-source voltage V_{DS}, and the gate-source capacitance C_{GS} is the function of V_{GS}. If the Ciss in the above formula is regarded as the function of V_{DS} and V_{GS} in actual designing of a drive circuit, the calculation becomes extremely complicated and cumbersome. Therefore, specifying the gate charge amount Qg as the function of V_{GS} and V_{DS} is the optimum method.
Figure 7-1 illustrates the input charge of the FMV06N60ES (600 V/6 A).

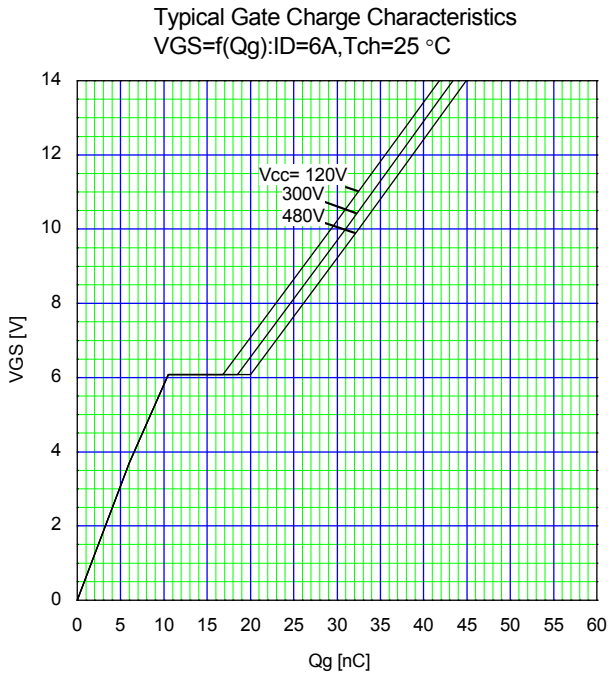


Fig.7-1 Typical Input Charge

The drive power dissipation of the drive circuit can be found based on the gate charge Qg, using the following formula.
Drive power dissipation: $Pd = f \cdot Qg \cdot V_{GS}$

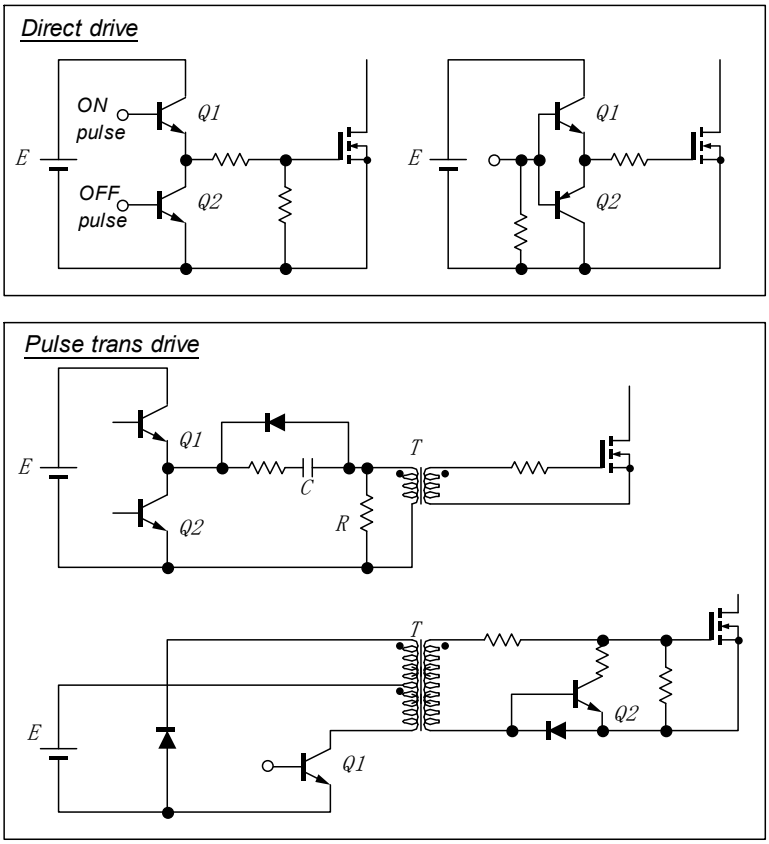
(Example) When driven at V_{GS} = 10 V and f = 200 kHz
- •When the drive power dissipation is calculated using the Ciss defined in the specification:
  Ciss=2280 pF , Pd=0.05W
- •When the drive power dissipation is calculated using the gate charge Qg:
  Qg=54nC , Pd=0.11W

The drive power dissipation calculated using Qg is approximately twice as large as the drive power dissipation calculated using the Ciss defined in the specification.

(b) Other points

Item	Caution
Switching loss	•To decrease the switching loss, measures should be taken to discharge the gate charge in a short time.
Drive circuit voltage	•The voltage should be maintained at least 8V or higher. To achieve this, measures such as stopping the oscillation before V_{GS} decreases to 8V or lower should be taken. •Measures should be taken not to allow V_{GS} to exceed the gate threshold voltage $V_{GS(th)}$ at the time of turning OFF.

<Typical drive circuit>



(2) SuperFAP series and gate resistance Rg

Compared with conventional products, high-speed switching is allowed with the SuperFAP series by reduced the gate charge. Conventionally, the gate resistance was decreased to increase the speed, thus decreasing the switching loss. Meanwhile, with the SuperFAP series, high-speed switching is allowed with a larger gate resistance than that of the conventional one, and the switching loss can be reduced.

Figure 7-2, 7-3, and 7-4 are the charts illustrating the turn OFF dissipation, temperature increase, and power efficiency obtained with the conventional product and the SuperFAP series mounted to the MOSFET for main switching of AC adaptor for 90W worldwide input laptop PCs.

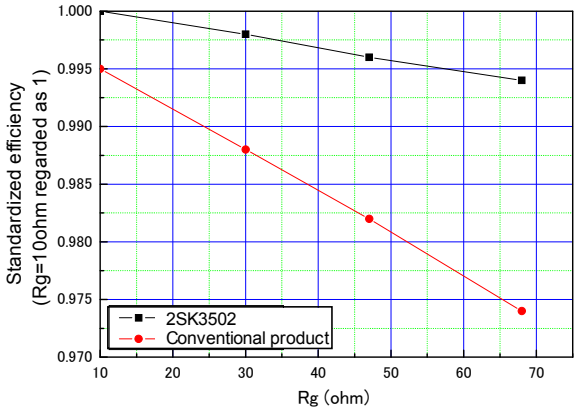


Fig.7-2 Gate resistance and standardized power efficiency

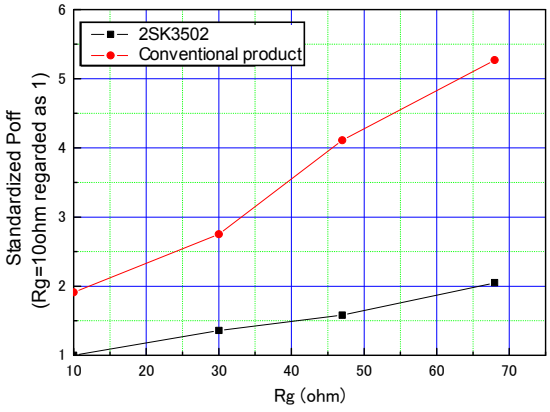


Fig.7-3 Gate resistance and standardized turn OFF dissipation

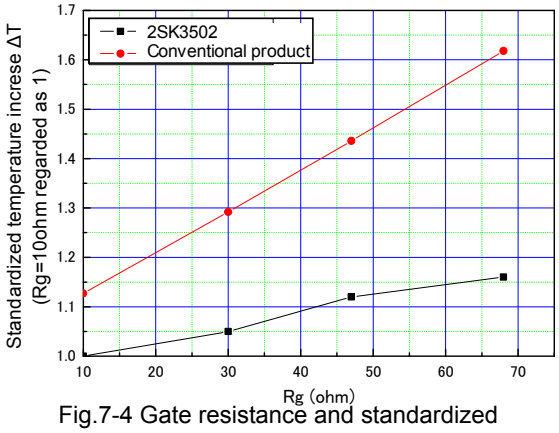


Fig.7-4 Gate resistance and standardized temperature increase

7-3. Cautions for parallel connection

To increase the output capacitance of electronic devices, power devices to be used for the main circuit of the electronic device are connected in parallel in many cases. Generally, the Power MOSFET is easier to be connected in parallel than bipolar transistors. The reason for this is that the operation resistance of the Power MOSFET has a positive temperature coefficient, and that even if unbalance should occur between the current fed through each device connected in series, the positive temperature coefficient offsets the current unbalance. However, if the wiring connecting each MOSFET in parallel is unbalanced, unbalance in current occurs during the transient period of the ON and OFF switching operation, thus resulting in non uniform channel temperature. Cautions in connecting the Power MOSFET in parallel are described below.

(1) Gate parasitic oscillation

If the gate of the MOSFET is directly connected in parallel, parasitic oscillation may occur to the gate and thus resulting in the breakdown of the device. (See 4-4. Breakdown due to parasitic oscillation)

To prevent this from occurring, connect a resistance of 4.7Ω or higher to each gate of the MOSFET connected in parallel.

(2) Circuit wiring

It is desirable that the gate drive and main circuit wiring connecting two or more MOSFETs in parallel be uniform. In particular, the counter electromotive force,

$$V_{ls} = l_s \cdot di/dt ,$$

generated due to the inductance Is contained in the wiring between the main circuit and the source electrode affects the voltage close to the gate-source electrodes of the MOSFET, thus having a large impact on the current balance at the time of turning ON and OFF of the MOSFET.

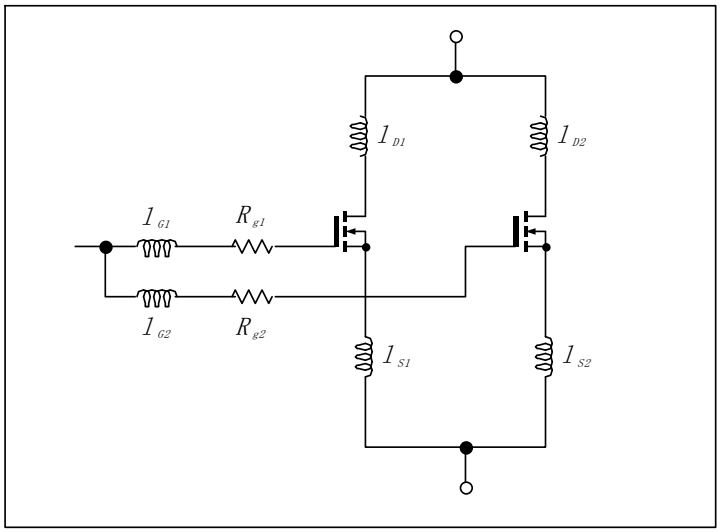


Fig.7-6 Wiring inductance equivalent circuit

Figures 7-7 and 7-8 illustrate the current balance waveforms at the time of turn ON and OFF generated due to the difference between the drain and the source wiring inductance ID and IS of the main circuit (two SuperFAP-Gs rated at 500 V/10 A are used).

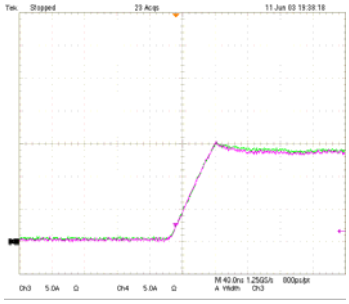
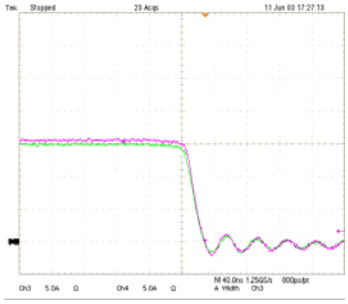
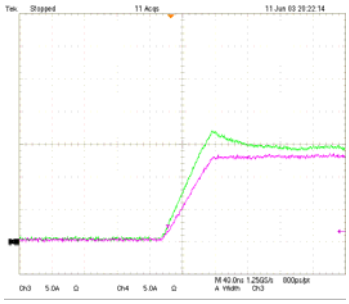
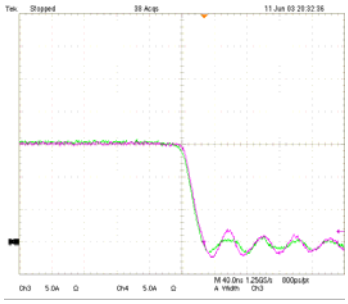
	Turn ON current balance	Turn OFF current balance
ΔLd=6nH		
ΔLd=45nH		

Fig.7-7 When there is a difference in the inductance of the drain electrode wiring of the main circuit

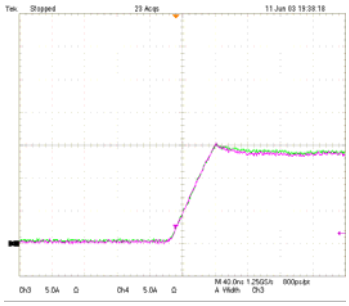
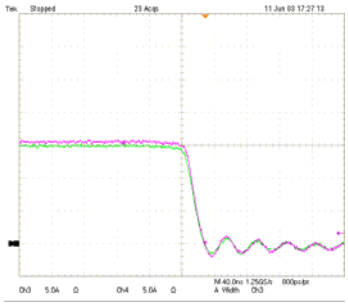
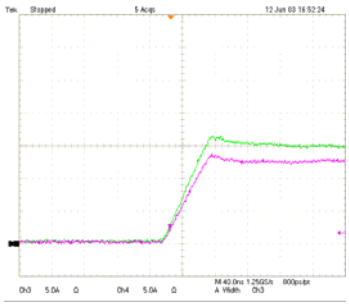
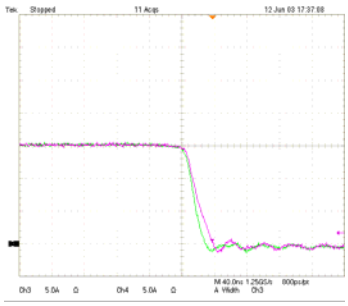
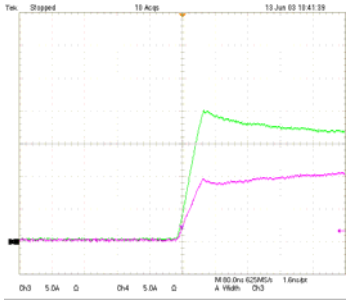
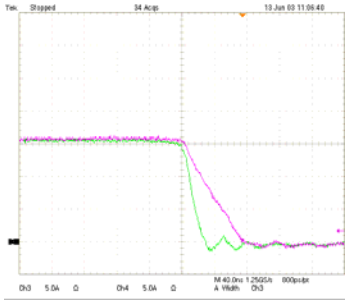
	Turn ON current balance	Turn OFF current balance
ΔLs=2nH		
ΔLs=6nH		
ΔLs=21nH		

Fig.7-8 When there is a difference in the inductance of the source electrode wiring of the main circuit

As shown above, the current balance at the time of turn ON in parallel operation depends largely on the wiring of the source of the main circuit. Consequently, the wiring between the source and the ground should be kept as short and thick as possible to minimize the inductance.

(3) Improving the current unbalance

(a) Characteristics of the MOSFET and current balance

The positive temperature coefficient of the operation resistance of the MOSFET affects the current unbalance generated in parallel operation to be improved at all times.

However, if the MOSFET is used at radiofrequency as in the case of an application to a switching power supply, the unbalance in power dissipation, which may be generated due to the unbalance in transient current at turn ON and OFF, cannot be ignored. As the method for improving this current unbalance, Fuji Power MOSFETs classified into various standard threshold voltage $V_{GS(th)}$ classes are available.

Table 7-1 Standard $V_{GS(th)}$ classification of the SuperFAP series

Series / Rank symbol	SuperFAP series (logic series) Range	SuperFAP series (nonlogic series) Range
C	0.95 V ~ 1.30 V	-
D	1.25 V ~ 1.60 V	-
E	1.55 V ~ 1.90 V	-
F	1.85 V ~ 2.20 V	-
G	2.15 V ~ 2.50 V	-
L	-	2.95 V ~ 3.35 V
M	-	3.30 V ~ 3.70 V
N	-	3.65 V ~ 4.05 V
P	-	4.00 V ~ 4.40 V
R	-	4.35 V ~ 4.75 V
S	-	4.70 V ~ 5.00 V

Note: Ranks cannot be specified.

(b) Drive condition and current balance

As a method for improving the current unbalance at turn OFF, in particular, measures should be taken to keep the switching time as short as possible. Figure 7-9 illustrates the current unbalance at turn ON and turn OFF due to increase/decrease of gate series resistance (500V/10A MOSFET is used).

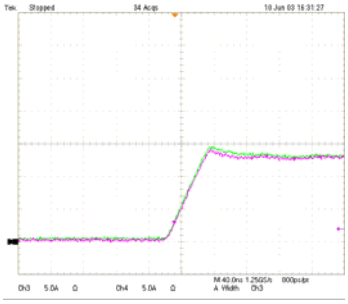
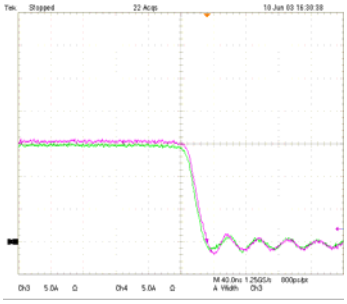
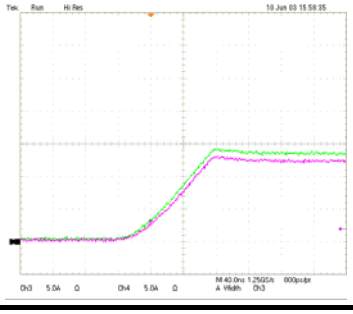
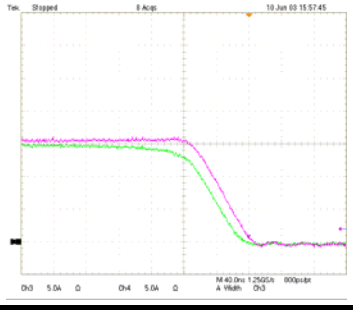
	Turn ON current balance	Turn OFF current balance
Rg=10Ω		
Rg=200Ω		

Fig.7-9 Current balance waveform due to the difference in series gate resistance

7-4. Example of applications

Application	Circuit type	MOSFET Breakdown Voltage BV_{DSS} [V]	○:Planer / ●:SJ-MOS MOSFET On-state Resistance $R_{DS(on)}$ [ohm] Power range [W] ~30	50	100	150	200	300	500	1k	2k	Recommended IC
Standard Power Supply	CRM-PFC	600V		○ 0.85	○ 0.52	○ 0.52	○ 0.38	○ 0.27				FA5590series
	CCM-PFC	600V							● 0.19	● 0.19x2	● 0.11x2	FA5502 FA5610series
	Single Forward	900V		○ 2.5	○ 2.0	○ 1.4	○ 1.0	○ 1.4x2	○ 1.0x2			FA5504/10/14 FA5604
	Double Forward	500V							○ 0.27	● 0.19		-
	Phase-shift Full-Bridge	600V								● 0.38	● 0.19	-
LCD-TV PDP-TV	CRM-PFC CCM-PFC	500V / 600V			○ 0.52	○ 0.38	○ 0.31	● 0.19	● 0.19x2			FA5590series FA5610series
	Current Resonant	500V			○ 1.5	○ 0.85	○ 0.52	○ 0.38				M-Power
	QR	800V		○ 2.0	○ 1.5							FA5571series
Photovoltaic Power Conditioner	Boost-Chopper	600V									● 0.05x2	-
	Full-Bridge	500V									● 0.05x2	-
Adapter (Low Power)	Ringing choke 100V / 110V	600V	○ 2.3									-
	Ringing choke 200V / 220V	900V	○ 4.6									-
Desktop PC / PC server	CCM-PFC	600V				○ 0.4	○ 0.4	● 0.19	● 0.19x2	● 0.19x2		FA5502 FA5610series
	Single Forward	900V				○ 2.0	○ 1.4	○ 1.0				FA5504/10/14 FA5604
	Double Forward	500V						○ 0.52	○ 0.27	● 0.19		-
Note PC-Adapter / IJP / LBP	CRM-PFC	600V			○ 0.52	● 0.38						FA5590series
	Flybuck-PWM	600V	○ 2.3	○ 1.2	○ 0.75	● 0.38						FA5528series FA5592series
	Flybuck-QR	600V	○ 2.3	○ 1.2	○ 0.75	● 0.38						FA5571series
Bus converter	Single Forward	200V		○ 170m	○ 66m	○ 66m	○ 66mx2	○ 66mx2	○ 66mx2			-
	Phase-shift Full-Bridge	100V						○ 10mx8	○ 10mx8			-

* The values in the above table are guidelines. Select your MOSFET after due consideration.