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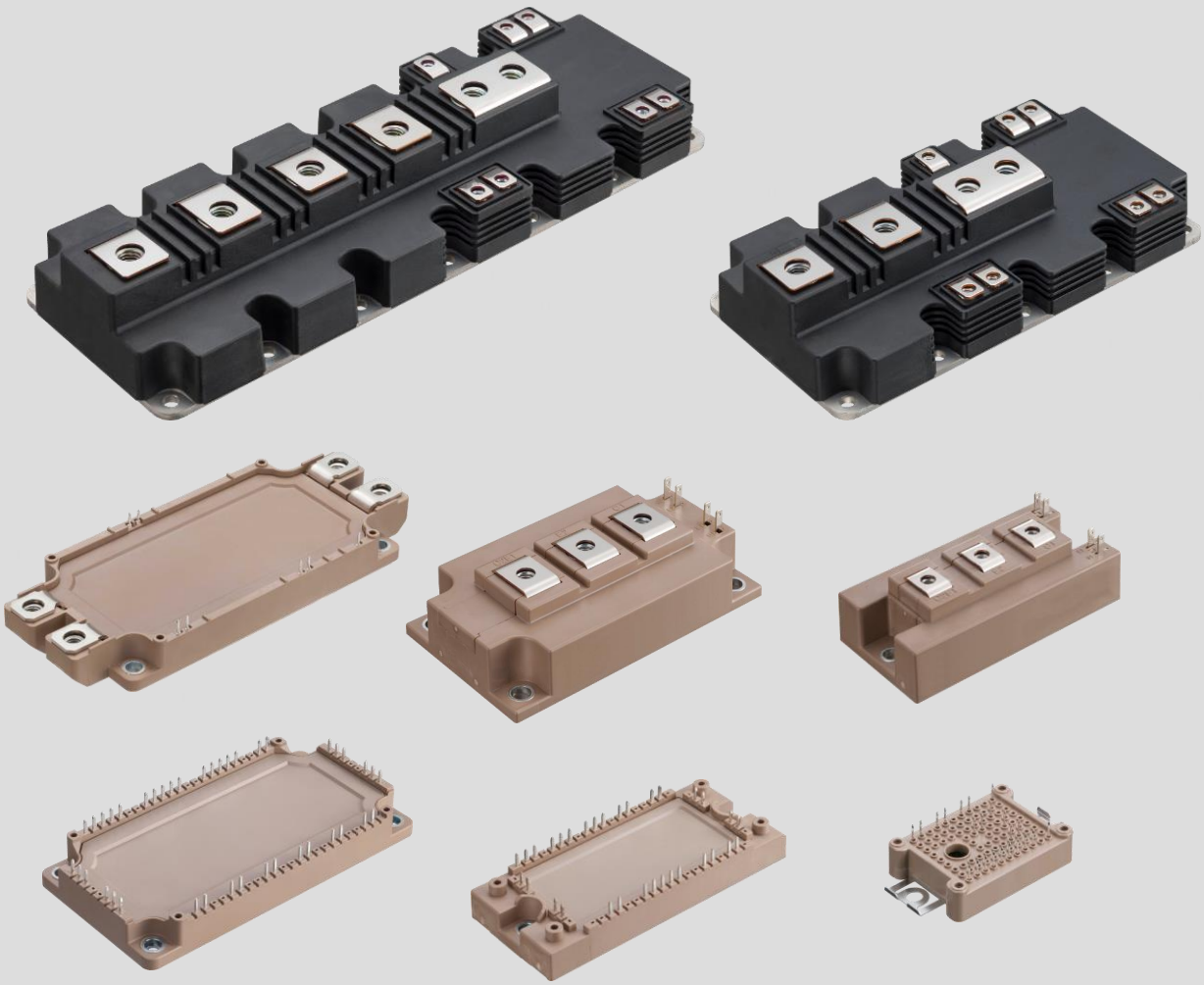

Fuji IGBT Module

Application Manual

March, 2023

Fuji Electric Co., Ltd.

REH984f

⚠ Cautions

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Chapter 7 Gate Drive Circuit Design

This chapter describes about the gate drive circuit design.

1. IGBT Gate Drive Conditions and Main Characteristics

Table 7-1 shows the general relationship between the gate drive conditions and the main characteristics of the IGBT. Since the main characteristics of the IGBT change depending on V_{GE} and R_G, it is necessary to set them according to the design goal of the equipment.

Table 7-1 IGBT drive conditions and main characteristics

Main characteristics	$+V_{GE}$ increase	$-V_{GE}$ increase	$R_{G(ON)}$ increase	$R_{G(OFF)}$ increase
$V_{CE(sat)}$	↓	–	–	–
t_{on} E_{on}	↓	–	↑	–
t_{off} E_{off}	–	↓	–	↑
Turn-on FWD surge voltage	↑	–	↓	–
Turn-off IGBT surge voltage	–	↑	–	↓*1
dv/dt malfunction	↑	↓	↓	↓
Saturation current	↑	–	–	–
Short circuit withstand capability	↓	–	–	–
Radiation noise	↑	–	↓	↓

*1: Gate voltage dependence of surge voltage is different for each series

1.1 Gate forward bias voltage $+V_{GE}$ (On state)

The recommended value for $+V_{GE}$ is +15V. Notes when designing $+V_{GE}$ are shown as follows.

(1) Set $+V_{GE}$ so that it remains below the maximum G-E rated voltage of ±20V.
(2) It is recommended that supply voltage fluctuations are kept within ±10%.
(3) The $V_{CE(sat)}$ is inversely proportional to $+V_{GE}$, so the higher the $+V_{GE}$ the smaller the $V_{CE(sat)}$.
(4) The higher the $+V_{GE}$, the shorter the turn-on switching time (smaller turn-on loss).
(5) The higher the $+V_{GE}$, the larger the opposing arm FWD reverse recovery surge voltage.
(6) Even while the IGBT is in the off-state, there may be malfunction due to dv/dt during FWD reverse recovery, causing pulsed short circuit current to flow and resulting in excessive heat generation. In the worst case, the module might be destroyed. This phenomenon is called a dv/dt shoot-through and is more likely to occur when $+V_{GE}$ is higher.
(7) The higher the $+V_{GE}$, the higher the saturation current.
(8) The higher the $+V_{GE}$, the smaller the short circuit withstand capability.

1.2 Gate reverse bias voltage -V_{GE} (Off state)

The recommended value for $-V_{GE}$ is –5 to -15V. Notes when designing $-V_{GE}$ are shown as follows.

(1) Set $-V_{GE}$ so that it remains below the maximum G-E rated voltage of ±20V.
(2) It is recommended that supply voltage fluctuations are kept within ±10%.
(3) The IGBT turn-off characteristics depend on $-V_{GE}$, especially the characteristics of the part where the collector current I_C begins to turn off strongly depend on $-V_{GE}$. Therefore, the higher the $-V_{GE}$, the shorter the turn-off switching time (smaller turn-off loss).
(4) If $-V_{GE}$ is too small, d*v*/d*t* shoot-through may occur. It is recommended to set $-V_{GE}$ to at least –5V. It is especially important when the gate wiring is long.

1.3 Gate resistance R_G

The R_G listed in the product datasheets is the value that minimizes the switching losses within the absolute maximum ratings under Fuji's measurement environment. Thus, R_G must be changed appropriately according to the circuit and operating conditions. Notes when designing R_G are shown as follows.

(1) The switching characteristics of both turn-on and turn-off are dependent on the value of R_G. The larger the R_G, the longer the switching time and the greater the switching loss. On the other hand, although generally the surge voltage during turn-off switching decreases as R_G increases, surge voltage may increase as R_G increases depending on the device structure. Refer to technical documents for details. Technical documents are available for each IGBT series and voltage rating. .
(2) The larger the R_G, d*v*/d*t* shoot-through is less likely to occur.
(3) Various switching characteristics vary greatly due to stray inductance in the circuit. In particular, the surge voltage during IGBT turn-off and FWD reverse recovery are greatly affected by stray inductance. Therefore, minimize the stray inductance when designing R_G.

Select the most suitable gate drive conditions while paying attention to the above points.

1.4 Countermeasures of d*v*/d*t* induced false turn-on

Fig. 7-1 shows the principle of d*v*/d*t* induced false turn-on. In this figure, it is assumed that IGBT1 transition from off state to on state, and V_{GE} of IGBT2 is reverse biased. In this condition, when IGBT1 turns on, reverse recovery of FWD2 happens. At the same time, the voltage across IGBT2 (FWD2) rises, generating d*v*/d*t* according to the turn-on of IGBT1. Because IGBT1 and IGBT2 have feedback capacitance C_{res}, current $I=C_{res}$ x d*v*/d*t* flows through C_{res}. V_{GE} of IGBT2 rises as this current flows through R_G. When V_{GE} exceeds the sum of the reverse biased voltage and gate threshold voltage $V_{GE(th)}$ of IGBT2, IGBT2 is turned on, resulting in short circuit of IGBT1 and IGBT2.

Based on this principle, countermeasures are shown in Fig. 7-2. There are three methods, which are (a) adding C_{GE} to suppress the transient rise of V_{GE}, (b) increase $-V_{GE}$ to lower the transient peak value of V_{GE}, and (c) increase R_G to lower d*v*/d*t*. The effectiveness of these countermeasures vary depending on the gate drive circuit, thus be sure to evaluate them thoroughly. Note that these countermeasures also affect switching loss, so be sure to consider this as well.

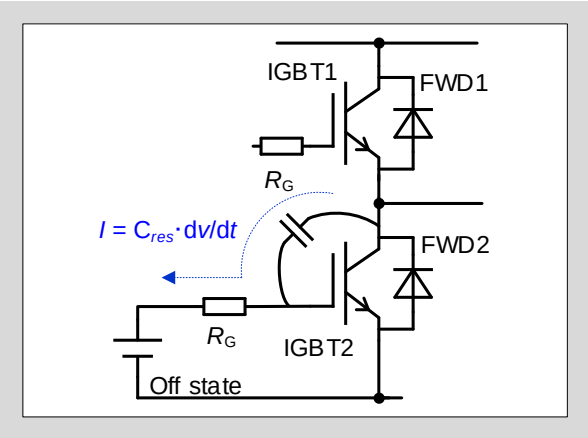

Fig. 7-1 Principle of d*v*/d*t* induced false turn-on

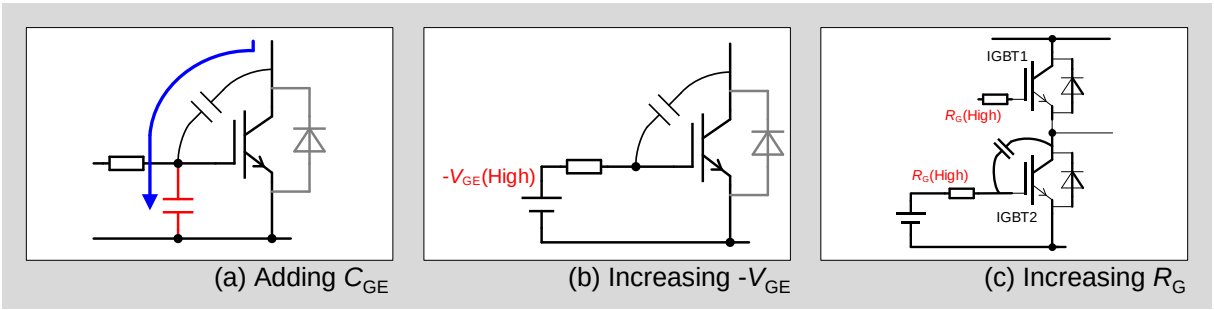

Fig. 7-2 Countermeasures against d*v*/d*t* induced false turn-on

The aim of adding C_{GE} is to reduce the current flowing through R_G by bypassing to C_{GE}. However, by adding C_{GE}, it is necessary to charge this C_{GE} when driving the gate, which reduces the switching speed and increase the switching loss. This can be adjusted by lowering the R_G value. In other words, by selecting an appropriate combination of C_{GE} and R_G, it is possible to avoid d*v*/d*t* induced false turn-on without increasing switching loss. As a guideline, the recommended C_{GE} value is about twice the C_{ies} value shown in the datasheet, and the recommended R_G value is about half the value before adding C_{GE}. Connect C_{GE} as close as possible to the G-E terminals. Confirm the selection of C_{GE} and R_G by actual evaluation.

2. Drive Current

Since IGBT has a MOS gate structure, drive current is needed to charge and discharge this gate during switching. Fig. 7-3 shows the gate charge (dynamic input) characteristics. The gate charge characteristics show the amount of charge required to drive the IGBT and can be used to calculate the average drive current and drive power. Fig. 7-4 shows the gate drive circuit schematic, as well as the gate voltage V_{GE} and drive current I_G waveforms. The principle of the gate drive circuit is to switch alternately between the forward bias and reverse bias power supply using switch S_1 and S_2. During switching, the drive current is used to charge and discharge the gate. The area (shaded) under the drive current waveform in Fig. 7-4 is equal to the gate charge shown in Fig. 7-3.

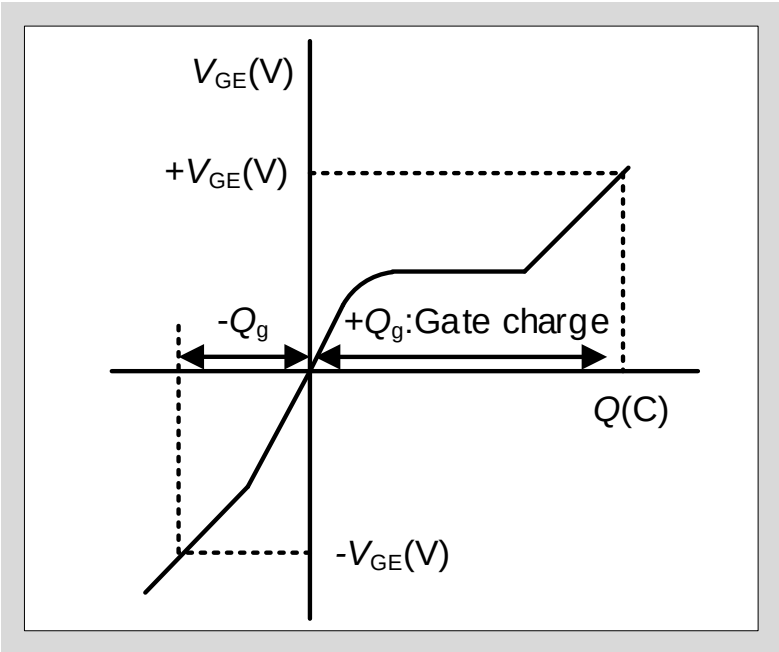

Fig. 7-3 Gate charge (Dynamic input) characteristics

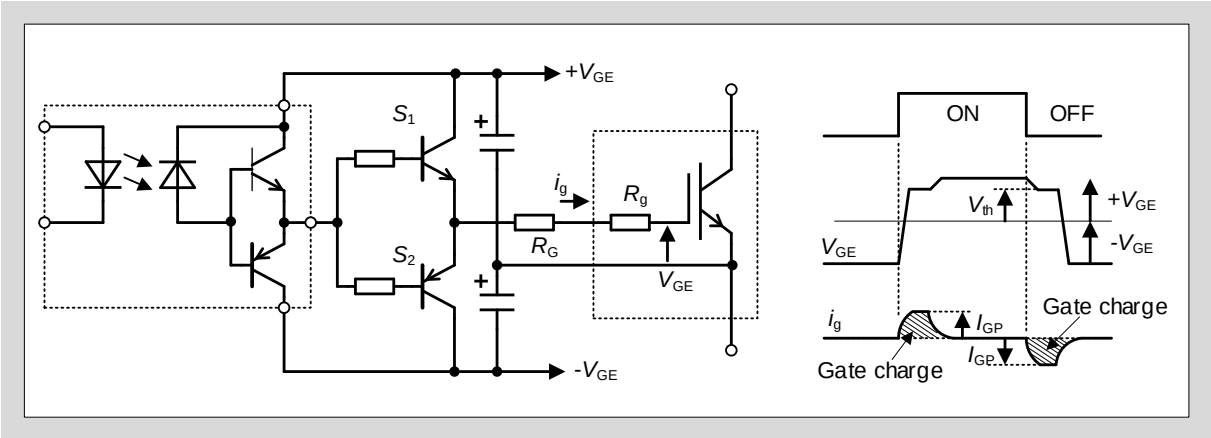

Fig. 7-4 Gate drive circuit schematic and waveforms

The drive current peak value I_{GP} can be approximately calculated as follows.

$$I_{GP} = \frac{+V_{GE} + |-V_{GE}|}{R_G + r_g}$$

$+V_{GE}$:Forward bias supply voltage
$-V_{GE}$:Reverse bias supply voltage
R_G :Gate resistance
r_g :Module internal gate resistance

Internal gate resistance r_g differs for each product. Thus, refer to the datasheet of each product.

On the other hand, the average value of the drive current I_G can be calculated by the following formula using the gate charge characteristics (Fig.7-3).

$$+I_G = -I_G = f_C \cdot \left(|+Q_g| + |-Q_g|\right)$$

f_c :Switching frequency
$+Q_g$:Gate charge from 0V to $+V_{GE}$
$-Q_G$:Gate charge from $-V_{GE}$ to 0V

Furthermore, if all the power loss of the gate drive circuit is consumed by R_G, the drive power P_d required to drive the IGBT is shown by the following formula.

$$P_{d(on)} = f_C \cdot \left[\frac{1}{2}\left(|+Q_g| + |-Q_g|\right) \cdot \left(|+V_{GE}| + |-V_{GE}|\right)\right]$$

$$P_{d(off)} = P_{d(on)}$$

$$P_d = P_{d(off)} + P_{d(on)}$$

$$= f_C \cdot \left(|+Q_g| + |-Q_g|\right) \cdot \left(|+V_{GE}| + |-V_{GE}|\right)$$

Therefore, it is necessary to select R_G with proper power rating according to P_d.

Be sure to design the gate drive circuit so that the above-mentioned drive current and drive power can be properly supplied.

3. Setting Dead time

In inverter circuits, etc., it is necessary to set an on-off timing delay (dead time) in order to prevent short circuits between the upper and lower arms. As shown in Fig. 7-5, both the upper and lower arms are in the off state during the dead time.

Basically, the dead time needs to be set longer than the IGBT switching time ($t_{off\ max}$.). For example, if R_G is increased, switching time also becomes longer, so the dead time must be increased as well. Also, it is necessary to consider other drive conditions and temperature characteristics. If the dead time is too short, short circuit between the upper and lower arms may occur, and the heat generated by the short circuit current may destroy the module. A dead time of 3μsec or more is recommended for IGBT modules. Check if the dead time is sufficient by doing actual evaluation.

One method of determining whether the dead time setting is sufficient is to check the current in the DC power line at no load condition.

In the case of a 3-phase inverter, set the inverter outputs (U, V, W) to open, apply normal input signals, and measure the DC power line current as shown in Fig. 7-6. Even if the dead time is sufficient, a very small pulse current (d*v*/d*t* current through the device output capacitance: about 5% of the rated current) will be observed. However, if the dead time is insufficient, a large short circuit current will be observed. In this case, increase the dead time until the short circuit current disappears. It is recommended to perform this test at high temperature as the turn-off time is longer. Short circuit current also increases if the gate reverse bias voltage $-V_{GE}$ is insufficient (refer to Chapter 4, section 3.3). Increase $-V_{GE}$ if increasing the dead time does not reduce the short circuit current. $-V_{GE}$ of 5V and above is recommended.

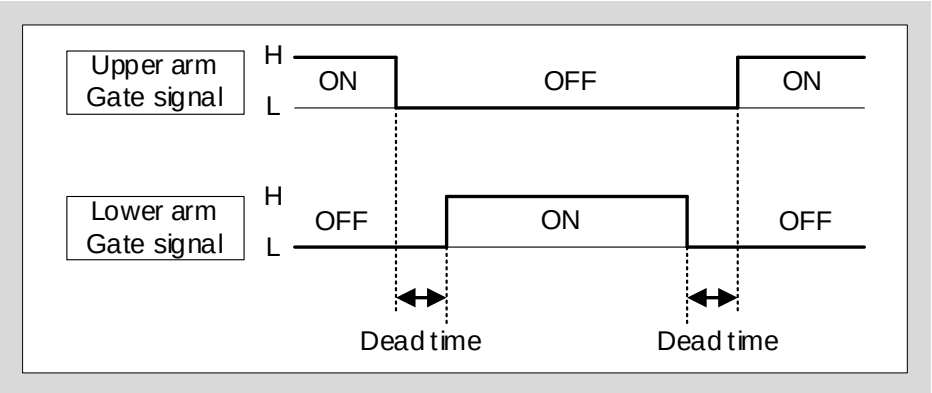

Fig. 7-5 Dead time timing chart

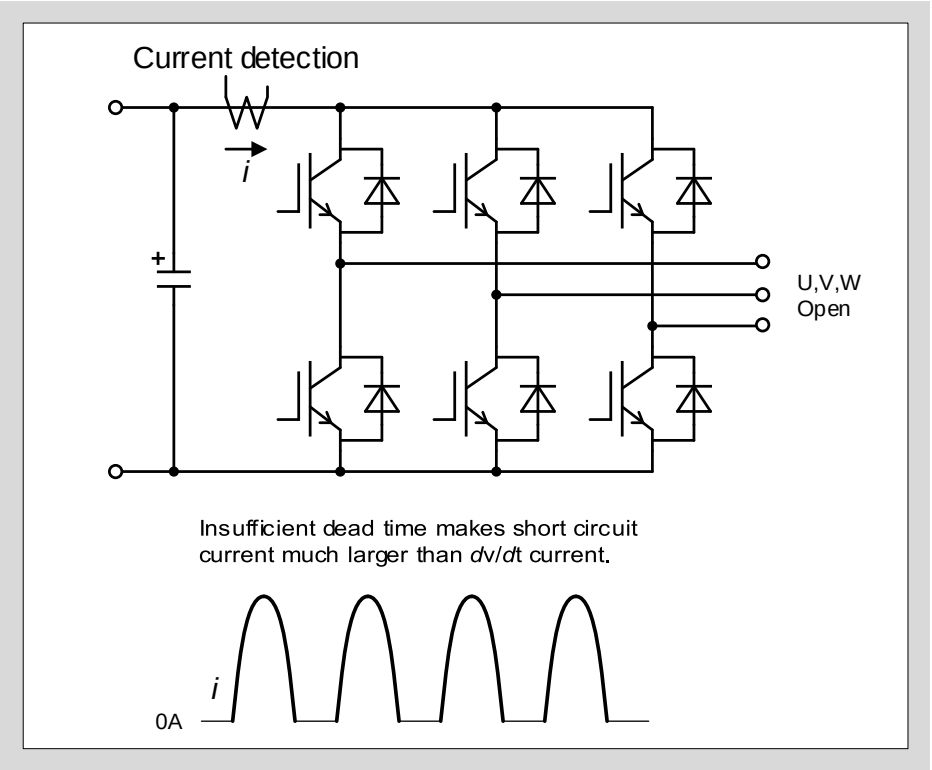

Fig. 7-6 Method for detecting short circuit current due to insufficient dead time

4. Example of Gate Drive Circuits

In inverter circuits, etc., it is necessary to electrically isolate the main circuit and the control circuit. Fig. 7-7 shows an example of a gate drive circuit using high speed optocoupler. By using optocoupler, the input signal and the module are electrically isolated from each other. Also, since optocouplers do not limit the output pulse width, they are suitable for applications where the signal pulse width varies over a wide range, such as PWM control, and is the most widely used.

In addition, turn-on and turn-off gate resistors can be used separately.

Furthermore, there is also a signal isolation method using a pulse transformer. This method can simplify the circuit because both the signal as well as the gate drive power can be supplied simultaneously from the signal side. However, this method have limitations such as a maximum duty ratio of 50%, and reverse bias cannot be set.

Recently, gate drive units (GDUs) that use pulse transformer are available in the market. Refer to the website of each GDU manufacturer for details.

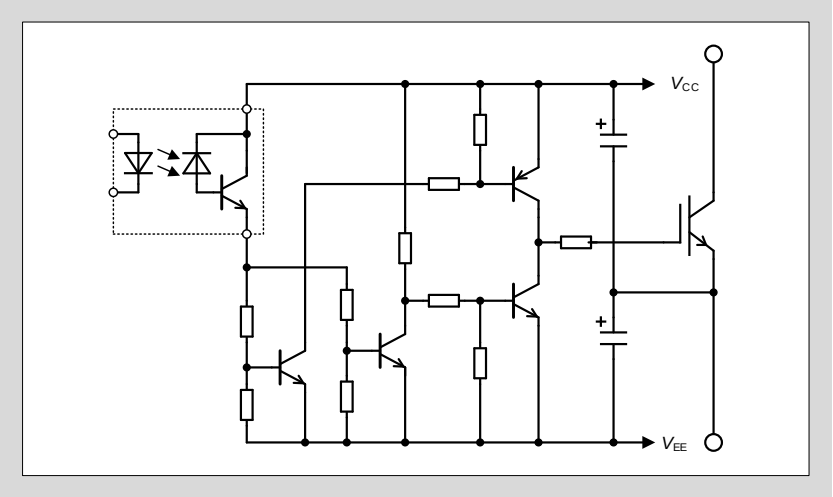

Fig. 7-7 Example of gate drive circuit using high speed optocoupler

5. Precautions for Gate Drive Circuit Design

5.1 Optocoupler noise ruggedness

As IGBTs are high speed switching devices, it is necessary to select optocoupler for gate drive circuit that has high noise ruggedness (e.g. HCPL4504). Also, to prevent malfunctions, make sure that the wiring from the optocoupler primary side and secondary side do not cross. Furthermore, in order to make full use of the IGBT high speed switching capability, using optocoupler with a short signal transmission delay is recommended.

5.2 Wiring between gate drive circuit and IGBT

If the wiring between the gate drive circuit and the IGBT is long, the IGBT may malfunction due to gate signal oscillation or induced noise. There are the following countermeasures.

(1) Make the gate drive circuit wiring as short as possible, and use twisted pair wires for the gate and emitter wiring.
(2) Increase R_G. However, pay attention to the increase of switching time and switching loss.
(3) Separate the gate drive circuit and main circuit wiring as far as possible. If the wirings overlap, design the layout so that they cross each other (in order to avoid mutual induction).
(4) Do not bundle the gate wiring or other phases together.

*1 About R_{GE}

The IGBT may be destroyed if voltage is applied to the main circuit when the gate drive circuit is malfunctioned or not fully operating (gate in open state). In order to prevent this, it is recommended to connect a resistor R_{GE} of about 10kΩ between G-E (refer to Fig. 7-8).

When powering up, first turn on the gate drive circuit power supply. Switch on the main circuit power supply when the gate drive circuit is fully operational.

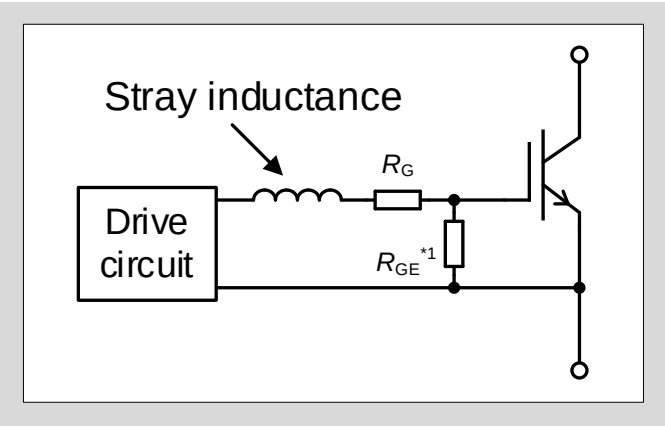

Fig. 7-8 Precautions for gate drive circuit design

5.3 Gate overvoltage protection

It is necessary that IGBT modules, like other MOS devices, are sufficiently protected against static electricity. The G-E absolute maximum rated voltage is ±20V. If there is a possibility that a voltage exceeding this may be applied to G-E, protective measures such as connecting Zenner diode between G-E are required as shown in Fig. 7-9.

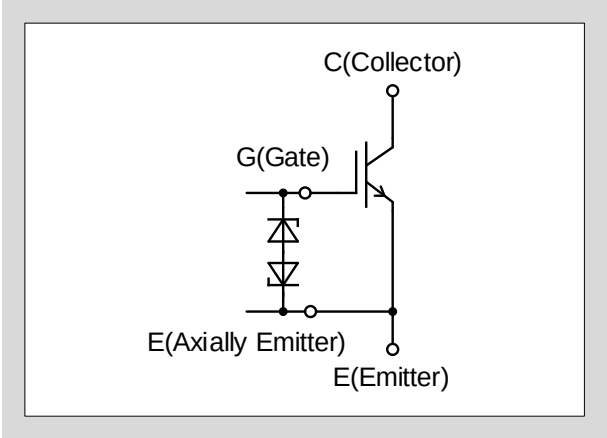

Fig. 7-9 G-E overvoltage protection circuit example