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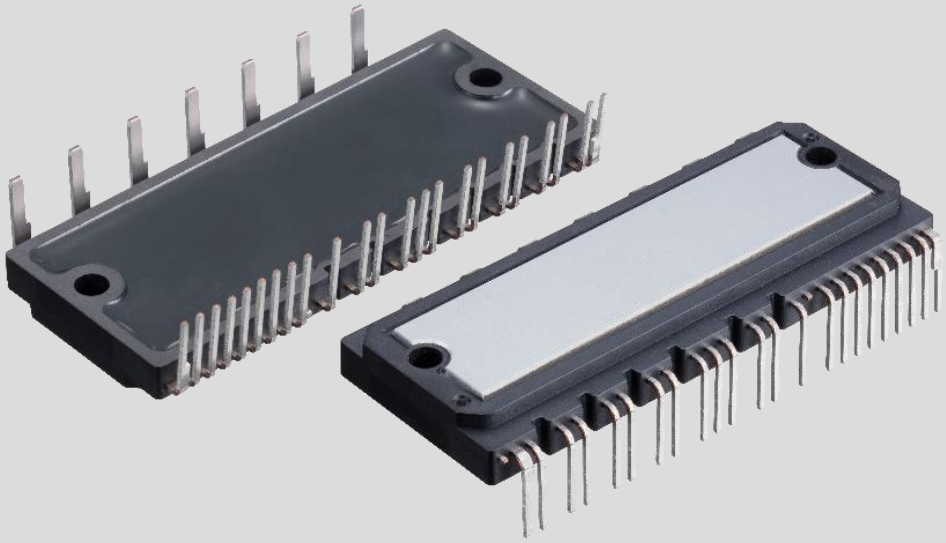

Small IPM (Intelligent Power Module)
P642 Series
6MBP**XT*065-50

Application Manual

April 2024

Fuji Electric Co., Ltd.

MT6M15234 c

Cautions

This Instruction contains the product specifications, characteristics, data, materials, and structures as of April 2024. The contents are subject to change without notice for specification changes or other reason. When using a product listed in this Instruction be sure to obtain the latest specifications.

The application examples in this note show the typical examples of using Fuji products and this note shall neither assure to enforce the industrial property including some other rights nor grant the license.

Although Fuji Electric Co., Ltd. continually strives to enhance product quality and reliability, a small percentage of semiconductor products may become faulty. When using Fuji Electric semiconductor products in your equipment, be sure to take adequate safety measures such as redundant, flame-retardant and fail-safe design in order to prevent a semiconductor product failure from leading to a physical injury, property damage or other problems.

The products described in this application manual are manufactured with the intention of being used in the following industrial electronic and electrical devices that require normal reliability.

- Compressor motor inverter
- Fan motor inverter for room air conditioner
- Compressor motor inverter for heat pump applications, etc.

If you need to use a semiconductor product in this application note for equipment requiring higher reliability than normal, such as listed below, be sure to contact Fuji Electric Co., Ltd. to obtain prior approval. When using these products, take adequate safety measures such as a backup system to prevent the equipment from malfunctioning when a Fuji Electric's product incorporated in the equipment becomes faulty.

- Transportation equipment (mounted on vehicles and ships)
- Trunk communications equipment
- Traffic-signal control equipment
- Gas leakage detectors with an auto-shutoff function
- Disaster prevention / security equipment
- Safety devices, etc.

Do not use a product in this application note for equipment requiring extremely high reliability such as:

- Space equipment
- Airborne equipment
- Atomic control equipment
- Submarine relaying equipment
- Medical equipment

If you have any question about any portion of this application note, ask Fuji Electric Co., Ltd. or its sales agencies. Neither Fuji Electric Co., Ltd. nor its agencies shall be liable for any injury or damage caused by any use of the products not in accordance with instructions set forth herein.

Chapter 3 Details of Control & Protection Functions

1. Control Power Supply, VCCH(U,V,W), VCCL, COM

<Voltage range of control power supply VCCH(U,V,W), VCCL >

- For control supply voltage, please connect a 15V±10% DC power supply between VCCH(U), VCCH(V), VCCH(W), VCCL and COM terminals.
- Table 3-1 describes the operation of the product for various control supply voltages. A low impedance capacitor and a high frequency decoupling capacitor should be connected close to the terminals of the power supply.
- High frequency noise on the power supply might cause malfunction of the internal control IC or erroneous fault signal output. To avoid these problems, the maximum amplitude of voltage ripple on the power supply should be less than ±1V/μs.
- When connecting external shunt resistor, the potential at the COM terminal is different from that at the N(U, V, W) terminal. Please refer all control circuits and power supplies to the COM terminal and not to the N(U, V, W) terminals. If circuits are improperly connected, current might flow through the shunt resistor and cause improper operation of the short-circuit protection function. In general, it is recommended to set the COM terminal as the ground potential in the PCB layout.
- The control power supply is also connected to the bootstrap circuit which provide floating power supplies for the high-side gate drivers.
- When high-side control power supply voltage $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ falls below $V_{CCH(OFF)}$, only the IGBT which UV protection is triggered is turned-off regardless of input signal condition.
- When low-side control power supply voltage V_{CCL} falls below $V_{CCL(OFF)}$, all low-side IGBTs are turned-off regardless of input signal condition.

Table 3-1 Functions versus supply voltage $V_{CCH(U,V,W)}$, V_{CCL}

Control Voltage Range [V]	Operating state
0 ~ 4	The product does not operate. UV protection and fault output are not activated. d*v*/d*t* noise on the main P-N power supply might cause the IGBTs to malfunction.
4 ~ 13	The product starts to operate. UV protection is activated, control input signals are blocked and fault output is generated.
13 ~ 13.5	UV protection is reset. IGBTs perform switching in accordance to input signal. Drive voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition. High-side IGBTs do not switch until $V_{B(*)}$*1 reaches $V_{B(ON)}$ after initial charging.
13.5 ~ 16.5	Normal operation. This is the recommended operating condition.
16.5 ~ 20	IGBTs perform switching. Because drive voltage is above the recommended range, IGBT's switching is faster and causes an increase in system noise. Even with proper overcurrent protection design, the short-circuit peak current can become very large and might lead to failure.
Over 20	Control circuit in the product might be damaged. It is recommended to insert a Zener diode between each pair of control supply terminals if necessary.

*1 : $V_{B(*)}$ is applied between VB(U)-U, VB(V)-V, VB(W)-W.

<Under voltage (UV) protection of control power supply $V_{CCH(U,V,W)}$, V_{CCL}>

- Fig.3-1 shows the UV protection circuit of VCCH(U,V,W) and VCCL.
- Fig.3-2 and Fig.3-3 shows the operation sequence of UV operation of VCCH and VCCL.
- As shown in Fig.3-1, a diode is connected between VCCH(U,V,W)-COM and VCCL-COM terminals. The diode is connected to protect the product from the input surge voltage. Do not use the diode for voltage clamp purpose otherwise the product might be damaged.

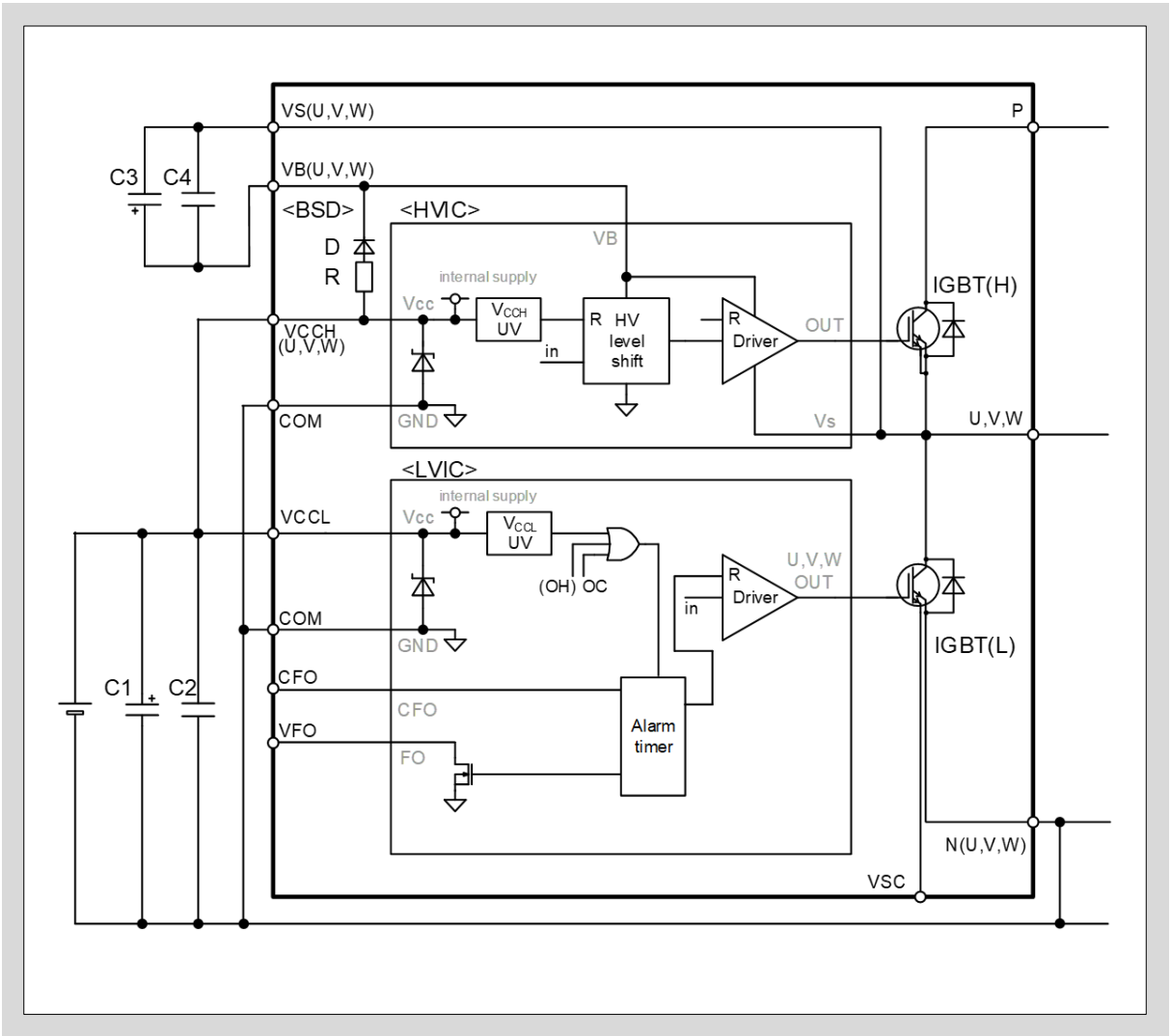

Fig. 3-1 UV protection circuit of high-side and low-side control power supply

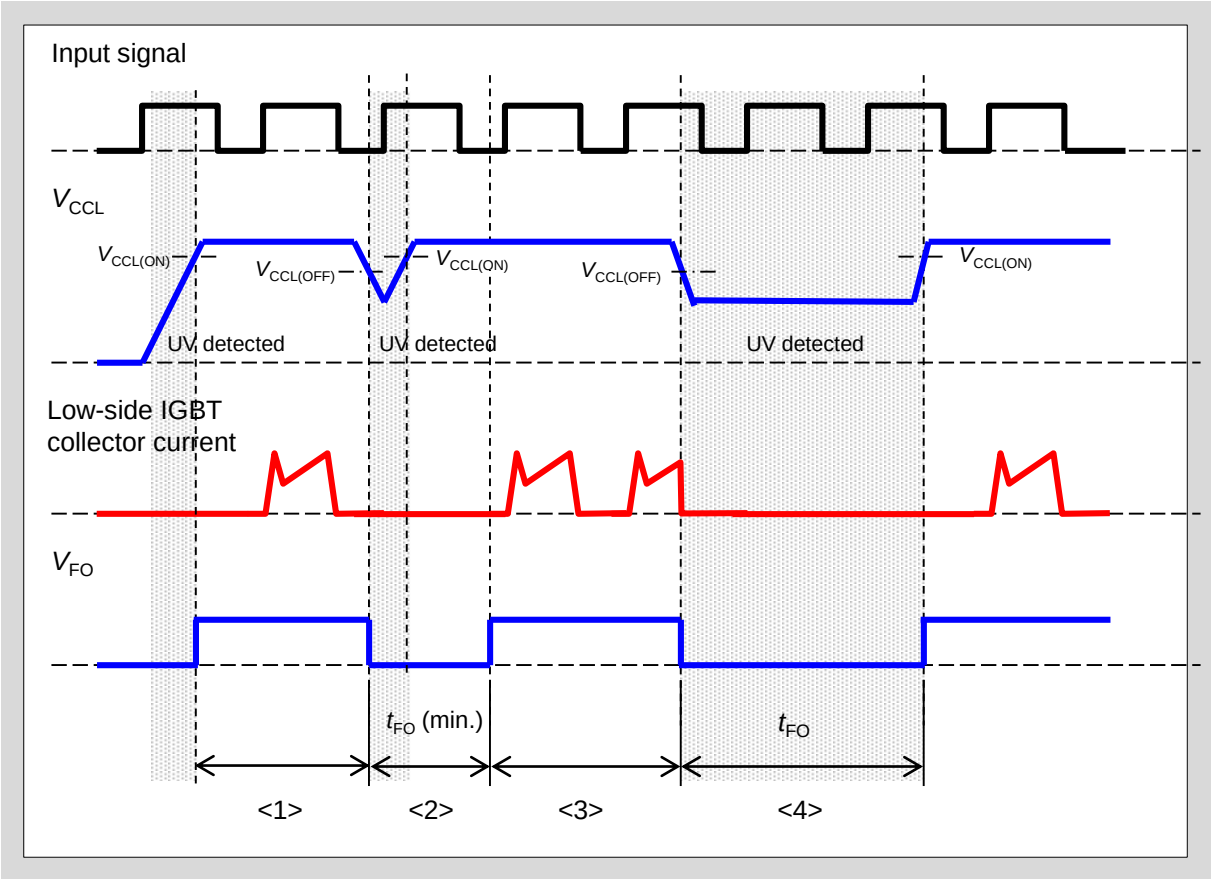

Fig. 3-2 UV protection operation sequence of V_{CCL}

When V_{CCL} is below 4V, UV and fault output are not activated.

<1> When V_{CCL} is lower than $V_{CCL(ON)}$, all lower side IGBTs are OFF state. After V_{CCL} exceeding $V_{CCL(on)}$, the fault output V_{FO} is released (high level). And the LVIC stars to operate, then next input is activated.

<2> The fault output V_{FO} is activated when V_{CCL} falls below $V_{CCL(OFF)}$, and all lower side IGBT remains OFF state. If the voltage drop time is less than $t_{FO(min)}$, the minimum pulse width of the fault output signal is $t_{FO(min)}$ and all lower side IGBTs are OFF state regardless of the input signal condition.

<3> UV protection is reset after t_{FO} and V_{CCL} exceeding $V_{CCL(ON)}$, then the fault output V_{FO} is reset simultaneously. After that the LVIC starts to operate from the next input signal.

<4> When the voltage drop time is more than t_{FO}, the fault output pulse width is generated and all lower side IGBTs are OFF state regardless of the input signal condition during the same time.

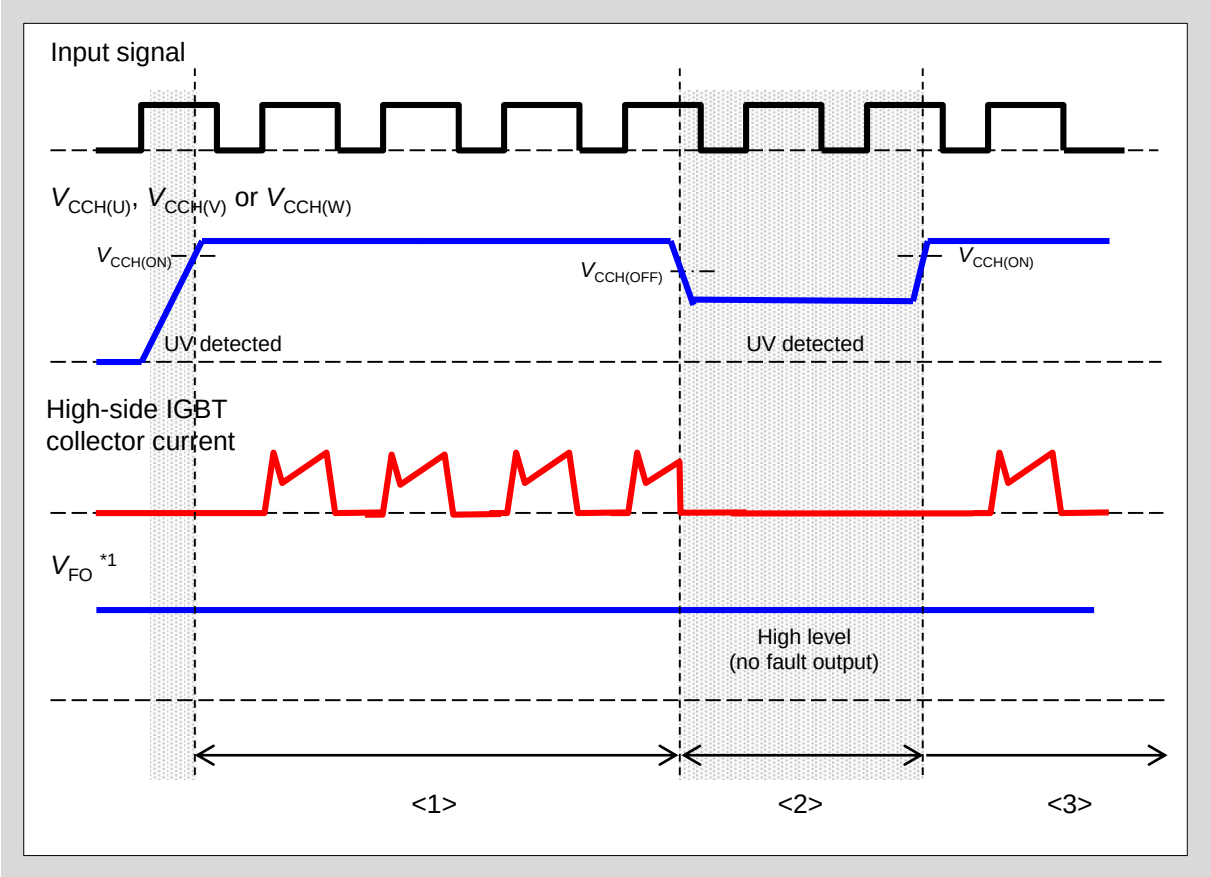

Fig. 3-3 UV protection operation sequence of $V_{CCH(U,V,W)}$

<1> When $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ is lower than $V_{CCH(ON)}$, the upper side IGBT is OFF state. After $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ exceeds $V_{CCH(ON)}$, the HVIC starts to operate from the next input signals. The fault output V_{FO} is constant (high level) regardless of $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$. *1

<2> After $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ falls below $V_{CCH(OFF)}$, the upper side IGBT remains OFF state. But the fault output VFO keeps high level.

<3> The HVIC starts to operate from the next input signal after UV is reset.

*1 : The fault output does not depend on the bias condition of the HVIC.

2. Power Supply Terminals of High-Side VB(U,V,W), VS(U,V,W)

<Voltage range of high-side bias voltage for IGBT driving terminals $V_{B(*)}$>

- The $V_{B(*)}$ voltage, which is the voltage difference between VB(U,V,W) and VS(U,V,W), provides the power supply to the HVICs within the product. This power supply must be in the range of 13.0~18.5V to ensure that the HVICs can fully drive the high-side IGBTs.
- The product includes UV protection for $V_{B(*)}$ to ensure that the HVICs do not drive the high-side IGBTs when $V_{B(*)}$ drops below a specified voltage.
- This function prevents the IGBT from operating in a high dissipation mode. Please note that the UV protection only works on the triggered phase and doesn't generate fault output.
- Conventionally, three isolated power supplies are necessary for IGBT drive at the high-side. In case of using bootstrap circuit, the IGBT drive power supply for high-side can be generated from the high-side/low-side control power supply.
- The power supply of the high-side is charged when the low-side IGBT is turned on or when freewheel current flows through the low-side FWD. Table 3-2 describes the operation of the product for various control supply voltages. The control supply should be well filtered with a low impedance capacitor and a high frequency decoupling capacitor connected close to the terminals in order to prevent malfunction of the internal control IC caused by a high frequency noise on the power supply.
- When $V_{B(*)}$ falls below $V_{B(OFF)}$, only the triggered phase IGBT is off-state even though the input signal is provided.

Table 3-2 Functions versus high side bias voltage for IGBT driving $V_{B(*)}$

Control Voltage Range [V]	Operations and functions
0 ~ 4	HVICs are not activated. UV does not operate. d*v*/d*t* noise on the main P-N power supply might cause the IGBTs to malfunction.
4 ~ 12.5	HVICs start to operate. As the UV is activated, control input signals are blocked.
12.5 ~ 13	UV is reset. The high-side IGBTs perform switching in accordance to input signal. Driving voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition.
13 ~ 18.5	Normal operation. This is the recommended operating condition.
18.5 ~ 20	The high-side IGBTs perform switching. Because drive voltage is above the recommended range, IGBT's switching is faster and causes an increase in system noise. Even with proper overcurrent protection design, the short-circuit peak current can become very large and might lead to failure.
Over 20	Control circuit in the product might be damaged. It is recommended to insert a Zener diode between each pair of high-side power supply terminals.

<Under voltage (UV) protection of high-side bias voltage $V_{B(*)}$>

- Fig.3-4 shows the UV protection circuit of high-side bias voltage $V_{B(*)}$.
- Fig.3-5 shows the UV protection operation sequence of $V_{B(*)}$.
- As shown in Fig.3-4, diodes are connected to the VB(U,V,W), VS(U,V,W) and VB(U,V,W)-COM terminals. These diodes protect the product from input surge voltage. Do not use these diodes for voltage clamp purpose otherwise the product might be damaged.

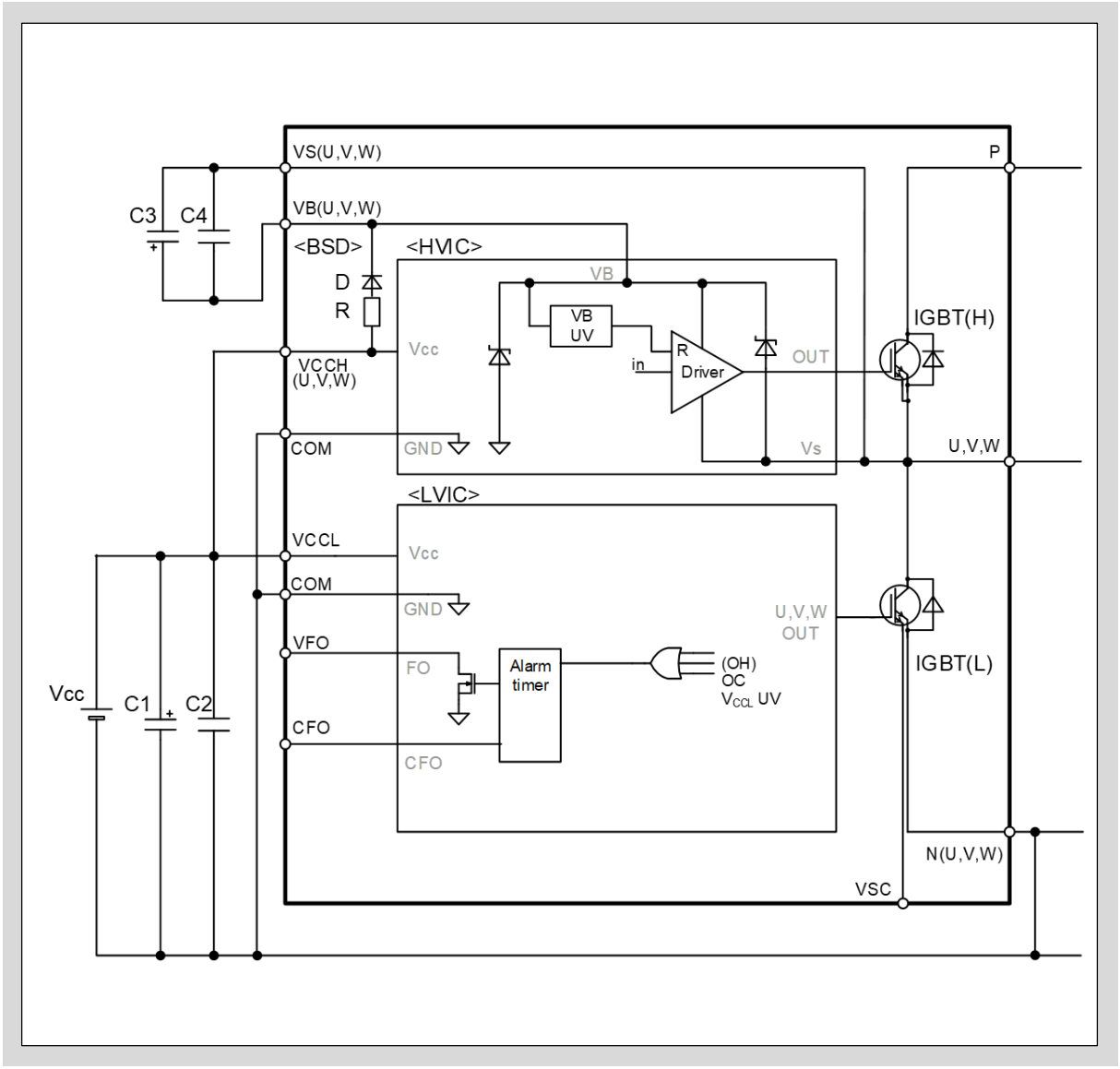

Fig. 3-4 UV protection circuit of high-side bias voltage

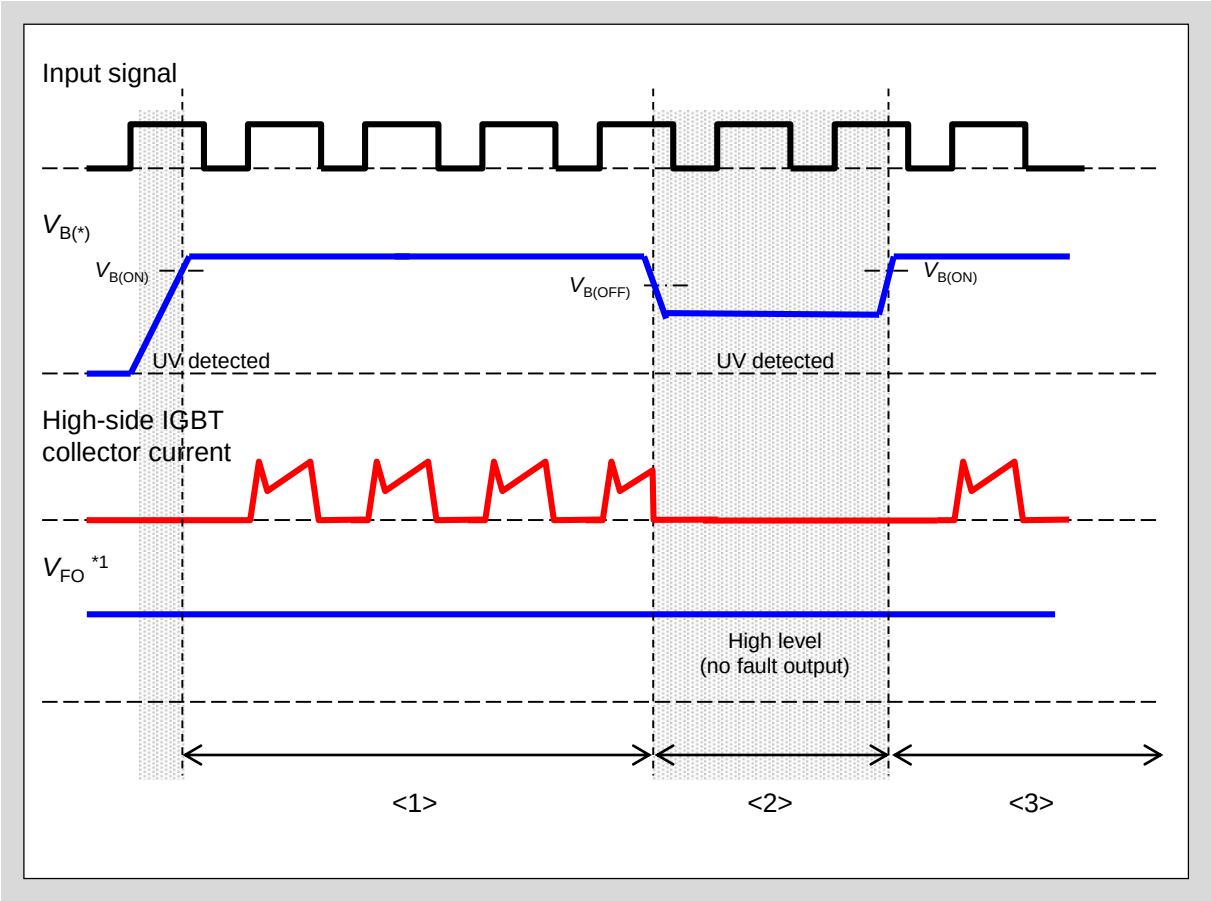

Fig. 3-5 UV protection operation sequence of $V_{B(*)}$

<1> When $V_{B(U)}$, $V_{B(V)}$ or $V_{B(W)}$ is below $V_{B(ON)}$, the corresponding high-side IGBT is OFF.
When $V_{B(*)}$ exceeds $V_{B(ON)}$, HVIC starts switching operation from the next input signal.
The fault output voltage V_{FO} is H level regardless of $V_{B(*)}$. *1

<2> When $V_{B(U)}$, $V_{B(V)}$ or $V_{B(W)}$ falls below $V_{B(OFF)}$, the corresponding high-side IGBT is turned off.
The fault output voltage V_{FO} remains at H level.

<3> After UV protection is reset, HVIC restarts switching operation from the next input signal.

*1 : The fault output does not depend on the bias condition of the HVIC.

3. Function of Built-in BSDs (Bootstrap Diodes)

There are several ways to generate high-side bias voltage $V_{B(*)}$ (VB(U)-VS(U), VB(V)-VS(V), VB(W)-VS(W) voltage). This product can configure a bootstrap circuit by using the built-in BSDs. When configuring the bootstrap circuit, it is necessary to set the duty ratio and on-time according to the bootstrap capacitor and the charging operation conditions.

<Bootstrap circuit operation>

When low-side IGBT is ON, the high-side bias voltage $V_{B(*)}(t1)$ from the charging operation of the bootstrap capacitor can C3 be expressed by the following equations. Fig.3-6 shows the circuit diagram of charging operation, and Fig.3-7 shows the timing chart.

$V_{B(*)}(t1) = V_{CC}-V_{F(D)}-V_{CE(sat)}-I_B \cdot R$ …… transient state
$V_{B(*)}(t1) \approx V_{CC}$ …….. steady state
$V_{F(D)}$: Forward voltage of BSD
$V_{CE(sat)}$: Saturation voltage of low-side IGBT
R : Bootstrap circuit resistance
I_B : Charging current of bootstrap circuit

When low-side IGBT is turned off, the motor current flows to the high-side FWD. When the V_S potential rises above V_{CC}, the charging of C3 stops, and $V_{B(*)}$ gradually decreases due to current consumption by the high-side control power supply.

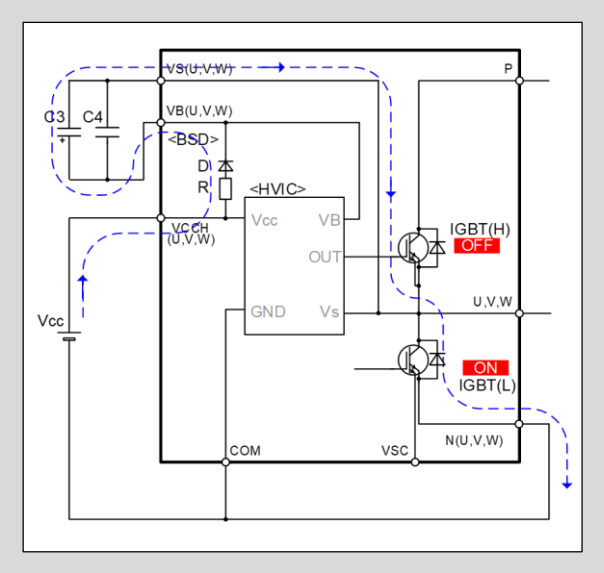

Fig. 3-6 Circuit diagram of charging operation when low-side IGBT is ON

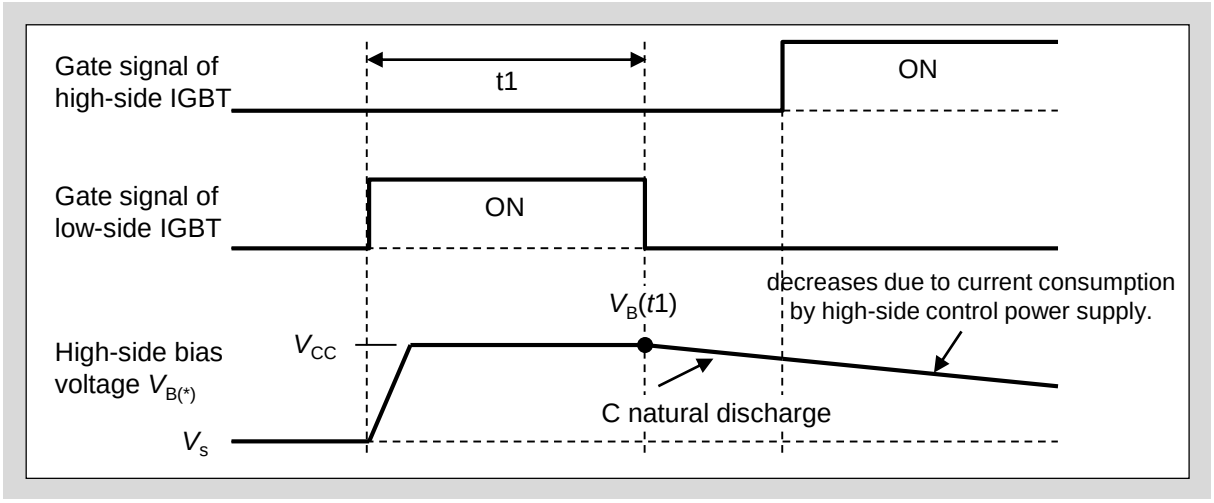

Fig. 3-7 Timing chart of charging operation when low-side IGBT is ON

When low-side IGBT is OFF and low-side FWD is ON, freewheel current flows through the low-side FWD. The high-side bias voltage $V_{B(*)}(t2)$ from the charging operation of the bootstrap capacitor can be expressed by the following equations. Fig.3-8 shows the circuit diagram of charging operation, Fig.3-9 shows the timing chart, and $V_{B(*)}(t2)$ can be expressed by the following equations

$V_{B(*)}(t2) = V_{CC}-V_{F(D)}+V_{F(FWD)}-I_B \cdot R$ … transient state
$V_{B(*)}(t2) \approx V_{CC}$ … steady state

$V_{F(D)}$: Forward voltage of BS
$V_{F(FWD)}$: Forward voltage of low-side FWD
R : Bootstrap circuit resistance
I_B : Charging current of bootstrap circuit

When both the low-side and high-side IGBTs are OFF, the regenerative current flows through the low-side FWD. Therefore, the V_S potential drops to $-V_F$ of FWD, and the bootstrap capacitor is recharged. When the high-side IGBT is turned on and the V_S potential rises above V_{CC}, the charging of C3 stops, and $V_{B(*)}$ gradually decreases due to current consumption by the high-side control power supply.

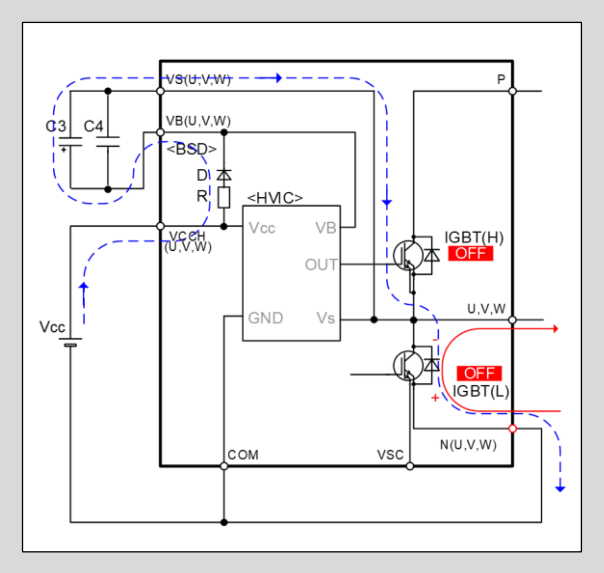

Fig. 3-8 Circuit diagram of charging operation when low-side FWD is ON

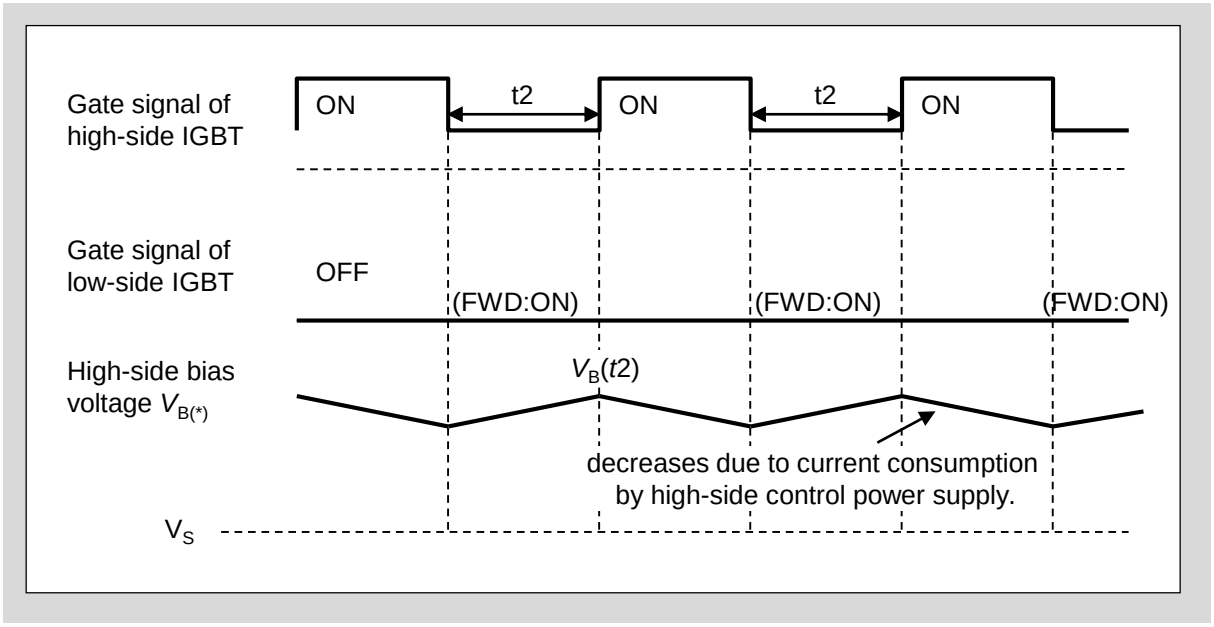

Fig. 3-9 Timing chart of charging operation when low-side FWD is ON

<Setting the bootstrap capacitance and minimum ON/OFF pulse width>

The bootstrap capacitance can be determined by the following equation:

$$C = I_{CCHB} \cdot \frac{t1}{dV}$$

* $t1$: the maximum ON pulse width of the high-side IGBT
* I_{CCHB} : consumption current of high-side drive power supply (temperature and frequency dependent)
* dV : allowable discharge voltage of $V_{B(*)}$ (refer to Fig.3-10)

- Certain margin should be added to the calculated capacitance. In general, select a capacitor that is two to three times of the calculated result.
- The recommended minimum ON pulse width ($t2$) of the low-side IGBT should be determined such that the time constant $R \cdot C$ will enable the discharged voltage (dV) to be fully recharged again during the ON period.
- In the case of the control mode which only the high-side IGBT performs switching operation (Fig. 3-10), the time constant should be set so that the discharged voltage can be fully recharged again during the high-side IGBT OFF (low-side FWD ON) period.
- The minimum pulse width is decided by the minimum ON pulse width of the low-side IGBT, or the minimum OFF pulse width of the high-side IGBT, whichever is longer.

$$t2 \geq \frac{R \cdot C \cdot dV}{V_{CC} - V_B(\min)}$$

* $t2$: Minimum ON pulse width of low-side IGBT
* R : Bootstrap circuit resistance $\Delta R_{F(BSD)}$
* C : Bootstrap capacitance
* dV : Allowable discharge voltage of $V_{B(*)}$
* V_{CC} : Voltage of high-side, low-side control power supply (ex.15V)
* V_B(min) : Minimum voltage of high-side bias voltage (add margin to $V_{B(ON)}$, ex.14V)

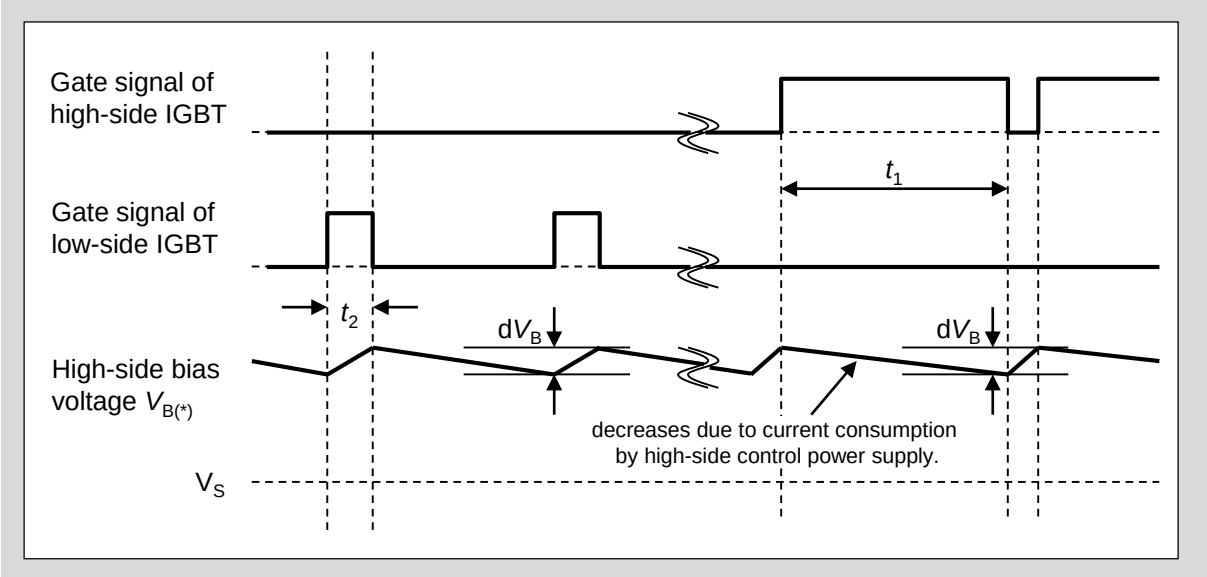

Fig. 3-10 Timing chart of charging and discharging operation

<Setting the initial charging of bootstrap capacitor>

- Initial charging of the bootstrap capacitor is required to start the inverter.
- The pulse width or the number of pulses should be long enough to fully charge the bootstrap capacitor.
- For reference, it takes about 10ms to charge a 47uF capacitor through the built-in bootstrap diode.

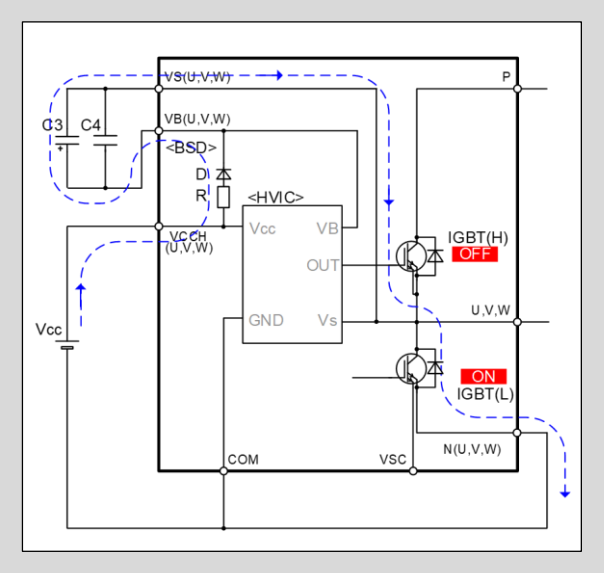

Fig. 3-11 Circuit diagram of initial charging operation

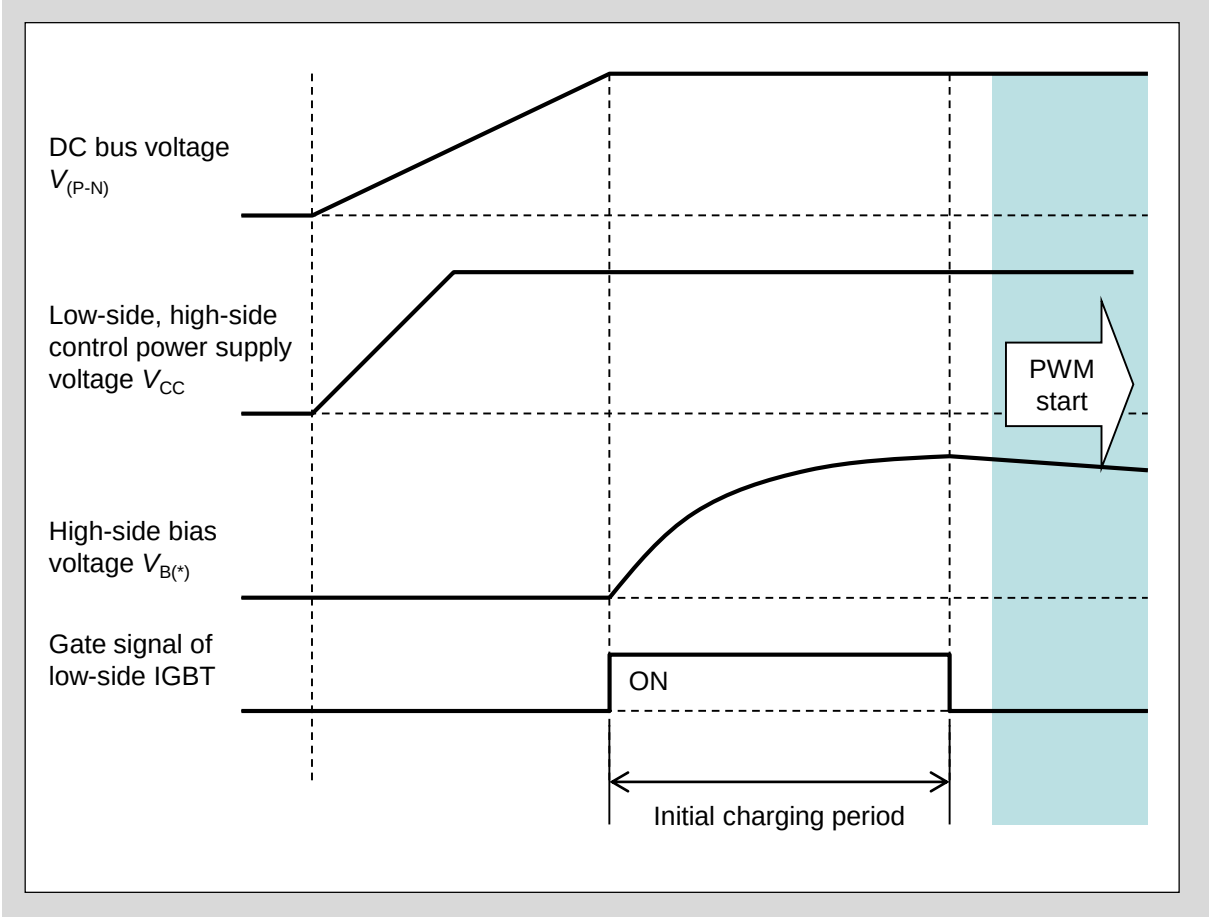

Fig. 3-12 Timing chart of initial charging operation

<BSD built-in current limiting resistance characteristic>

The bootstrap diode has built-in current limiting resistor of 20Ω (typ.). Fig. 3-13 and Fig. 3-14 show the V_F-I_F characteristics of the bootstrap diode.

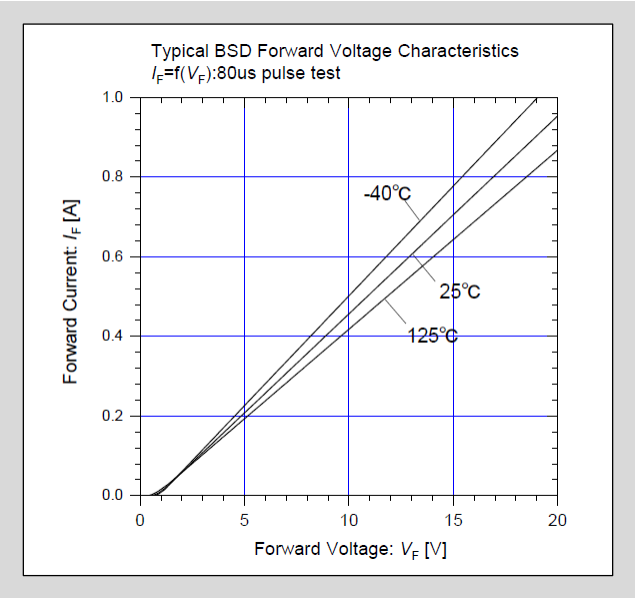

Fig. 3-13 V_F-I_F characteristic of BSD

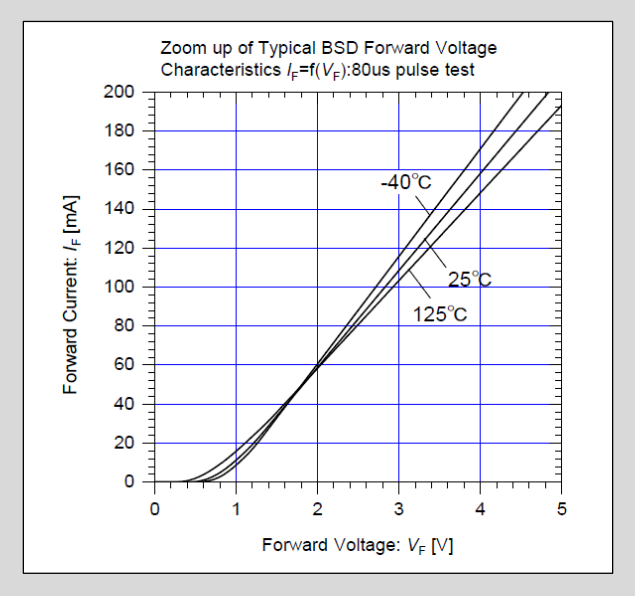

Fig. 3-14 V_F-I_F characteristic of BSD (zoom at low current range)

4. Signal Input, IN(HU,HV,HW), IN(LU,LV,LW)

<Input terminals connection>

- Fig. 3-15 shows an example of interface circuit between MPU and the product. The input terminals can be connected directly to the MPU. The input terminals have built-in pull-down resistors, so there is no need for external pull-down resistors. Also, the input logic is high active, thus there is no need for external pull-up resistors.
- Insert RC filter circuit as shown by the dotted line in Fig. 3-15 if noise is superimposed on long signal wire. Adjust the RC constant according to the PWM control method and the wiring pattern of the printed circuit board.

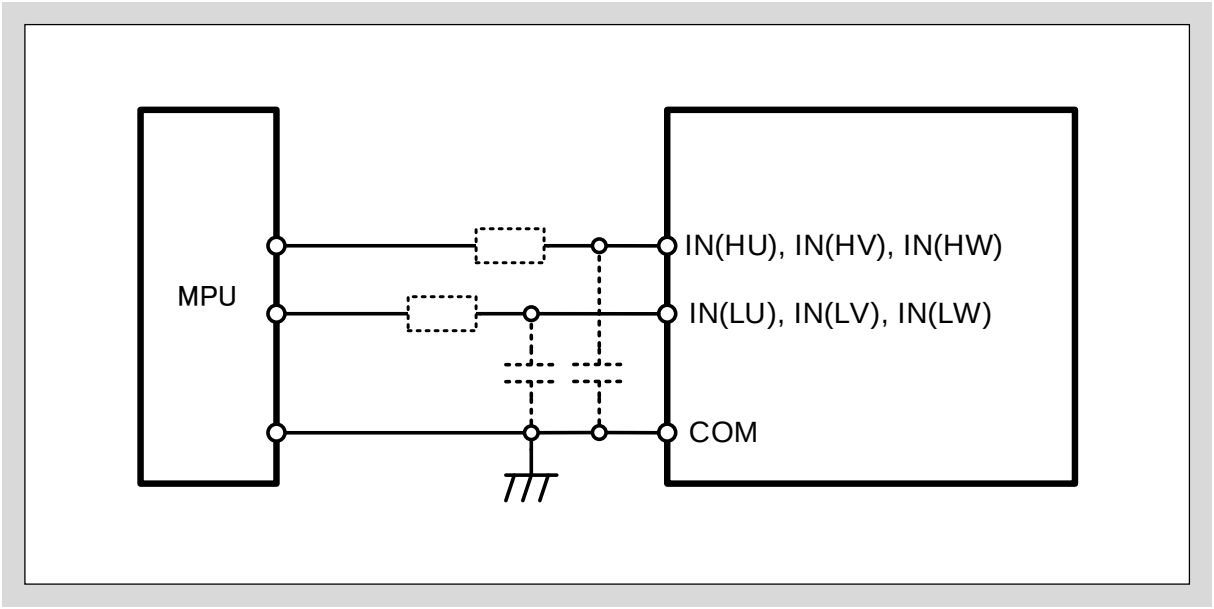

Fig. 3-15 Recommended MPU I/O interface circuit of IN(HU,HV,HW), IN(LU,LV,LW) terminals

<Input terminals circuit>

- The input logic of this product is high active. Thus, the input signal has no restriction on the power supply startup and shutdown sequence, so the system is fail safe. In addition, as shown in Fig. 3-16, the input terminals have built-in pull-down resistors, thus there is no need for external pull-down resistors, reducing the number of system components. Furthermore, a 3.3V-class MPU can be connected directly since the input signal threshold voltage is low.
- In the case of connecting an external filter resistor between the MPU and the input terminal of the product, make sure that the input terminal voltage is above the input signal threshold voltage in consideration of the built-in pull-down resistor.
- As shown in Fig.3-16, diodes are connected to the VCCL-IN(HU,HV,HW,LU,LV,LW) and IN(HU,HV,HW,LU,LV,LW)-COM terminals. These diodes are built-in to protect the product from input surge voltage. Do not use these diodes for voltage clamp purpose as it might damage the product.

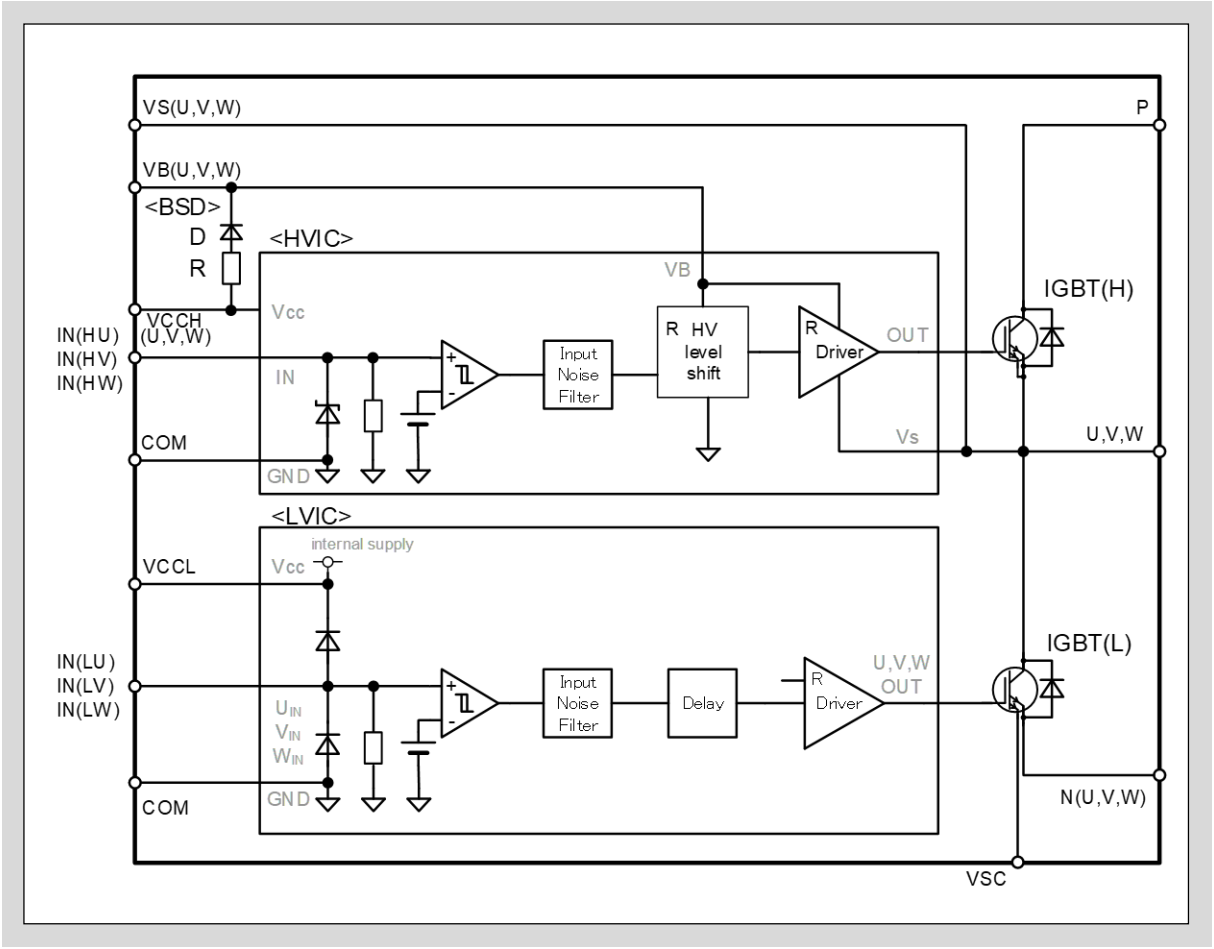

Fig.3-16 Circuit of IN(HU,HV,HW), IN(LU,LV,LW) terminals

<IGBT drive state and input signal pulse width>

$t_{IN(on)}$ is the recommended minimum ON pulse width required to turn-on the IGBT without malfunction, and $t_{IN(off)}$ is the recommended minimum OFF pulse width required to turn-off the IGBT without malfunction. Fig. 3-17 and Fig. 3-18 show the IGBT drive state at various input signal pulse width.

A : IGBT might turn-on even when the input signal ON pulse width is less than minimum $t_{IN(on)}$. In the case of input signal ON pulse width is less than minimum $t_{IN(on)}$ and a voltage below -5V is applied between U-COM, V-COM, W-COM terminals, not only the product might be broken but also the IGBT might not turn-off due to malfunction of the control circuit.

B : In steady state operation. IGBT operates in the linear region.

C : IGBT might turn-off even when the input signal OFF pulse width is less than minimum $t_{IN(off)}$. In the case of input signal OFF pulse width is less than minimum $t_{IN(off)}$ and a voltage below -5V is applied between U-COM, V-COM, W-COM terminals, not only the product might be broken but also the IGBT might not turn-on due to malfunction of the control circuit.

D : In steady state operation. IGBT is completely turned off.

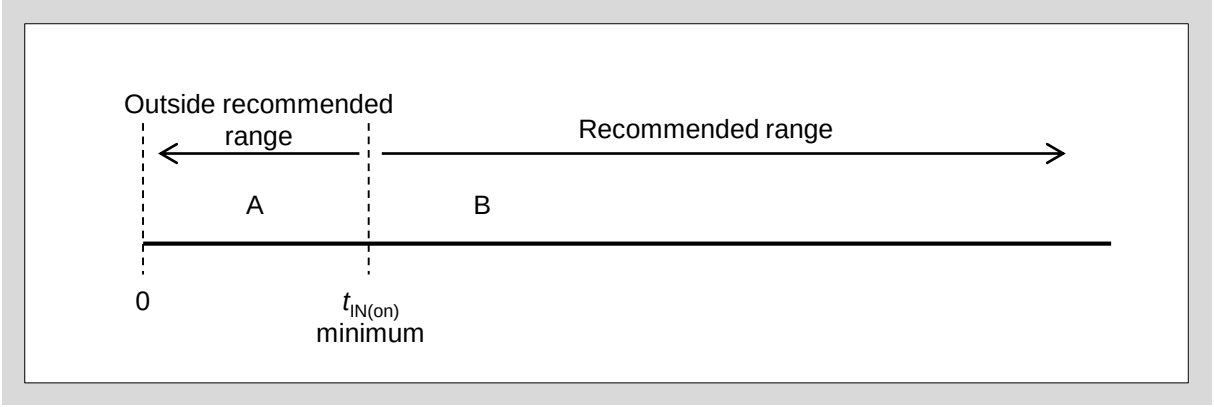

Fig. 3-17 IGBT drive state versus input signal ON pulse width

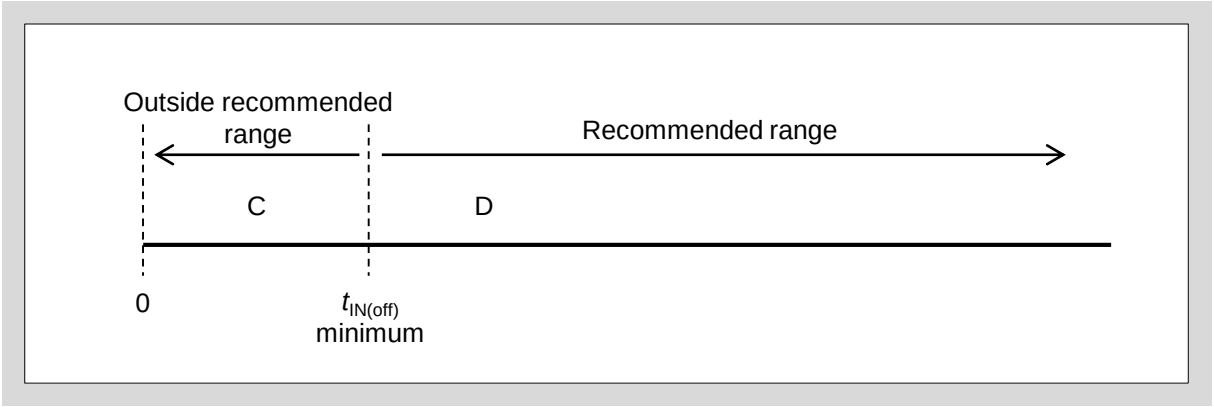

Fig. 3-18 IGBT drive state versus input signal OFF pulse width

5. Overcurrent Protection Function, IS

- The overcurrent (OC) protection works by detecting the voltage generated at the external shunt resistor connected between N(U,V,W) and COM terminal, or the voltage generated at the sense resistor connected between VSC and COM terminal, and input to IS terminal. When this voltage exceeds $V_{IS(ref)}$, all low-side IGBTs are turned-off and fault output is generated.
- Fig. 3-19 shows the OC protection detection circuit of IS terminal. Fig. 3-20 shows the OC protection operation sequence.
- To prevent the product from unnecessary operations due to switching noise or recovery current during normal operation, it is recommended to insert an external RC filter (time constant is approximately 1.1μs) to the IS terminal. Keep the wiring between the product and the shunt resistor as short as possible.
- As shown in Fig. 3-19, diodes are connected between VCCL-IS and IS-COM terminals. These diodes are built-in to protect the product from input surge voltage. Do not use these diodes for voltage clamp purpose as it might damage the product.

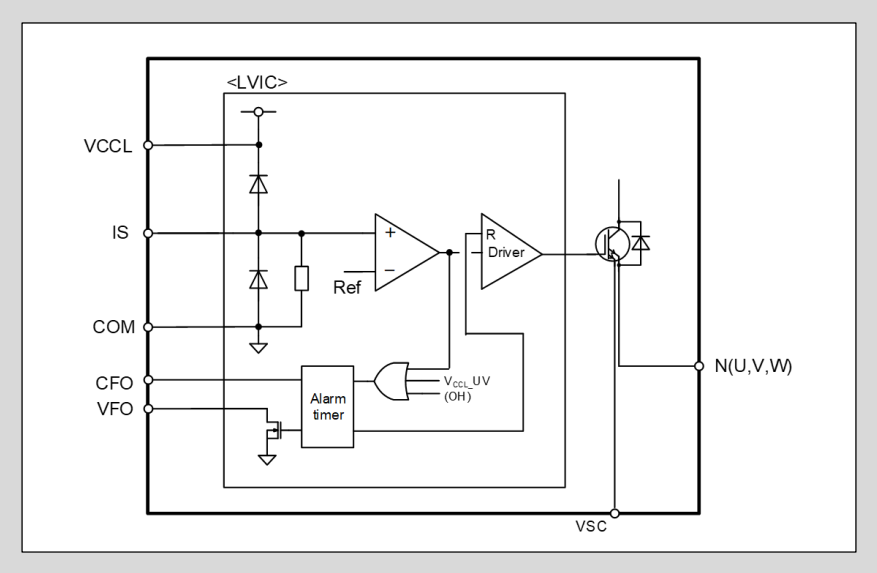

Fig. 3-19 OC protection detection circuit of IS terminal

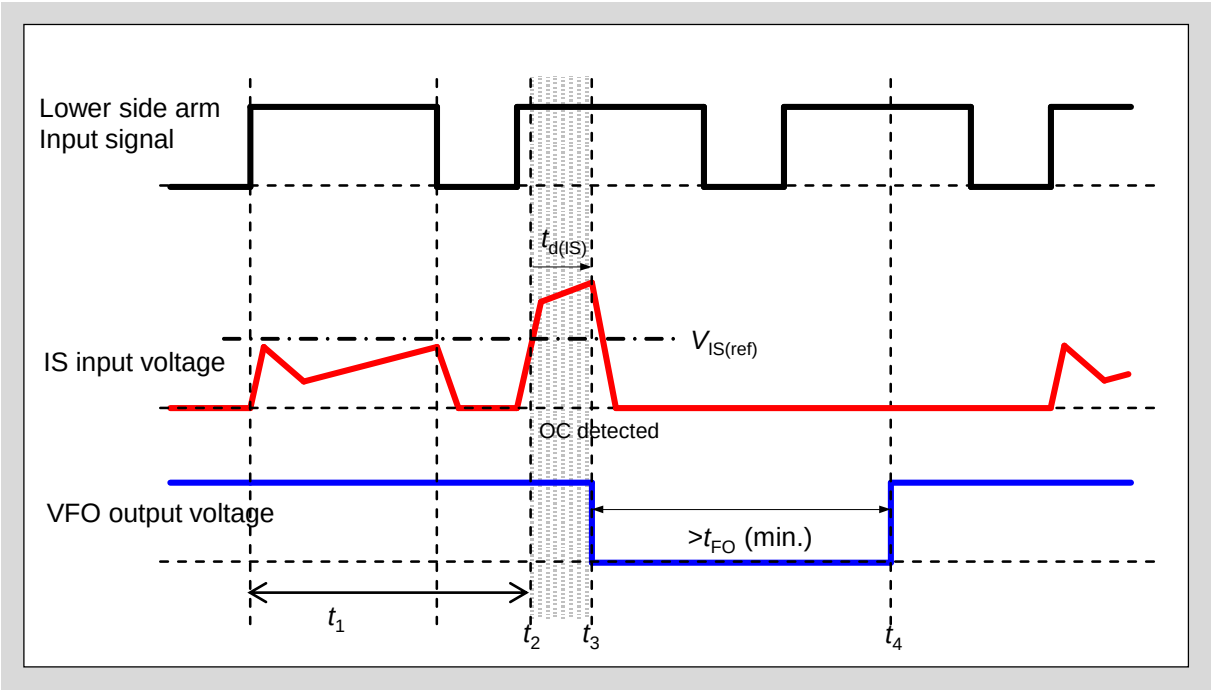

Fig. 3-20 OC protection operation sequence

*t*1: The IS input voltage is less than $V_{IS(ref)}$. All low-side IGBTs perform normal switching operation.

*t*2 :When IS input voltage exceeds $V_{IS(ref)}$, OC is detected.

*t*3: Fault output voltage is generated and all low-side IGBTs are turned off after the overcurrent protection delay time $t_{d(IS)}$. Propagation delay of LVIC is included in $t_{d(IS)}$.

*t*4: OC protection is reset after t_{FO}. LVIC restarts switching operation from the next input signal.

6. Fault Status Output Function, VFO, CFO

- As shown in Fig. 3-21, it is possible to connect the fault status output terminal VFO directly to the MPU.
- The VFO terminal is open drain configured, thus this terminal should be pulled up to 5V or 3.3V DC logic power supply with a 10kΩ resistor. It is also recommended to connect a bypass capacitor C1 and inrush current limiting resistor R1 of 5kΩ or more between the MPU and the VFO terminal. These signal lines should be as short as possible.
- VFO terminal generates fault status output during UV protection of VCCL, OC protection, and OH protection. (OH protection is built into “6MBP ** XTC065-50”)
- The pulse width of the fault status output (t_{FO}) can be adjusted by the capacitance of the capacitor between CFO and COM terminal. The fault status output pulse width is 2.4ms when the capacitor capacitance is 22nF. CFO is given by CFO (typ.) = t_{FO} x (9.1 x 10-6) [F].
- As shown in Fig. 3-21, diodes are connected between VCCL-VFO and VFO-COM terminals. These diodes are built-in to protect the product from input surge voltage. Do not use these diodes for voltage clamp purpose as it might damage the product.
- Fig. 3-22 shows the voltage-current characteristics of VFO terminal during fault status output. I_{FO} is the sink current of VFO terminal.

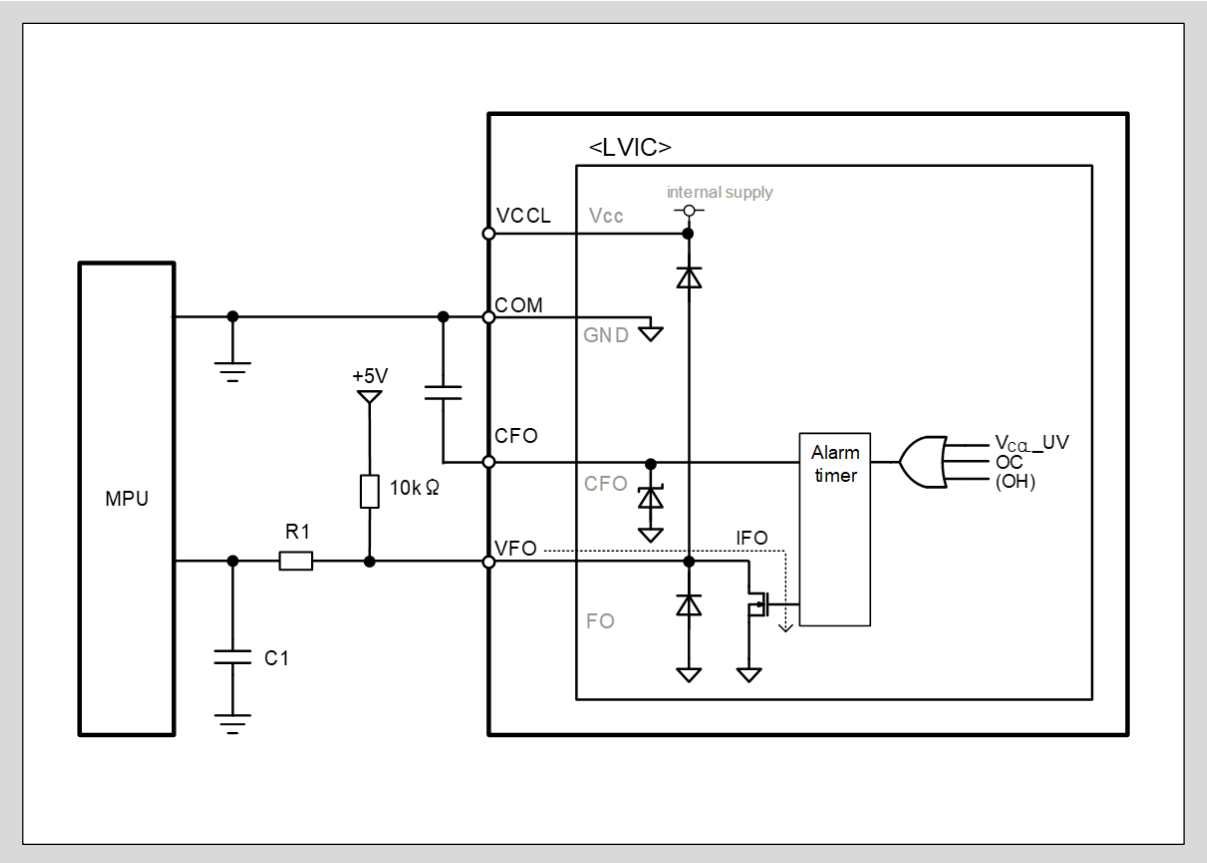

Fig. 3-21 Recommended MPU I/O interface circuit of VFO terminal

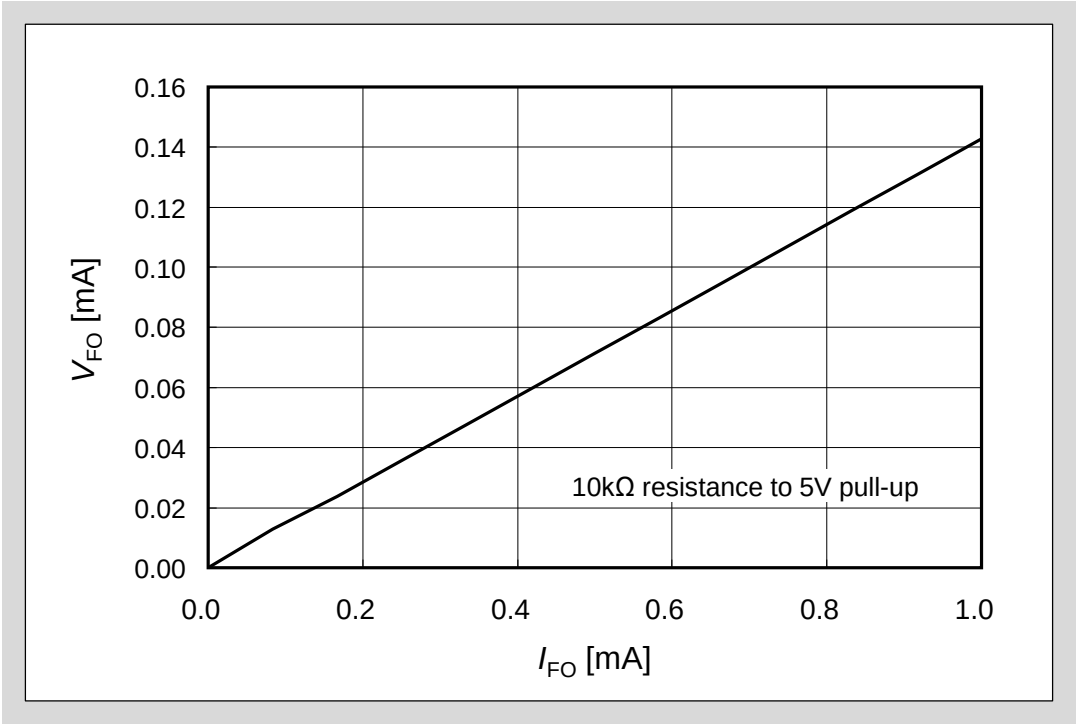

Fig. 3-22 Voltage-current characteristics of VFO terminal during fault status output

7. Temperature Output Function, TEMP

- As shown in Fig. 3-23, the temperature output terminal TEMP can be connected directly to the MPU. It is recommended to connect a bypass capacitor C_{TEMP} and an inrush current limiting resistor R_{TEMP} of 10kΩ or more between the MPU and the TEMP terminal. These signal lines should be as short as possible.
- This product has a built-in temperature sensor in LVIC that outputs analog voltage according to the LVIC virtual junction temperature. This function has no fault status output because it is not intended to protect the product. "6MBP ** XTC065-50" has built-in overheating (OH) protection. Fault status output is generated when the temperature exceeds T_{OH}.
- Since the position of the IGBT chip and the position of the temperature sensor are different, it is not possible to respond to sudden rise in T_{vj} such as during motor lock and short circuit.
- As shown in Fig. 3-23, a diode is connected between the TEMP-COM terminals. This diode is built-in to protect the product from input surge voltage. Do not use this diode for voltage clamp purpose as it might damage the product.
- Fig. 3-24 shows the LVIC virtual junction temperature versus TEMP output voltage characteristics. In the case of the MPU power supply voltage is 3.3V, connect a Zener diode to the TEMP terminal. The output voltage shows clamp characteristic at below room temperature. Connect a 5kΩ±10% pull-down resistor $R_{pulldown}$ to the TEMP terminal if linear characteristic is required.
- Fig. 3-25 shows the LVIC virtual junction temperature versus TEMP output voltage characteristics with 5kΩ pull-down resistor.
- Fig. 3-26 shows the operation sequence of the TEMP terminal during startup and shutdown of product.

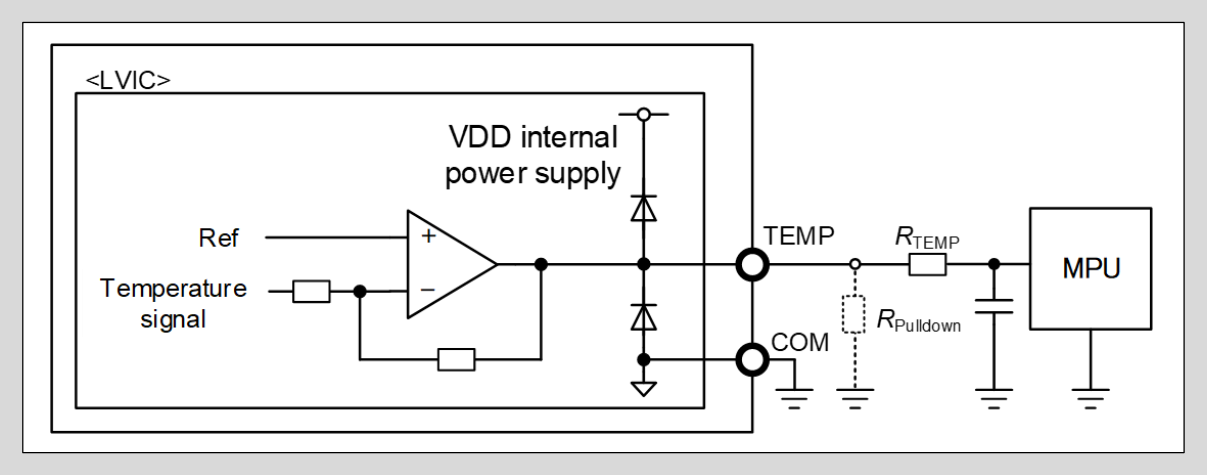

Fig. 3-23 Recommended MPU I/O interface circuit of TEMP terminal

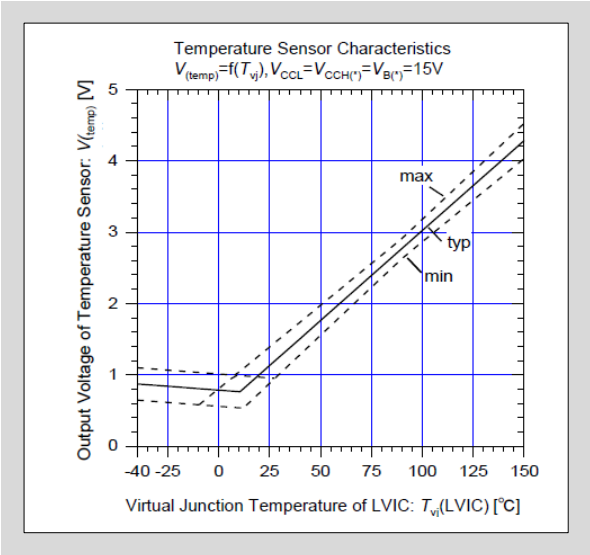

Fig. 3-24 LVIC virtual junction temperature vs. TEMP output voltage characteristic (without pull-down resistor)

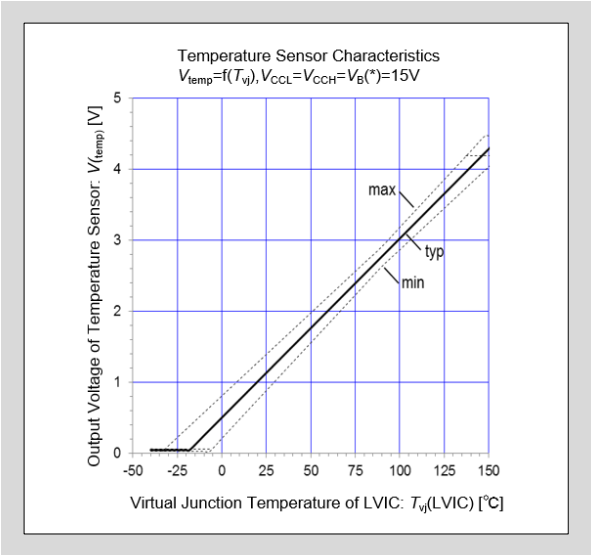

Fig. 3-25 LVIC virtual junction temperature vs. TEMP output voltage characteristic (with 5kΩ pull-down resistor)

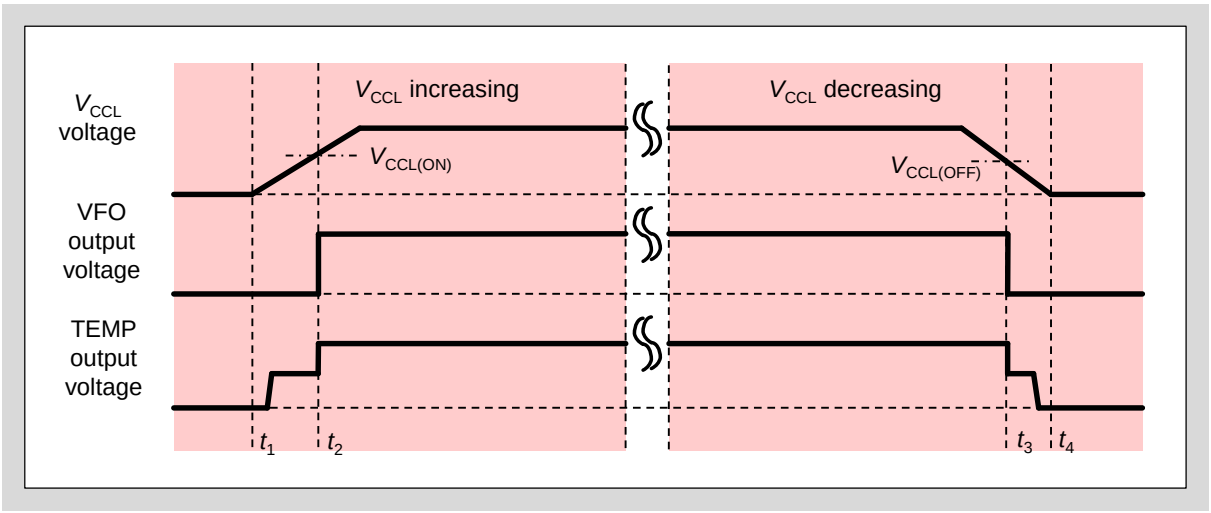

Fig. 3-26 Operation sequence of TEMP terminal during startup and shutdown

*t*1-*t*2 : TEMP output function is activated when V_{CCL} exceeds $V_{CCL(ON)}$. When V_{CCL} is lower than $V_{CCL(ON)}$, TEMP output voltage is the same as clamp voltage.

*t*2-*t*3 : TEMP output voltage rises to the voltage determined by LVIC virtual junction temperature. Under temperature condition that cause clamp operation, TEMP output voltage is the same as clamp voltage even if V_{CCL} exceeds $V_{CCL\ (ON)}$.

*t*3-*t*4 : TEMP output function is reset when V_{CCL} falls below $V_{CCL(OFF)}$. TEMP output voltage is the same as clamp voltage.

8. Overheating Protection Function

- The over heating (OH) protection functions is integrated into "6MBP**XTC065-50".
- The OH function monitors the LVIC junction temperature. Since the position of the IGBT chip and the position of the temperature sensor are different, it is not possible to respond to sudden rise in T_{vj} such as during motor lock and short circuit.
- The T_{OH} sensor position is shown in Fig.2-3.
- As shown in Fig.3-27, the product shuts down all low side IGBTs when the LVIC temperature exceeds T_{OH}. The fault status is reset when the LVIC temperature drops below $T_{OH} - T_{OH(hys)}$.

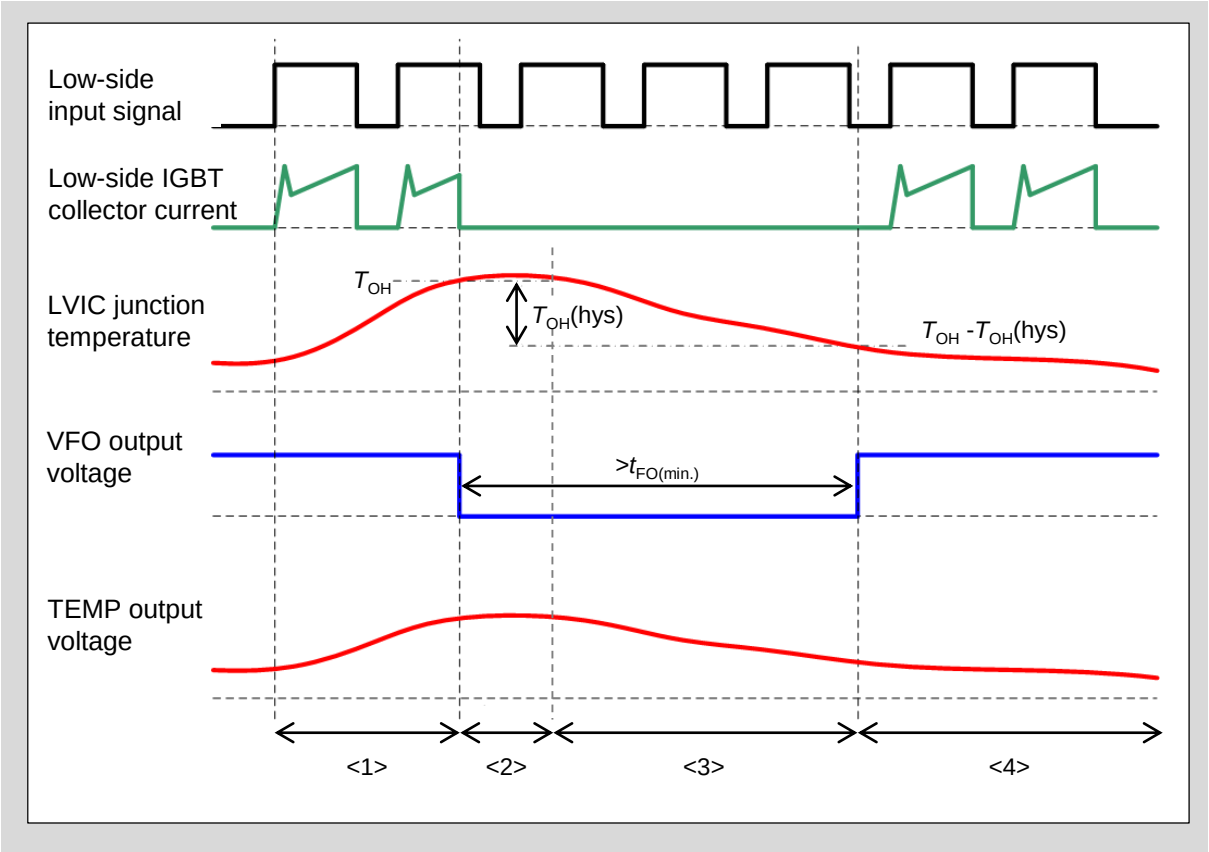

Fig. 3-27 OH protection operation sequence

<1> : When LVIC virtual junction temperature is below T_{OH}, all low-side IGBTs operate normally.

<2> : While LVIC virtual junction temperature is above T_{OH}, all low-side IGBTs are turned off and fault output voltage is generated.

<3> : During OH protection status, TEMP terminal continues to output voltage corresponding to LVIC virtual junction temperature.

<4> : Fault status and OH protection status are reset after LVIC virtual junction temperature falls below T_{OH}-$T_{OH(hys)}$ and t_{FO} has elapsed. The low-side IGBTs restart operation from the next input signal. $T_{OH(hys)}$ is the hysteresis temperature of overheating protection.