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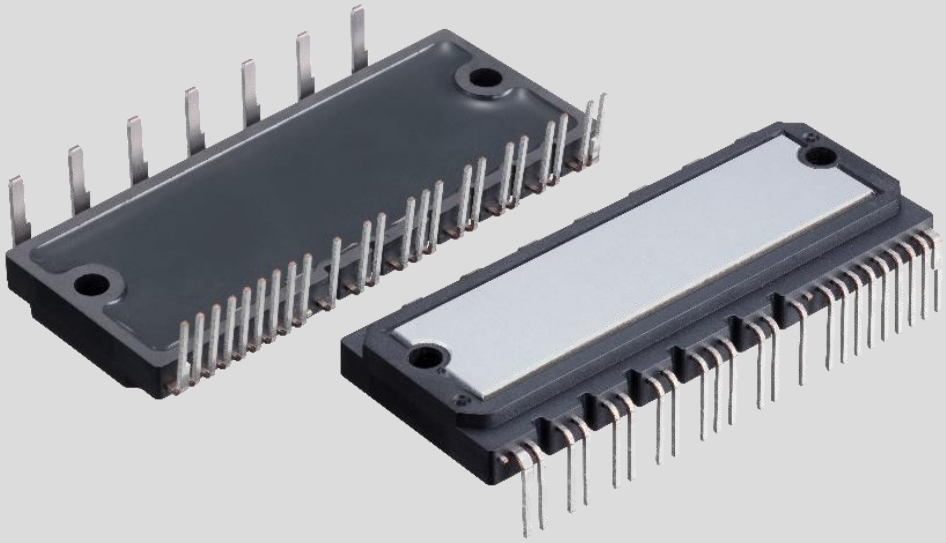

Small IPM (Intelligent Power Module)
P642 Series
6MBP**XT*065-50

Application Manual

April 2024

Fuji Electric Co., Ltd.

MT6M15234 c

Cautions

This Instruction contains the product specifications, characteristics, data, materials, and structures as of April 2024. The contents are subject to change without notice for specification changes or other reason. When using a product listed in this Instruction be sure to obtain the latest specifications.

The application examples in this note show the typical examples of using Fuji products and this note shall neither assure to enforce the industrial property including some other rights nor grant the license.

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The products described in this application manual are manufactured with the intention of being used in the following industrial electronic and electrical devices that require normal reliability.

- Compressor motor inverter
- Fan motor inverter for room air conditioner
- Compressor motor inverter for heat pump applications, etc.

If you need to use a semiconductor product in this application note for equipment requiring higher reliability than normal, such as listed below, be sure to contact Fuji Electric Co., Ltd. to obtain prior approval. When using these products, take adequate safety measures such as a backup system to prevent the equipment from malfunctioning when a Fuji Electric's product incorporated in the equipment becomes faulty.

- Transportation equipment (mounted on vehicles and ships)
- Trunk communications equipment
- Traffic-signal control equipment
- Gas leakage detectors with an auto-shutoff function
- Disaster prevention / security equipment
- Safety devices, etc.

Do not use a product in this application note for equipment requiring extremely high reliability such as:

- Space equipment
- Airborne equipment
- Atomic control equipment
- Submarine relaying equipment
- Medical equipment

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CONTENTS

CONTENTS

Chapter 1 Product Outline

This manual describes the following contents for Fuji IGBT Intelligent Power Module “Small IPM P642 series”

- Product summary
- Explanation of terminal symbols and terms
- Detailed explanation and design guideline of control terminals and power terminals
- Recommended wiring, layout and mounting guidelines

1. Introduction

<Product overview>

- IGBT modules used in inverters for compressors and air conditioner fans are developing rapidly in response to the growing demand for energy saving, equipment miniaturization and weight reduction.
- IGBTs are devices that combine the high-speed switching performance of power MOSFETs and the high-voltage, high-current capabilities of bipolar transistors, and are expected to further develop in the future.
- Among them, the IPM (Intelligent Power Module) is a 3-phase IGBT inverter bridge circuit with integrated gate drive circuits and protection circuits.

<Product features>

- 7th generation IGBT technology reduces power loss and realizes energy saving of equipment.
- Expansion of operating current by guaranteed T_{vjop}=150ºC and time limited T_{vj}=175ºC operation.
- Expansion of overload operating area by higher accuracy of short circuit protection detection.
- Lineup of 650V / 50A, 75A.
- Total power loss is reduced by improving the trade-off between Collector-Emitter saturation voltage $V_{CE(sat)}$ and switching loss.

<Internal circuit>

- The control IC of upper side arms have built-in high voltage level shift circuit (HVIC).
- Both the low-side and high-side IGBTs can be driven directly by a microprocessor. The voltage level of input signal is 3.3V or 5.0V.
- No reverse bias power supply is required due to the wiring length between the built-in drive circuit and IGBT is short and the impedance of the drive circuit is low.
- IPM has built-in bootstrap diodes (BSD) and can be driven by a single power supply. No insulated power supplies for the high-side drive are needed.

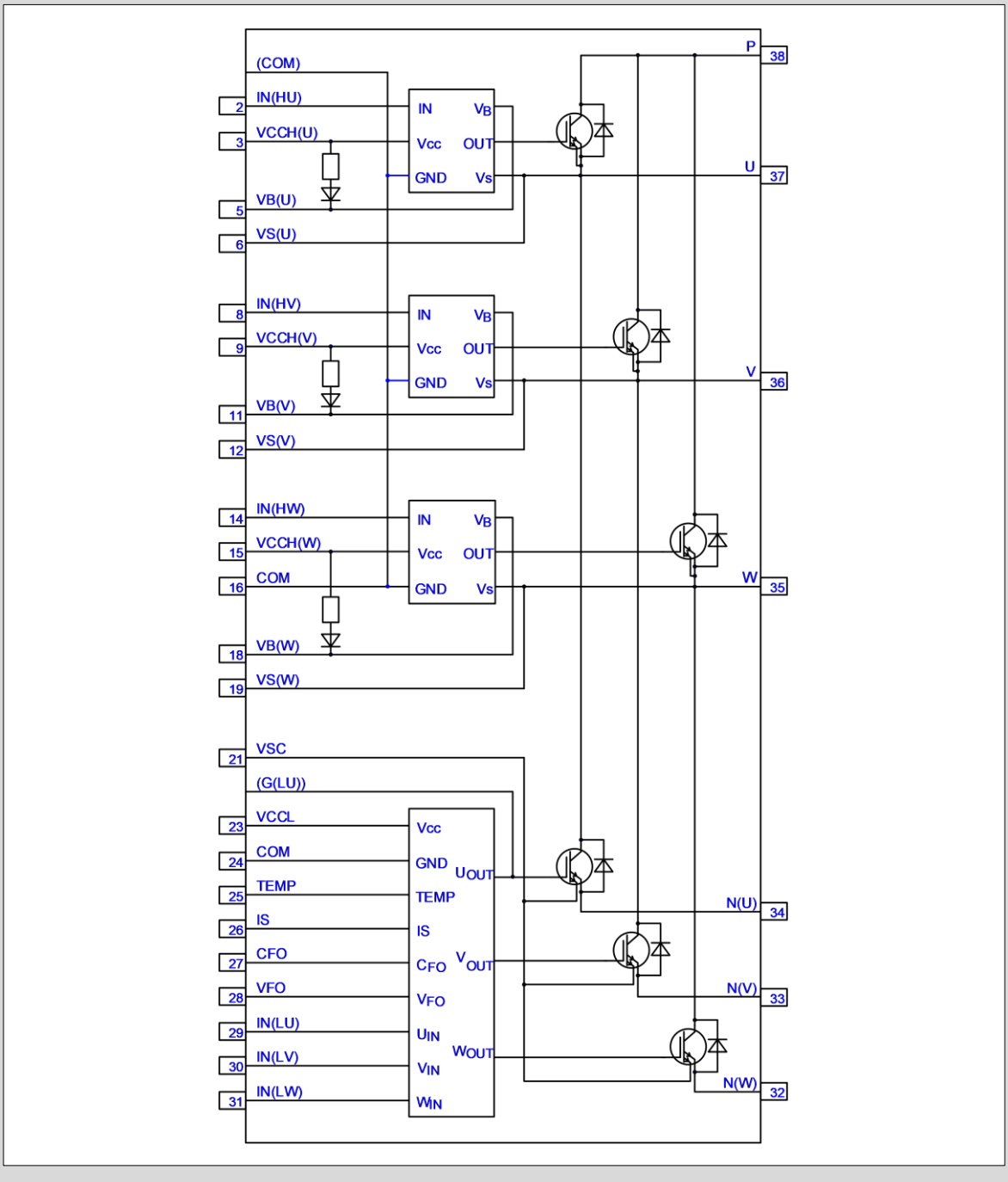


Fig.1-1 Internal circuit diagram

<Built-in protection circuit>

- The following built-in protection circuits are incorporated in the product:
  (OC): Overcurrent protection
  (UV): Under voltage protection for power supplies of control IC
  (LT): Temperature sensor output function
  (OH): Overheating protection (only applied to some products)
  (FO): Fault status output
- The OC protection circuit protects the IGBT from overcurrent due to load short-circuit and arm short-circuit. This protection circuit adopts both sense current method and external shunt resistor method, thus arm short-circuit protection is possible.
- The UV protection circuit is triggered when there is voltage drop at the control power supply and the high-side drive power supply. It is integrated into all IGBT drive circuits.
- The OH protection circuit protects the product from overheating. It is built into the low-side control IC (LVIC).
- The temperature sensor output function outputs temperature as analog voltage. It is built into LVIC.
- The FO function outputs a fault signal when the product detects abnormal conditions. By outputting a fault signal to the microprocessor unit (MPU), it is possible to shut down and prevent destruction of the system.

<Compact package>

- This product uses aluminum insulated metal substrate (IMS) and has excellent heat dissipation.
- The pitch between control terminals is 2.54mm.
- The pitch between power terminals is 10mm.

Fig.1-2 Package external view

2. Product Lineup and Target Application

Table 1-1 Lineup

Type Name	IGBT Rating		Isolation Voltage [Vrms]	Variation *1
	Voltage [V]	Current [A]		
6MBP50XTA065-50	650	50	2500Vrms Sinusoidal 60Hz, 1min. (Between all shorted terminals and IMS)	LT
6MBP50XTC065-50				LT OH
6MBP75XTA065-50		75		LT
6MBP75XTC065-50				LT OH

*1 (LT): Temperature sensor output function
(OH): Overheating protection function

3. Definition of Type Name

• Type Name

6 MBP 50 X T C 065 –50

- 6 : Number of switching elements
  6 : 6 switching elements
- MBP : Indicates IGBT-IPM
- 50 : IGBT current rating
  50:50A, 75:75A
- X : Series name
  X: Chip generation
- T : Series name
  T: Package type
- C : Additional series code
  A : Temperature sensor output
  C : Temperature sensor output and Overheat protection
- 065 : Voltage rating
  065 : 650V
- 50 : Additional model number (Option)
  50 : RoHS

Fig. 1-3 Definition of Type

4. Marking Specification

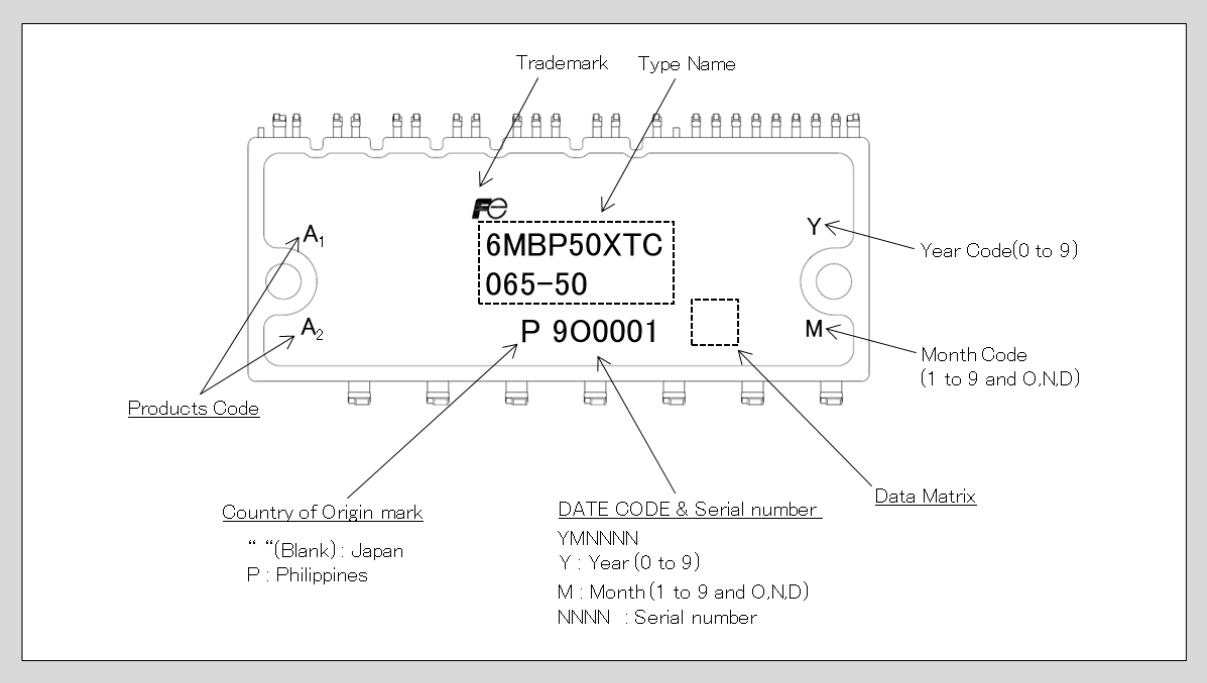
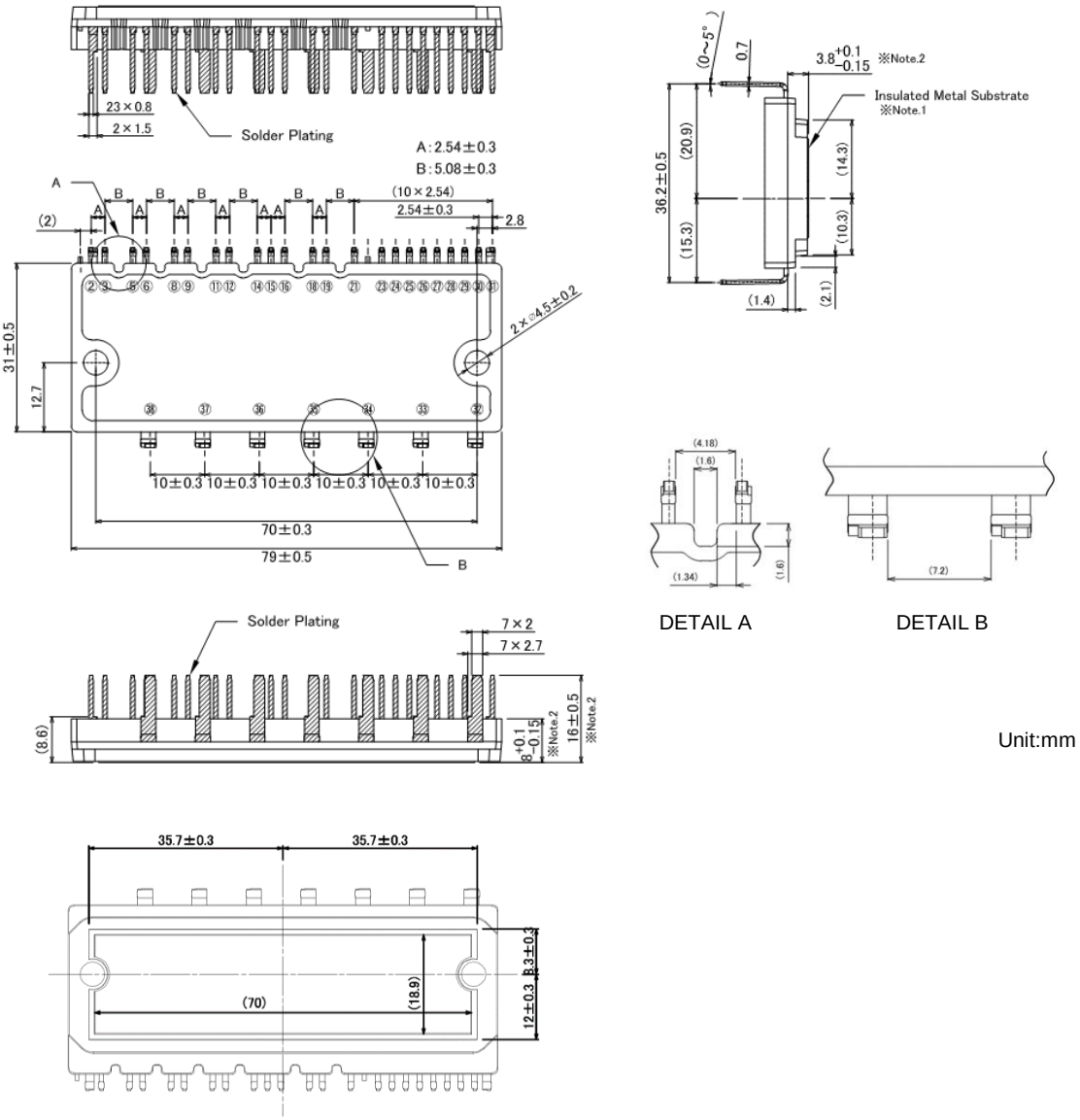


Fig. 1-4 Marking specification

Table 1-2 Products code

TYPE NAME	PRODUCT CODE	
	A_1	A_2
6MBP50XTA065-50	A	A
6MBP50XTC065-50	A	C
6MBP75XTA065-50	B	A
6MBP75XTC065-50	B	C

5. Package Outline Dimension



Unit:mm

Note.1
The IMS (Insulated Metal Substrate) is deliberately protruded to improve the thermal conductivity between IMS and heat-sink.

Note.2
Thickness from the package surface to the back side including the IMS.

Fig. 1-5 Case outline drawing

6. Absolute Maximum Ratings

An example of the absolute maximum ratings of 6MBP50XTA065-50 is shown in Table 1-3 and Table 1-4.

Table 1-3 Inverter Block Absolute Maximum Ratings at T_{vj}=25°C, T_c=25°C, V_{CC}*1=15V, $V_{B(*)}$=15V (unless otherwise specified)

Item	Symbol	Rating	Unit	Description
DC Bus Voltage	$V_{DC\ (terminal)}$	450	V	DC voltage that can be applied between P-N(U), N(V), N(W) terminals. Please refer to Fig. 1-5 for details.
Bus Voltage (Surge)	$V_{DC(Surge,\ terminal)}$	500	V	Peak value of the surge voltage that can be applied between P-N(U),N(V),N(W) terminals during switching operation. Please refer to Fig. 1-5 for details.
Collector-Emitter Voltage	$V_{CE(chip)}$	650	V	Maximum collector-emitter voltage of IGBT and repeated peak reverse voltage of FWD. Please refer to Fig. 1-5 for details.
Collector Current	I_C	50	A	Maximum collector current of IGBT at T_c=25°C, T_{vj}=150°C*2
Peak Collector Current	I_{CP}	100	A	Maximum pulse collector current of IGBT at T_c=25°C, T_{vj}=150°C*2
Forward Current	I_F	50	A	Maximum forward current of FWD at T_c=25°C, T_{vj}=150°C*2
Peak Forward Current	I_{FP}	100	A	Maximum pulse forward current of FWD at T_c=25°C, T_{vj}=150°C*2
Collector Power Dissipation	P_{D_IGBT}	132	W	Maximum power dissipation per IGBT at T_c=25°C, T_{vj}=150°C*2
FWD Power Dissipation	P_{D_FWD}	89	W	Maximum power dissipation per FWD at T_c=25°C, T_{vj}=150°C*2
Self Protection DC Bus Voltage (arm short-circuit)	$V_{DC(sc)}$	400	V	Maximum DC voltage at which IGBT can be safely shut off by the IPM's protection function during short-circuit or overcurrent. Please refer to Fig. 1-5 for details.
Maximum Virtual Junction Temperature of Inverter Block	T_{vj}	175	°C	Maximum virtual junction temperature of IGBT and FWD*3
Operating Virtual Junction Temperature of Inverter Block	T_{vjop}	-40 ~ +150	°C	Virtual Junction Temperature of IGBT and FWD during continuous operation *3

*1 V_{CC} is applied between VCCH(U,V,W)-COM and VCCL-COM terminals.

*2 Pulse width and duty are limited by T_{vj}.

*3 The maximum virtual junction temperature during continuous operation is T_{vj}=150°C. Continuous operation at over T_{vj}=150°C may result in degradation of product lifetime such as power cycling capability with respect to the designed lifetime.

Table 1-4 Control Circuit Block Absolute Maximum Ratings at T_{vj}=25°C, T_c=25°C,V_{CC} [*1]=15V, $V_{B(*)}$=15V (continued)

Item	Symbol	Rating	Unit	Description
High-side Supply Voltage	$V_{CCH(U)}$ $V_{CCH(V)}$ $V_{CCH(W)}$	-0.5 ~ 20	V	Voltage that can be applied between VCCH(U) - COM, VCCH(V) - COM, VCCH(W) - COM terminals.
Low-side Supply Voltage	V_{CCL}	-0.5 ~ 20	V	Voltage that can be applied between VCCL-COM terminals.
High-side Bias Absolute Voltage	$V_{VB(U)-COM}$ $V_{VB(V)-COM}$ $V_{VB(W)-COM}$	-0.5 ~ 670	V	Voltage that can be applied between VB(U)-COM, VB(V)-COM, VB(W)-COM terminals.
High-side Bias Voltage for IGBT Gate Driving	$V_{B(U)}$ $V_{B(V)}$ $V_{B(W)}$	-0.5 ~ 20	V	Voltage that can be applied between VB(U)-VS(U), VB(V)-VS(V), VB(W)-VS(W) terminals.
High-side Bias Offset Voltage	V_U V_V V_W	-5 ~ 650	V	Voltage that can be applied between U-COM, V-COM, W-COM terminals. [*4]
Input Signal Voltage	V_{IN}	-0.5 ~ V_{CCH}+0.5 -0.5 ~ V_{CCL}+0.5	V	Voltage that can be applied between IN(HU)-COM, IN(HV)-COM, IN(HW)-COM, IN(LU)-COM, IN(LV)-COM, IN(LW)-COM terminals.
Input Signal Current	I_{IN}	3	mA	Maximum current between IN(HU)-COM, IN(HV)-COM, IN(HW)-COM, IN(LU)-COM, IN(LV)-COM, IN(LW)-COM terminals.
Fault Signal Voltage	V_{FO}	-0.5 ~ V_{CCL}+0.5	V	Voltage that can be applied between VFO-COM terminals.
Fault Signal Current	I_{FO}	1	mA	Maximum sink current between VFO-COM terminals.

(Continued on next page.)

[*4] Apply 13.0V or more between VB(U)-U, VB(V)-V, VB(W)-W terminals.
The product might malfunction if the high-side bias offset voltage is less than -5V.

Table 1-4 Control Circuit Block Absolute Maximum Ratings at T_{vj}=25°C, T_c=25°C, V_{CC} [*1]=15V, $V_{B(*)}$=15V (continued)

Item	Symbol	Rating	Unit	Description
CFO Signal Voltage	V_{CFO}	-0.5 ~ 5.0	V	Voltage that can be applied between CFO-COM terminals.[*5]
CFO Signal Current	I_{CFO}	-0.05 / 3	mA	Maximum source / sink current between CFO-COM terminals.[*5]
Over Current Sensing Input Voltage	V_{IS}	-0.5 ~ V_{CCL}+0.5	V	Voltage that can be applied between IS-COM terminals.
TEMP Signal Voltage	V_{TEMP}	-0.5 ~ 5.0	V	Voltage that can be applied between TEMP-COM terminals.
TEMP Signal Current	I_{TEMP}	-0.05 / 3	mA	Maximum source / sink current between TEMP-COM terminals.
VSC Signal Voltage	V_{VSC}	-0.5 ~ V_{CCL}+0.5	V	Voltage that can be applied between VSC-COM terminals.[*6]
VSC Signal Current	I_{VSC}	-20	mA	Maximum source current between VSC-COM terminals.[*6]
Virtual Junction Temperature of Control Circuit Block	T_{vj}	150	°C	Maximum virtual junction temperature of the control circuit.
Operating Case Temperature	T_c	-40 ~ +125	°C	Operating case temperature (temperature of IMS directly under the IGBT or FWD chip).
Storage Temperature	T_{stg}	-40 ~ +125	°C	Ambient temperature range for storage and transportation (no load condition).
Isolation Voltage	V_{isol}	AC 2500	Vrms	Maximum voltage between IMS and all shorted terminals (Sine wave 60Hz, 1min)

[*5] CFO is output terminal. Do not apply voltage or current. Connect only the specified capacitor between CFO-COM terminals.

[*6] VSC is output terminal. Do not apply voltage or current. Connect only the specified resistor between VSC-COM terminals.

<Absolute Maximum Rating of Collector-Emitter Voltage>

The absolute maximum rating of collector-emitter voltage of the IGBT is specified below. During operation, the voltage between P-N(U, V, W) is usually applied to high-side or low-side of one phase. Therefore, the voltage between P-N(U, V, W) must not exceed the absolute maximum rating of IGBT. The collector-emitter voltage absolute maximum rating is described below.

$V_{CE(chip)}$: Breakdown voltage of IGBT and FWD chip. Because it is difficult to measure directly, please use the product with $V_{DC(terminal)}$, $V_{DC(Surge,terminal)}$ within the absolute maximum rating.

$V_{DC(terminal)}$: DC bus voltage (between P-N(U, V, W) terminals)

$V_{DC(Surge, terminal)}$: DC bus voltage at P-N(U, V, W) terminals including surge voltage generated during switching.

- Fig.1-5 shows the waveforms during short-circuit, IGBT turn-off and FWD reverse recovery. Since $V_{DC(Surge, terminal)}$ is different in each situation, it is necessary to set $V_{DC(terminal)}$ considering these situations.
- $V_{CE(chip)}$ is the collector-emitter voltage absolute maximum rating of the IGBT chip. $V_{DC(Surge, terminal)}$ is specified considering the margin of surge voltage generated by the wiring inductance inside the Product.
- $V_{DC(terminal)}$ is specified considering the margin of surge voltage generated by the wiring inductance between P-N(*) terminals and electrolytic capacitor.

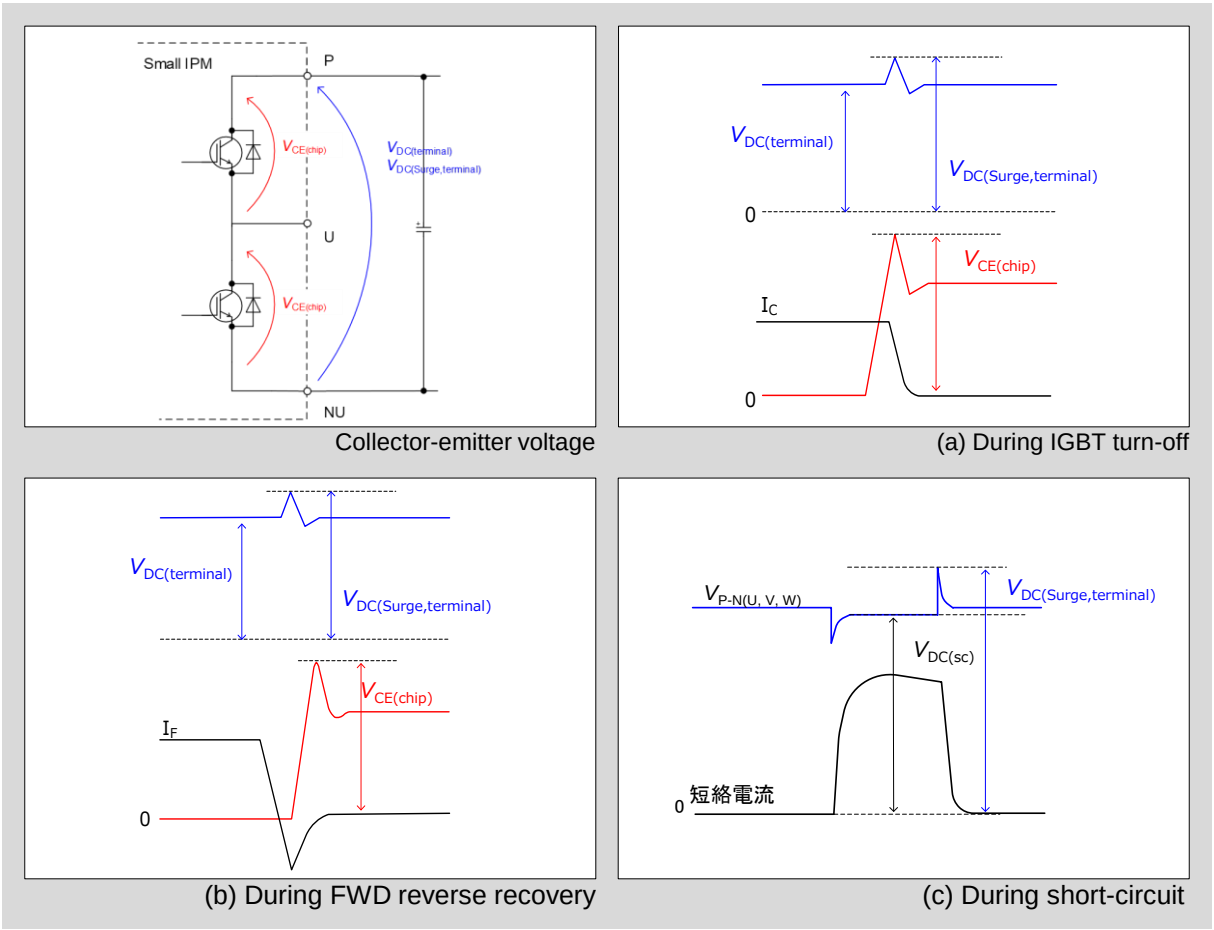


Fig.1-6 Waveforms and Collector-Emitter voltage during IGBT turn-off, FWD reverse recovery, and short-circuit

Chapter 2 Description of Terminal Symbols and Terminology

1. Description of Terminal Symbols

Table 2-1 and Table 2-2 describe the terminal symbols and terminology, respectively.

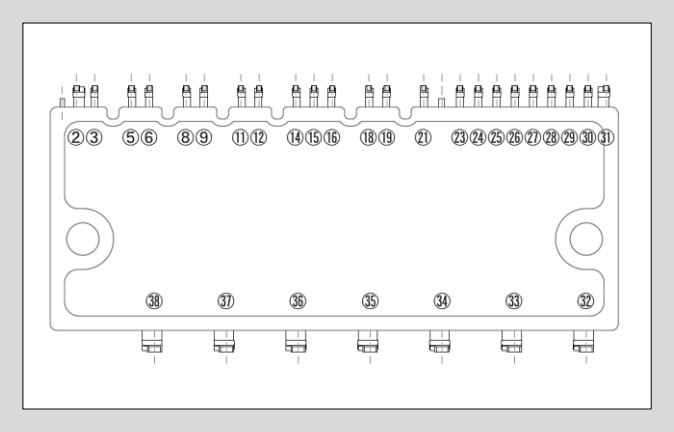


Fig.2-1 Terminals number

Table 2-1 Description of terminal symbols

Terminal No.	Terminal Name	Terminal Description	Terminal No.	Terminal Name	Terminal Description
2	IN(HU)	Signal Input for High-side U-phase	24	COM	Low-side Control Power Supply GND
3	VCCH(U)	High-side Control Power Supply for U-phase	25	TEMP	Temperature Sensor Output
5	VB(U)	High-side Bias Voltage for U-phase	26	IS	Overcurrent Sensing Voltage Input
6	VS(U)	High-side Bias Voltage for U-phase GND	27	CFO	Fault Output Pulse Width Setting
8	IN(HV)	Signal Input for High-side V-phase	28	VFO	Fault Output
9	VCCH(V)	High-side Control Power Supply for V-phase	29	IN(LU)	Signal Input for Low-side U-phase
11	VB(V)	High-side Bias Voltage for V-phase	30	IN(LV)	Signal Input for Low-side V-phase
12	VS(V)	High-side Bias Voltage for V-phase GND	31	IN(LW)	Signal Input for Low-side W-phase
14	IN(HW)	Signal Input for High-side W-phase	32	N(W)	Negative Bus Voltage Input for W-phase
15	VCCH(W)	High-side Control Power Supply for W-phase	33	N(V)	Negative Bus Voltage Input for V-phase
16	COM	High-side Control Power Supply GND	34	N(U)	Negative Bus Voltage Input for U-phase
18	VB(W)	High-side Bias Voltage for W-phase	35	W	W-phase Output
19	VS(W)	High-side Bias Voltage for W-phase GND	36	V	V-phase Output
21	VSC	Low-side Sense Current Detection	37	U	U-phase Output
23	VCCL	Low-side Control Power Supply	38	P	Positive Bus Voltage Input

2. Description of Terminology

Table 2-2 Description of terminology (Inverter Block)

Item	Symbol	Description
Zero Gate Voltage Collector Current	I_{CE}	Leakage current when a specified voltage is applied between the collector and emitter of an IGBT with all input signals L (= 0V).
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$ (terminal)	Collector-emitter voltage at a specified collector current when only the input signal of the element under measurement is H (= 5V) and the inputs of all other elements are L (= 0V).
Forward Voltage	V_F	Forward voltage at a specified forward current with all input signals L (= 0V).
Turn-on Time	t_{on}	The time from when the input signal voltage level exceeds the threshold value until the collector current rises to 90% of the rated current. See Fig. 2-2 for details.
Turn-on Delay Time	$t_{d(on)}$	The time from when the input signal voltage level exceeds the threshold value until the collector current rises to 10% of the rated current. See Fig. 2-2 for details.
Turn-on Rise Time	t_r	The time for the collector current to rise from 10% to 90% of the rated current when the IGBT is turned on. See Fig. 2-2 for details.
V_{CE}-I_C Cross Time of Turn-on	$t_{c(on)}$	The time from when the collector current reaches 10% of the rated current until the V_{CE} voltage fall to 10% of the rated voltage when the IGBT is turned on. See Fig. 2-2 for details.
Turn-off Time	t_{off}	The time from when the input signal voltage level falls below the threshold value until the collector current falls to 10% of the rated current. See Fig. 2-2 for details.
Turn-off Delay Time	$t_{d(off)}$	The time from when the input signal voltage level falls below the threshold value until the collector current falls to 90% of the rated current. See Fig. 2-2 for details.
Turn-off Fall Time	t_f	The time for the collector current to fall from 90% to 10% of the rated current when the IGBT is turned off. See Fig. 2-2 for details.
V_{CE}-I_C Cross Time of Turn-off	$t_{c(off)}$	The time from when the V_{CE} voltage reaches 10% of the rated voltage until the collector current fall to 10% of the rated current when the IGBT is turned off. See Fig. 2-2 for details.
Reverse Recovery Time	t_{rr}	The time required to reduce the reverse recovery current of FWD to zero. See Fig. 2-2 for details.

Table 2-3 Description of terminology (Control Circuit Block)

Item	Symbol	Description
Circuit Current of Low-side	I_{CCL}	Consumption current between VCCL and COM.
Circuit Current of High-side	I_{CCH}	Consumption current between VCCH(U, V, W) and COM (for each phase).
Circuit current of Bootstrap circuit	I_{CCHB}	Consumption current between VB(U)-VS(U), VB(V)-VS(V), and VB(W)-VS(W) (for each phase).
Input Signal Threshold Voltage	$V_{th(on)}$	Input signal threshold voltage that turns on the IGBT.*1
	$V_{th(off)}$	Input signal threshold voltage that turns off the IGBT.*1

Table 2-3 Description of terminology (Control Circuit Block) (Continued)

Item	Symbol	Description
Input Signal Threshold Voltage	$V_{th(on)}$	Input signal threshold voltage that turns on the IGBT.*1
	$V_{th(off)}$	Input signal threshold voltage that turns off the IGBT.*1
Input Signal Threshold Hysteresis Voltage	$V_{th(hys)}$	Hysteresis voltage between $V_{th(on)}$ and $V_{th(off)}$.*1
Operational Input Pulse Width of Turn-on	$t_{IN(on)}$	Control signal pulse width required to turn-on the IGBT. Refer to Chapter 3.4 for details.
Operational Input Pulse Width of Turn-off	$t_{IN(off)}$	Control signal pulse width required to turn-off the IGBT. Refer to Chapter 3.4 for details.
Input Current	I_{IN}	Current flowing between IN(HU,HV,HW,LU,LV,LW) and COM.
Input Pull-down Resistance	R_{IN}	Resistance of built-in resistor between IN(HU,HV,HW,LU,LV,LW) and COM. (for each phase).
Fault Output Voltage	$V_{FO(H)}$	VFO output voltage during normal operation (low-side protection function is not activated). External pull-up resistor = 10kΩ.
	$V_{FO(L)}$	VFO output voltage when low-side protection function is activated.
Fault Output Pulse Width	t_{FO}	The period during which VFO continues to output after low-side protection function is activated. Refer to Chapter 3.6 for details.
Overcurrent Protection Voltage Level	$V_{IS(ref)}$	Overcurrent protection threshold voltage of IS. Refer to Chapter 3.5 for details.
Overcurrent Protection Delay Time	$t_{d\ (IS)}$	The time from overcurrent condition is detected until the collector current falls below 50% of rating. Refer to Chapter 3.5 for details.
Overcurrent Trip Level	I_{oc}	The current value that can be detected when a specified sense resistor Rsc is connected between VSC and COM without connecting external shunt resistors to N(U), N(V), and N(W).
Output Voltage of Temperature Sensor	$V_{(temp)}$	TEMP output voltage. Applied to temperature sensor output model. Refer to Fig. 2-3 and Chapter 3.7 for details.
Pull down Resistance of TEMP terminal	$R_{(temp)}$	Resistance value at which the temperature characteristic of TEMP output voltage becomes linear below room temperature.
Overheating Protection Temperature	T_{OH}	Tripping temperature of overheating protection by LVIC. All low-side IGBTs are shut down when the temperature exceeds this threshold. Refer to Figure 2-3 and Chapter 3.8 for details.
T_{OH} Hysteresis	$T_{OH(hys)}$	Hysteresis temperature that does not reset the protection status during overheating protection. Refer to Figure 2-3 and Chapter 3.8 for details. T_{OH} and $T_{OH(hys)}$ are applied to overheating protection model.
V_{CC} Under Voltage Trip Level of Low-side	$V_{CCL(OFF)}$	Tripping voltage of under voltage protection of low-side control power supply. When V_{CCL} falls below the threshold voltage, all low-side IGBTs are shut down. Refer to Chapter 3.1 for details.
V_{CC} Under Voltage Reset Level of Low-side	$V_{CCL(ON)}$	Reset voltage that resets the under voltage protection of low-side control power supply. Refer to Chapter 3.1 for details.
V_{CC} Under Voltage Hysteresis of Low-side	$V_{CCL(hys)}$	Hysteresis voltage between $V_{CCL(OFF)}$ and $V_{CCL(ON)}$,

*1 If the pulse width of the input signal is less than $t_{IN(on)}$ or $t_{IN(off)}$, the product might make incorrect response.

Table 2-3 Description of terminology (Control Circuit Block) (Continued)

Item	Symbol	Description
V_{CC} Under Voltage Trip Level of High-side	$V_{CCH(OFF)}$	Tripping voltage of under voltage protection of high-side control power supply. When $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ falls below the threshold voltage, the corresponding high-side IGBTs are shut down. Refer to Chapter 3.1 for details.
V_{CC} Under Voltage Reset Level of High-side	$V_{CCH(ON)}$	Reset voltage that resets the under voltage protection of high-side control power supply. Refer to Chapter 3.1 for details.
V_{CC} Under Voltage Hysteresis of High-side	$V_{CCH(hys)}$	Hysteresis voltage between $V_{CCH(OFF)}$ and $V_{CCH(ON)}$.
V_B Under Voltage Trip Level	$V_{B(OFF)}$	Tripping voltage of under voltage protection of high-side bias voltage. When $V_{B(U)}$, $V_{B(V)}$, $V_{B(W)}$ falls below the threshold voltage, the corresponding high-side IGBT is shut down. Refer to Chapter 3.2 for details.
V_B Under Voltage Reset Level	$V_{B(ON)}$	Reset voltage that resets the under voltage protection of high-side bias voltage. Refer to Chapter 3.2 for details.
V_B Under Voltage Hysteresis	$V_{B(hys)}$	Hysteresis voltage between $V_{B(OFF)}$ and $V_{B(ON)}$.
Forward Voltage of Bootstrap Diode	$V_{F(BSD)}$	Forward voltage when a specified forward current flows through BSD.
Built-in Limiting Resistance	$R_{(BSD)}$	Built-in current limiting resistor resistance value of bootstrap circuit.

Table 2-4 Description of terminology (Thermal Characteristics)

Item	Symbol	Description
Junction to Case Thermal Resistance (per single IGBT)	$R_{th(j-c)\_IGBT}$	Thermal resistance from junction to case of a single IGBT.
Junction to Case Thermal Resistance (per single Diode)	$R_{th(j-c)\_FWD}$	Thermal resistance from junction to case of a single FWD.

Table 2-5 Description of terminology (Mechanical Characteristics)

Item	Symbol	Description
Mounting Torque of Screws	M_S	Maximum screwing torque when mounting the IPM to a cooling body with specified screws.
Heat-sink Side Flatness	-	Flatness of the IMS's aluminum surface. Refer to Fig. 2-4.
Weight	-	Weight of a single IPM.
Resistance to Soldering Heat	-	Number of times of solder heat resistance under specified conditions.

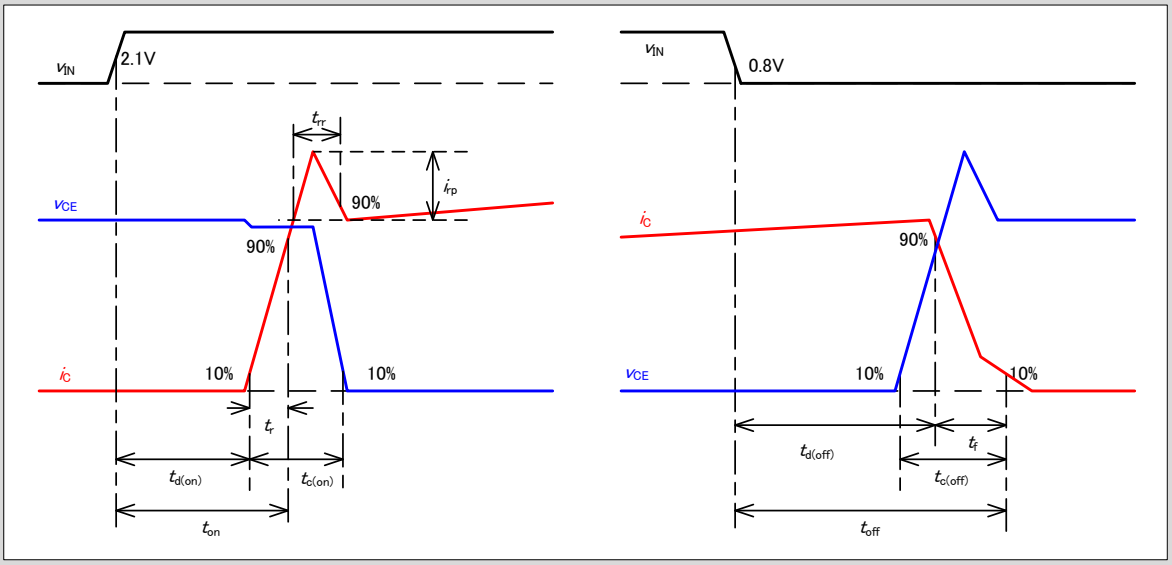


Fig. 2-2 Definition of switching time

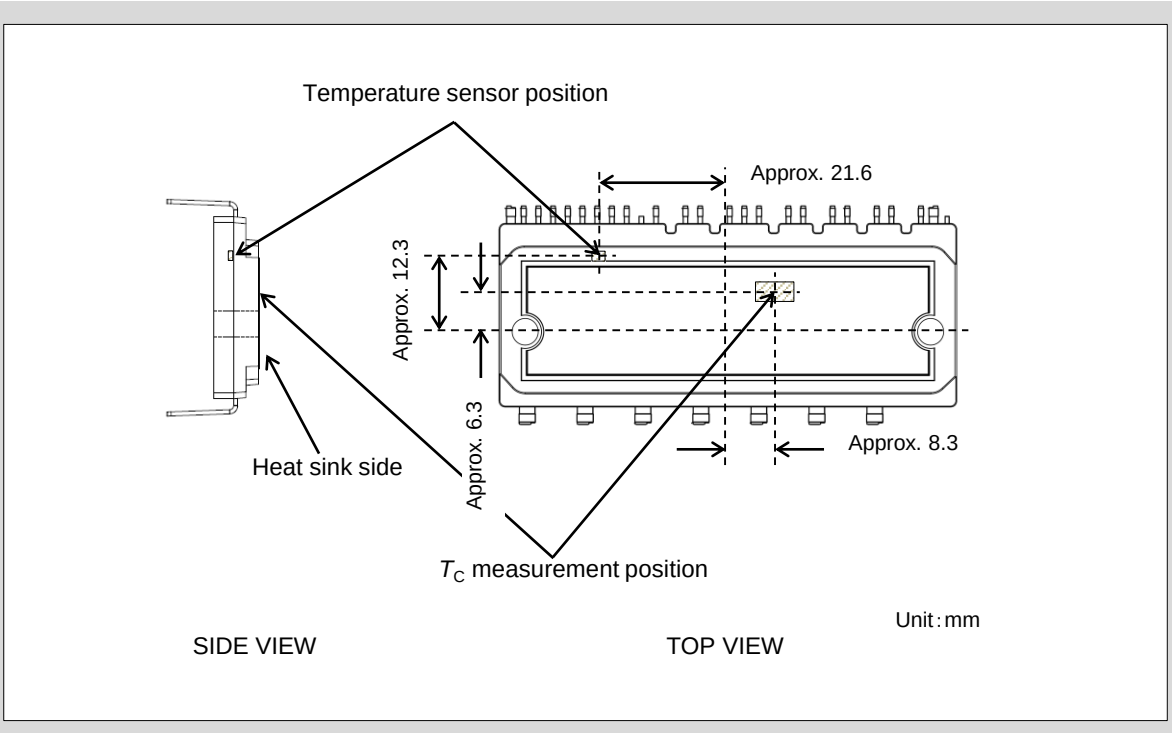


Fig. 2-3 Temperature sensor position and T_c measurement position

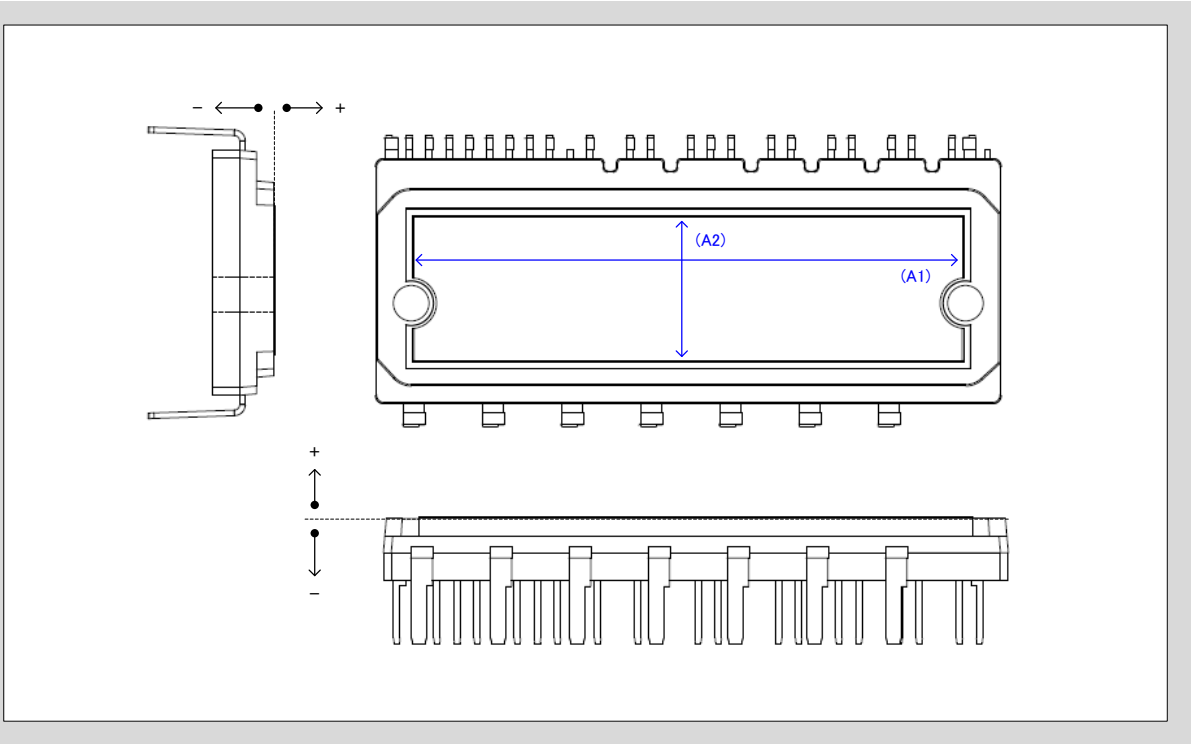


Fig. 2-4 Measurement point of heat sink surface flatness

Chapter 3 Details of Control & Protection Functions

1. Control Power Supply, VCCH(U,V,W), VCCL, COM

<Voltage range of control power supply VCCH(U,V,W), VCCL >

- For control supply voltage, please connect a 15V±10% DC power supply between VCCH(U), VCCH(V), VCCH(W), VCCL and COM terminals.
- Table 3-1 describes the operation of the product for various control supply voltages. A low impedance capacitor and a high frequency decoupling capacitor should be connected close to the terminals of the power supply.
- High frequency noise on the power supply might cause malfunction of the internal control IC or erroneous fault signal output. To avoid these problems, the maximum amplitude of voltage ripple on the power supply should be less than ±1V/μs.
- When connecting external shunt resistor, the potential at the COM terminal is different from that at the N(U, V, W) terminal. Please refer all control circuits and power supplies to the COM terminal and not to the N(U, V, W) terminals. If circuits are improperly connected, current might flow through the shunt resistor and cause improper operation of the short-circuit protection function. In general, it is recommended to set the COM terminal as the ground potential in the PCB layout.
- The control power supply is also connected to the bootstrap circuit which provide floating power supplies for the high-side gate drivers.
- When high-side control power supply voltage $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ falls below $V_{CCH(OFF)}$, only the IGBT which UV protection is triggered is turned-off regardless of input signal condition.
- When low-side control power supply voltage V_{CCL} falls below $V_{CCL(OFF)}$, all low-side IGBTs are turned-off regardless of input signal condition.

Table 3-1 Functions versus supply voltage $V_{CCH(U,V,W)}$, V_{CCL}

Control Voltage Range [V]	Operating state
0 ~ 4	The product does not operate. UV protection and fault output are not activated. d*v*/d*t* noise on the main P-N power supply might cause the IGBTs to malfunction.
4 ~ 13	The product starts to operate. UV protection is activated, control input signals are blocked and fault output is generated.
13 ~ 13.5	UV protection is reset. IGBTs perform switching in accordance to input signal. Drive voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition. High-side IGBTs do not switch until $V_{B(*)}$*1 reaches $V_{B(ON)}$ after initial charging.
13.5 ~ 16.5	Normal operation. This is the recommended operating condition.
16.5 ~ 20	IGBTs perform switching. Because drive voltage is above the recommended range, IGBT's switching is faster and causes an increase in system noise. Even with proper overcurrent protection design, the short-circuit peak current can become very large and might lead to failure.
Over 20	Control circuit in the product might be damaged. It is recommended to insert a Zener diode between each pair of control supply terminals if necessary.

*1 : $V_{B(*)}$ is applied between VB(U)-U, VB(V)-V, VB(W)-W.

<Under voltage (UV) protection of control power supply $V_{CCH(U,V,W)}$, V_{CCL}>

- Fig.3-1 shows the UV protection circuit of VCCH(U,V,W) and VCCL.
- Fig.3-2 and Fig.3-3 shows the operation sequence of UV operation of VCCH and VCCL.
- As shown in Fig.3-1, a diode is connected between VCCH(U,V,W)-COM and VCCL-COM terminals. The diode is connected to protect the product from the input surge voltage. Do not use the diode for voltage clamp purpose otherwise the product might be damaged.

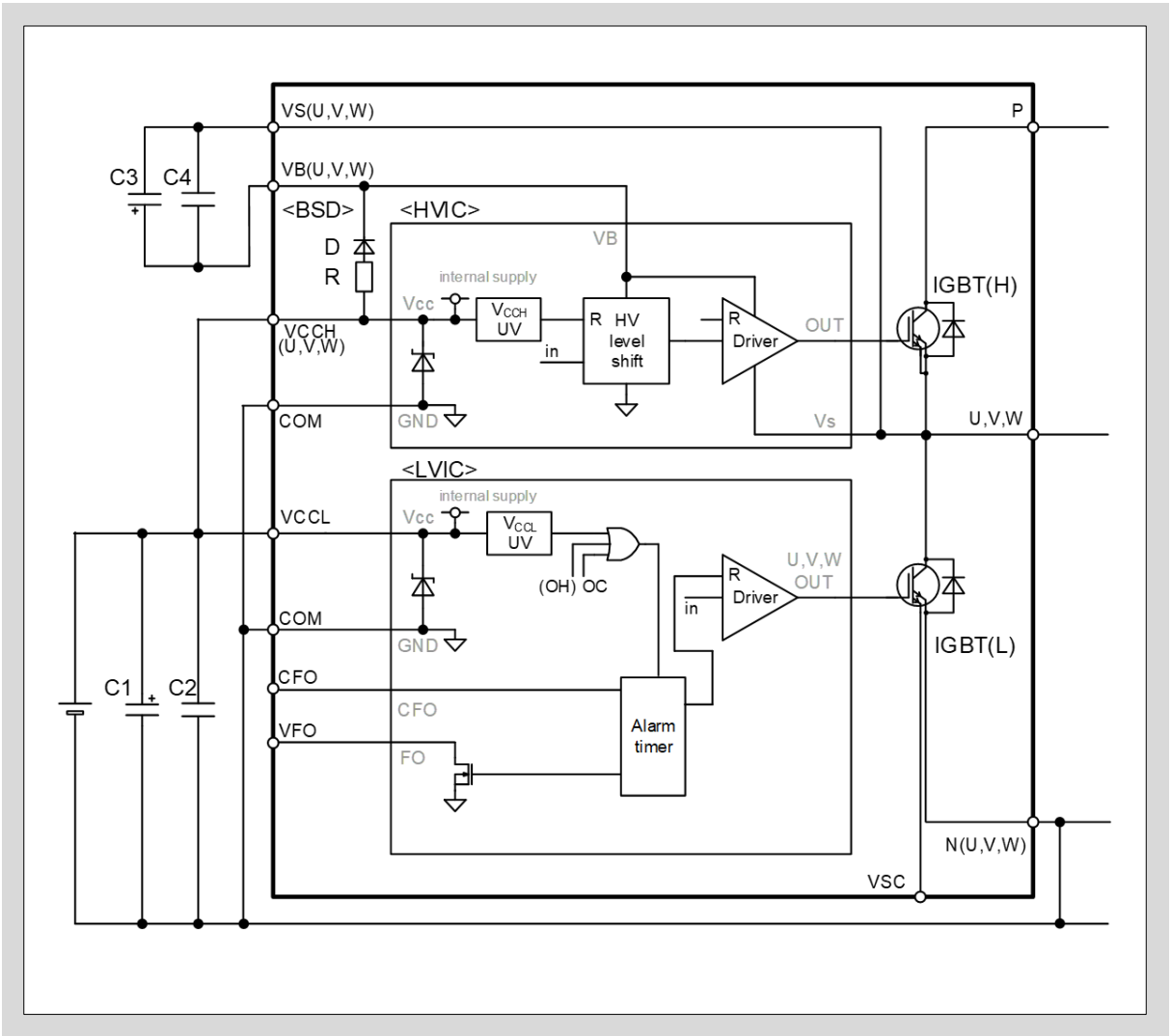


Fig. 3-1 UV protection circuit of high-side and low-side control power supply

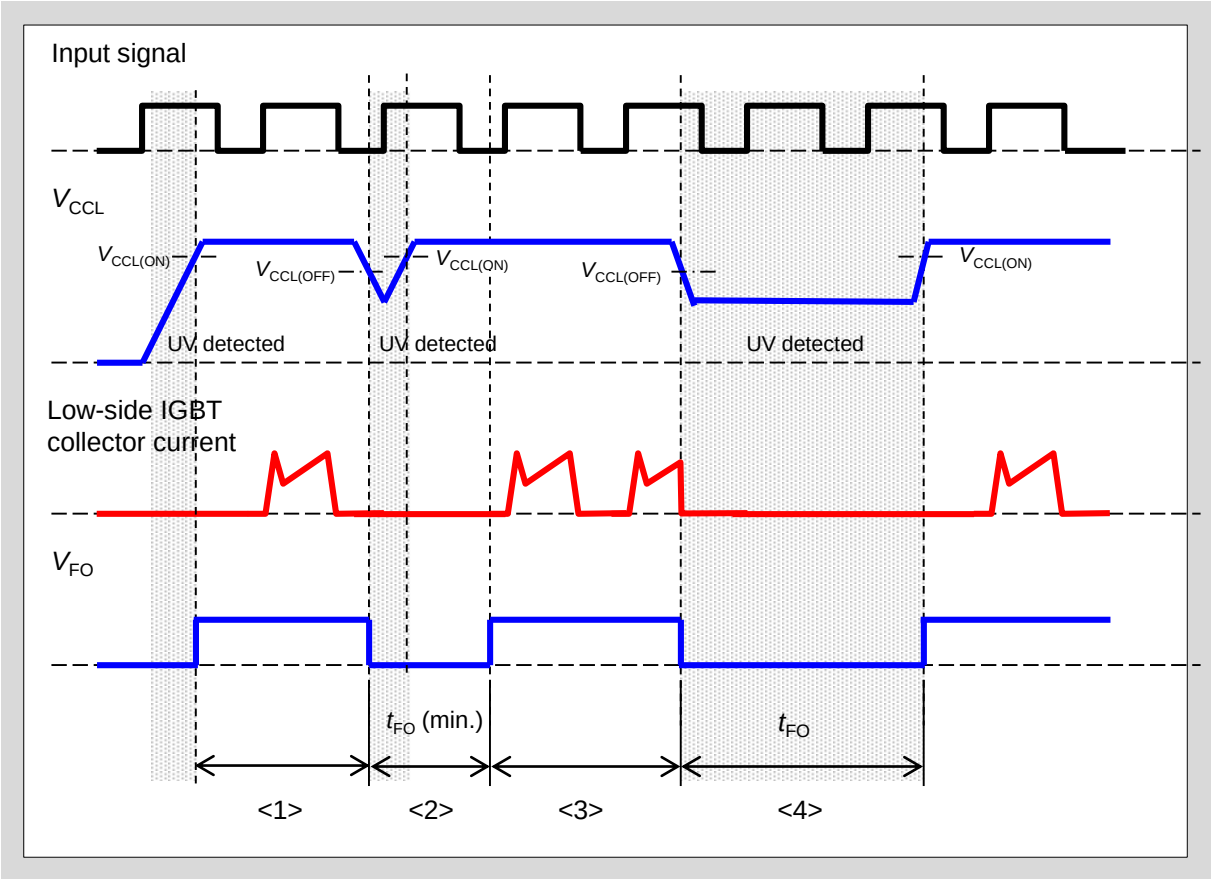


Fig. 3-2 UV protection operation sequence of V_{CCL}

When V_{CCL} is below 4V, UV and fault output are not activated.

<1> When V_{CCL} is lower than $V_{CCL(ON)}$, all lower side IGBTs are OFF state. After V_{CCL} exceeding $V_{CCL(on)}$, the fault output V_{FO} is released (high level). And the LVIC stars to operate, then next input is activated.

<2> The fault output V_{FO} is activated when V_{CCL} falls below $V_{CCL(OFF)}$, and all lower side IGBT remains OFF state. If the voltage drop time is less than $t_{FO(min)}$, the minimum pulse width of the fault output signal is $t_{FO(min)}$ and all lower side IGBTs are OFF state regardless of the input signal condition.

<3> UV protection is reset after t_{FO} and V_{CCL} exceeding $V_{CCL(ON)}$, then the fault output V_{FO} is reset simultaneously. After that the LVIC starts to operate from the next input signal.

<4> When the voltage drop time is more than t_{FO}, the fault output pulse width is generated and all lower side IGBTs are OFF state regardless of the input signal condition during the same time.

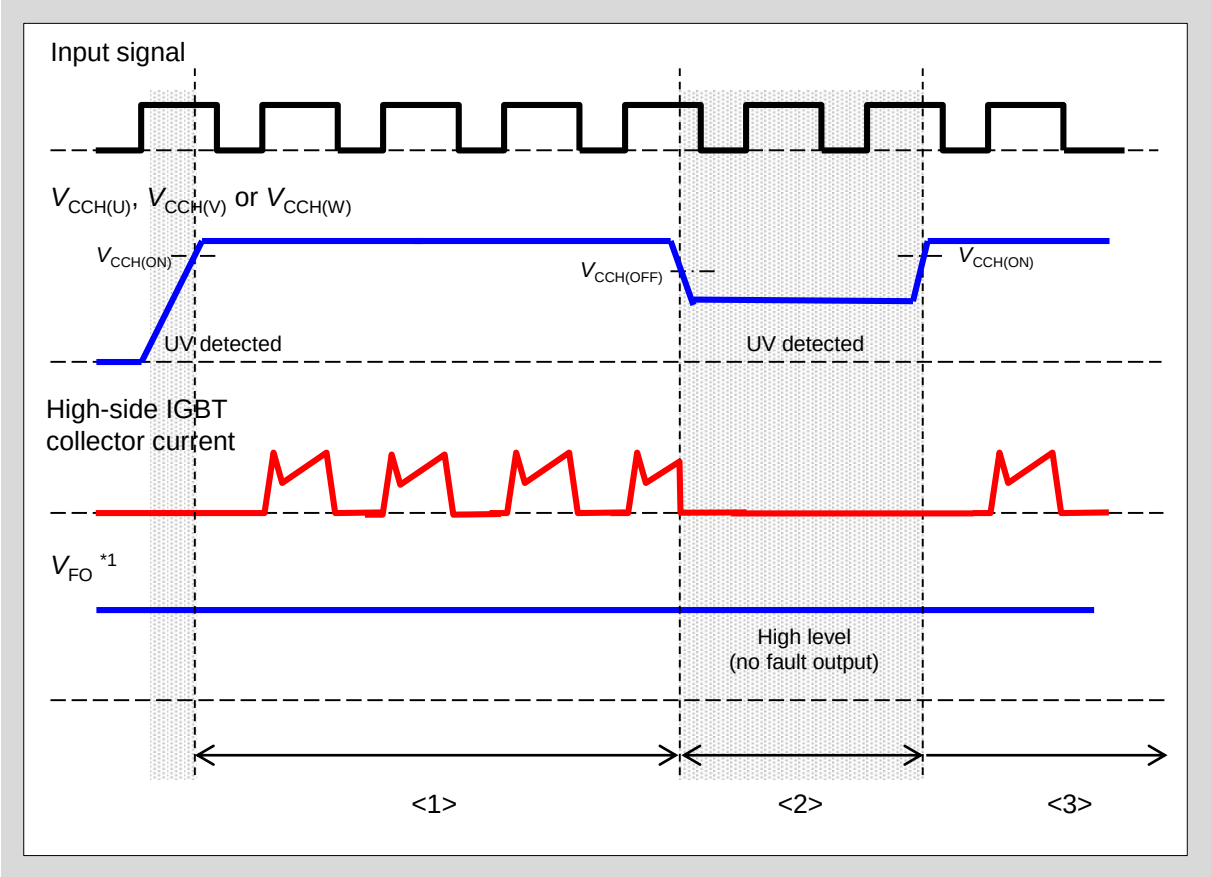


Fig. 3-3 UV protection operation sequence of $V_{CCH(U,V,W)}$

<1> When $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ is lower than $V_{CCH(ON)}$, the upper side IGBT is OFF state. After $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ exceeds $V_{CCH(ON)}$, the HVIC starts to operate from the next input signals. The fault output V_{FO} is constant (high level) regardless of $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$. *1

<2> After $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ falls below $V_{CCH(OFF)}$, the upper side IGBT remains OFF state. But the fault output VFO keeps high level.

<3> The HVIC starts to operate from the next input signal after UV is reset.

*1 : The fault output does not depend on the bias condition of the HVIC.

2. Power Supply Terminals of High-Side VB(U,V,W), VS(U,V,W)

<Voltage range of high-side bias voltage for IGBT driving terminals $V_{B(*)}$>

- The $V_{B(*)}$ voltage, which is the voltage difference between VB(U,V,W) and VS(U,V,W), provides the power supply to the HVICs within the product. This power supply must be in the range of 13.0~18.5V to ensure that the HVICs can fully drive the high-side IGBTs.
- The product includes UV protection for $V_{B(*)}$ to ensure that the HVICs do not drive the high-side IGBTs when $V_{B(*)}$ drops below a specified voltage.
- This function prevents the IGBT from operating in a high dissipation mode. Please note that the UV protection only works on the triggered phase and doesn't generate fault output.
- Conventionally, three isolated power supplies are necessary for IGBT drive at the high-side. In case of using bootstrap circuit, the IGBT drive power supply for high-side can be generated from the high-side/low-side control power supply.
- The power supply of the high-side is charged when the low-side IGBT is turned on or when freewheel current flows through the low-side FWD. Table 3-2 describes the operation of the product for various control supply voltages. The control supply should be well filtered with a low impedance capacitor and a high frequency decoupling capacitor connected close to the terminals in order to prevent malfunction of the internal control IC caused by a high frequency noise on the power supply.
- When $V_{B(*)}$ falls below $V_{B(OFF)}$, only the triggered phase IGBT is off-state even though the input signal is provided.

Table 3-2 Functions versus high side bias voltage for IGBT driving $V_{B(*)}$

Control Voltage Range [V]	Operations and functions
0 ~ 4	HVICs are not activated. UV does not operate. d*v*/d*t* noise on the main P-N power supply might cause the IGBTs to malfunction.
4 ~ 12.5	HVICs start to operate. As the UV is activated, control input signals are blocked.
12.5 ~ 13	UV is reset. The high-side IGBTs perform switching in accordance to input signal. Driving voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition.
13 ~ 18.5	Normal operation. This is the recommended operating condition.
18.5 ~ 20	The high-side IGBTs perform switching. Because drive voltage is above the recommended range, IGBT's switching is faster and causes an increase in system noise. Even with proper overcurrent protection design, the short-circuit peak current can become very large and might lead to failure.
Over 20	Control circuit in the product might be damaged. It is recommended to insert a Zener diode between each pair of high-side power supply terminals.

<Under voltage (UV) protection of high-side bias voltage $V_{B(*)}$>

- Fig.3-4 shows the UV protection circuit of high-side bias voltage $V_{B(*)}$.
- Fig.3-5 shows the UV protection operation sequence of $V_{B(*)}$.
- As shown in Fig.3-4, diodes are connected to the VB(U,V,W), VS(U,V,W) and VB(U,V,W)-COM terminals. These diodes protect the product from input surge voltage. Do not use these diodes for voltage clamp purpose otherwise the product might be damaged.

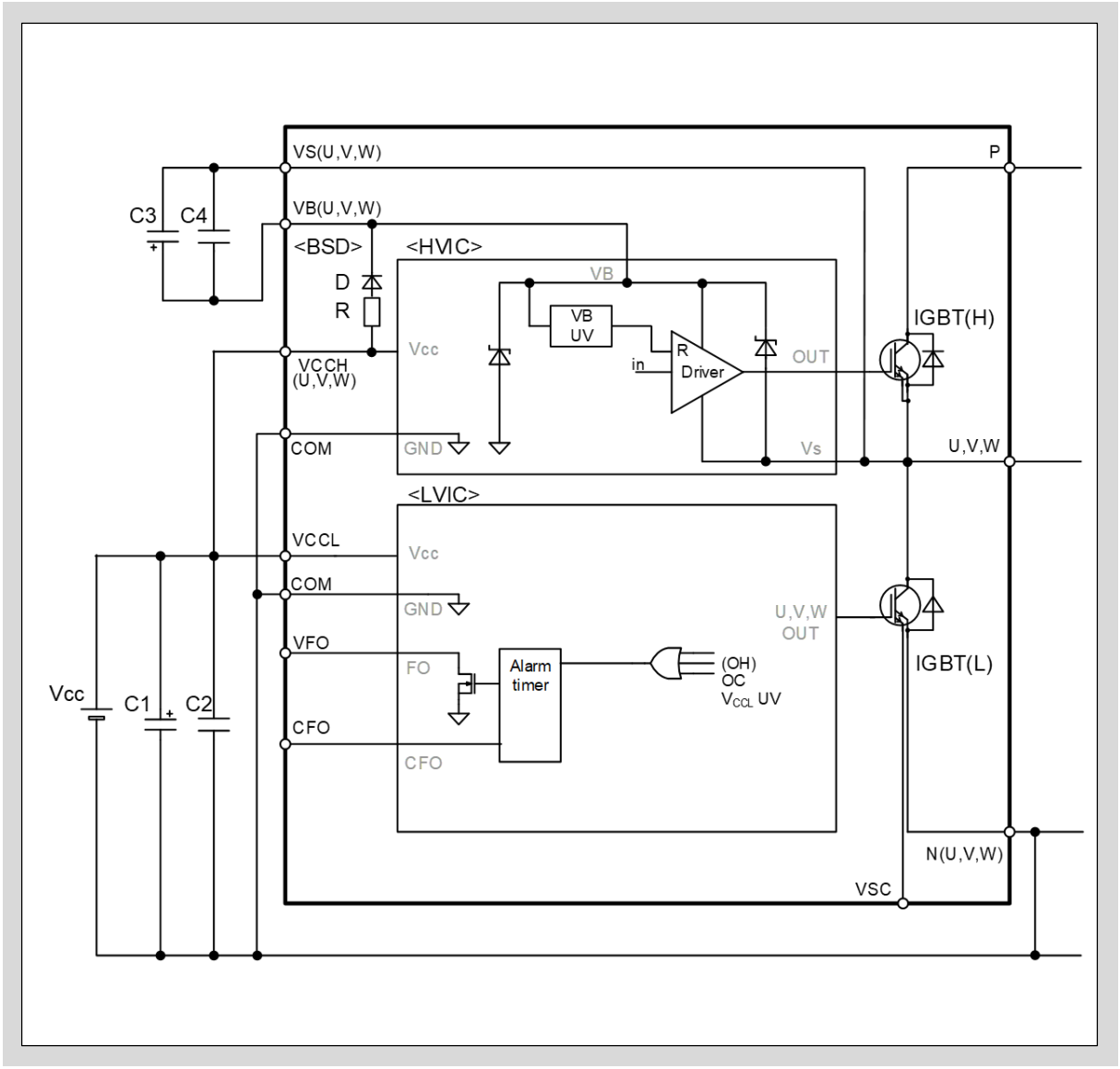


Fig. 3-4 UV protection circuit of high-side bias voltage

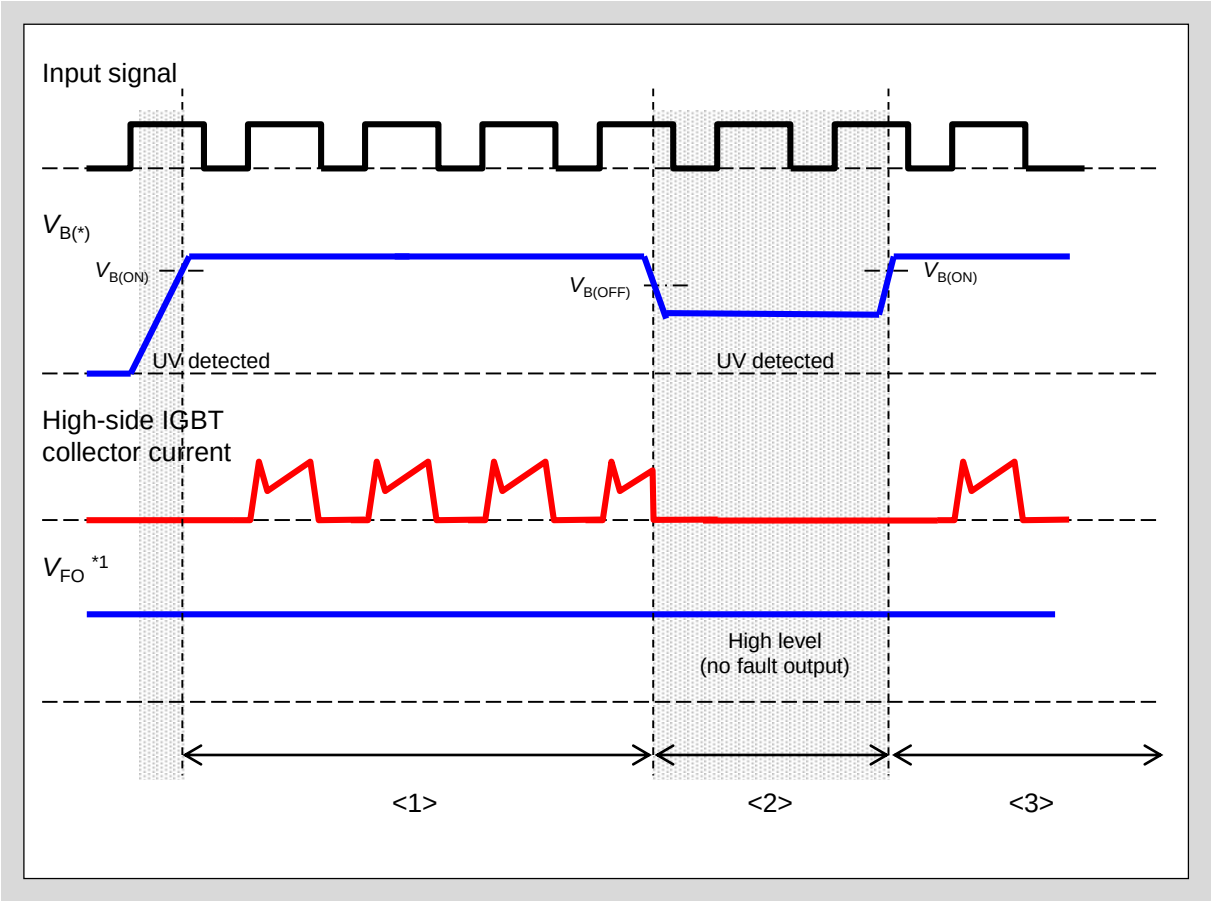


Fig. 3-5 UV protection operation sequence of $V_{B(*)}$

<1> When $V_{B(U)}$, $V_{B(V)}$ or $V_{B(W)}$ is below $V_{B(ON)}$, the corresponding high-side IGBT is OFF.
When $V_{B(*)}$ exceeds $V_{B(ON)}$, HVIC starts switching operation from the next input signal.
The fault output voltage V_{FO} is H level regardless of $V_{B(*)}$. *1

<2> When $V_{B(U)}$, $V_{B(V)}$ or $V_{B(W)}$ falls below $V_{B(OFF)}$, the corresponding high-side IGBT is turned off.
The fault output voltage V_{FO} remains at H level.

<3> After UV protection is reset, HVIC restarts switching operation from the next input signal.

*1 : The fault output does not depend on the bias condition of the HVIC.

3. Function of Built-in BSDs (Bootstrap Diodes)

There are several ways to generate high-side bias voltage $V_{B(*)}$ (VB(U)-VS(U), VB(V)-VS(V), VB(W)-VS(W) voltage). This product can configure a bootstrap circuit by using the built-in BSDs. When configuring the bootstrap circuit, it is necessary to set the duty ratio and on-time according to the bootstrap capacitor and the charging operation conditions.

<Bootstrap circuit operation>

When low-side IGBT is ON, the high-side bias voltage $V_{B(*)}(t1)$ from the charging operation of the bootstrap capacitor can C3 be expressed by the following equations. Fig.3-6 shows the circuit diagram of charging operation, and Fig.3-7 shows the timing chart.

$V_{B(*)}(t1) = V_{CC}-V_{F(D)}-V_{CE(sat)}-I_B \cdot R$ …… transient state
$V_{B(*)}(t1) \approx V_{CC}$ …….. steady state
$V_{F(D)}$: Forward voltage of BSD
$V_{CE(sat)}$: Saturation voltage of low-side IGBT
R : Bootstrap circuit resistance
I_B : Charging current of bootstrap circuit

When low-side IGBT is turned off, the motor current flows to the high-side FWD. When the V_S potential rises above V_{CC}, the charging of C3 stops, and $V_{B(*)}$ gradually decreases due to current consumption by the high-side control power supply.

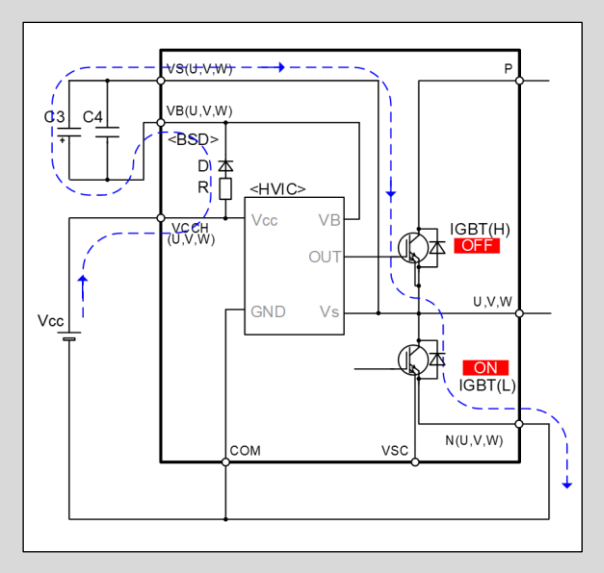


Fig. 3-6 Circuit diagram of charging operation when low-side IGBT is ON

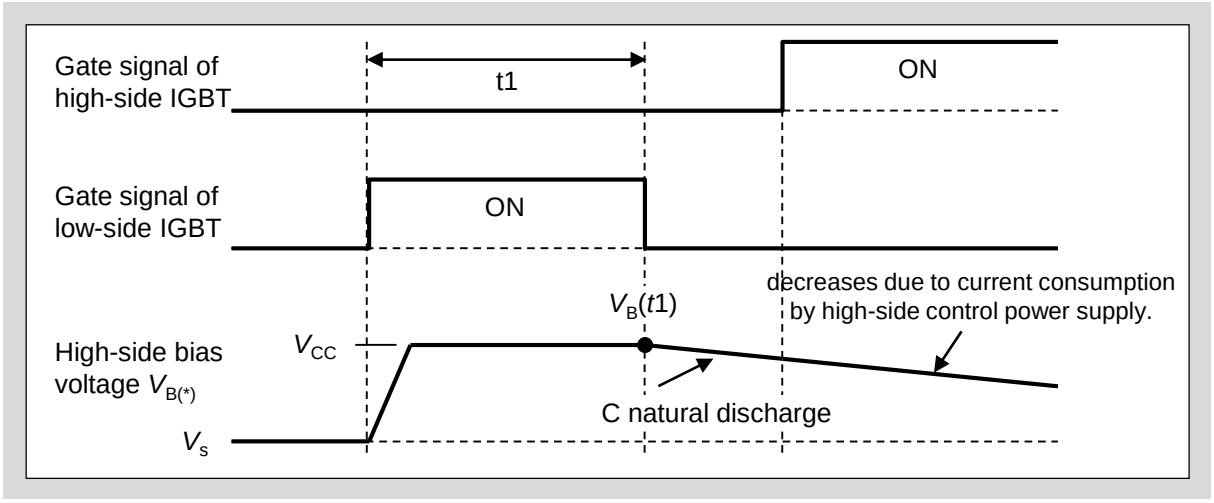


Fig. 3-7 Timing chart of charging operation when low-side IGBT is ON

When low-side IGBT is OFF and low-side FWD is ON, freewheel current flows through the low-side FWD. The high-side bias voltage $V_{B(*)}(t2)$ from the charging operation of the bootstrap capacitor can be expressed by the following equations. Fig.3-8 shows the circuit diagram of charging operation, Fig.3-9 shows the timing chart, and $V_{B(*)}(t2)$ can be expressed by the following equations

$V_{B(*)}(t2) = V_{CC}-V_{F(D)}+V_{F(FWD)}-I_B \cdot R$ … transient state
$V_{B(*)}(t2) \approx V_{CC}$ … steady state

$V_{F(D)}$: Forward voltage of BS
$V_{F(FWD)}$: Forward voltage of low-side FWD
R : Bootstrap circuit resistance
I_B : Charging current of bootstrap circuit

When both the low-side and high-side IGBTs are OFF, the regenerative current flows through the low-side FWD. Therefore, the V_S potential drops to $-V_F$ of FWD, and the bootstrap capacitor is recharged. When the high-side IGBT is turned on and the V_S potential rises above V_{CC}, the charging of C3 stops, and $V_{B(*)}$ gradually decreases due to current consumption by the high-side control power supply.

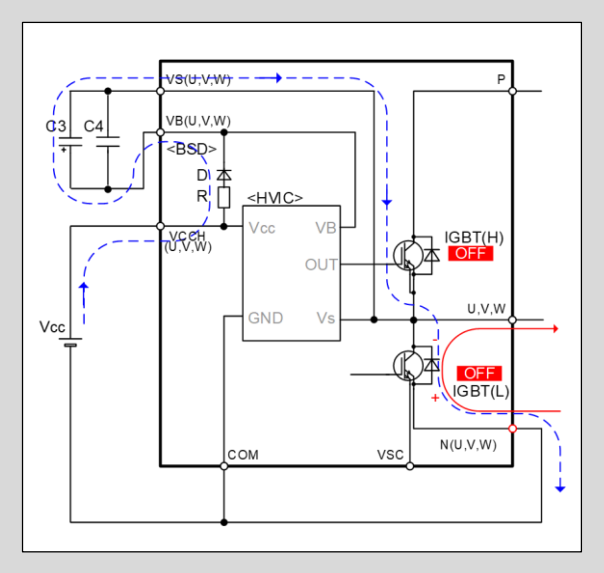


Fig. 3-8 Circuit diagram of charging operation when low-side FWD is ON

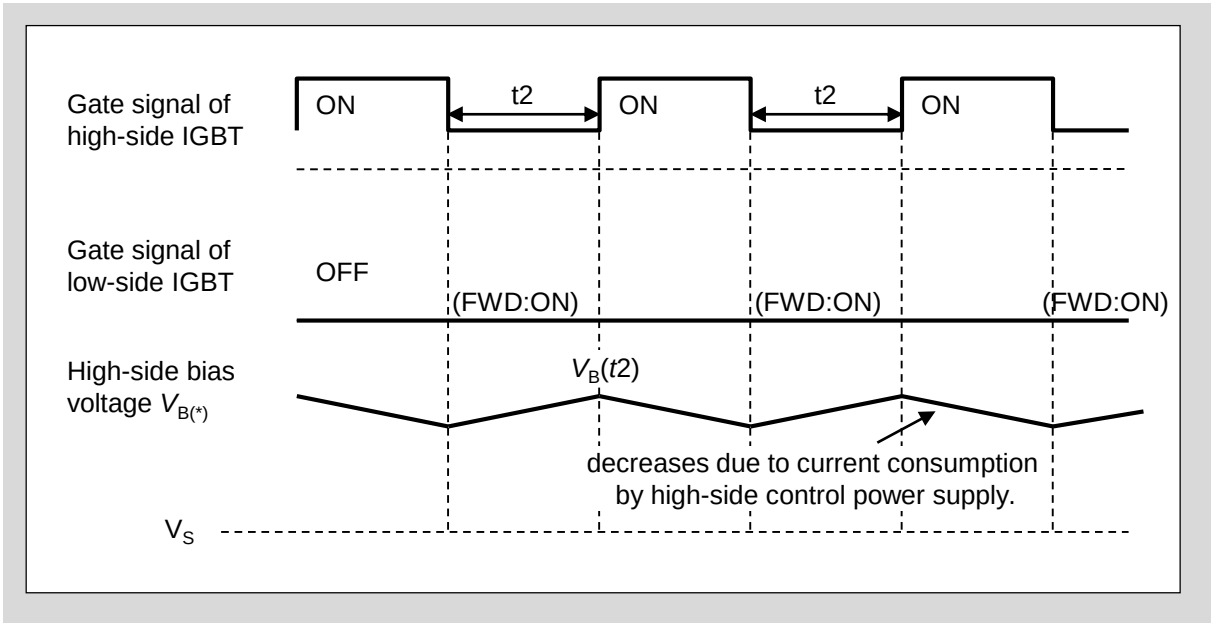


Fig. 3-9 Timing chart of charging operation when low-side FWD is ON

<Setting the bootstrap capacitance and minimum ON/OFF pulse width>

The bootstrap capacitance can be determined by the following equation:

$$C = I_{CCHB} \cdot \frac{t1}{dV}$$

* $t1$: the maximum ON pulse width of the high-side IGBT
* I_{CCHB} : consumption current of high-side drive power supply (temperature and frequency dependent)
* dV : allowable discharge voltage of $V_{B(*)}$ (refer to Fig.3-10)

- Certain margin should be added to the calculated capacitance. In general, select a capacitor that is two to three times of the calculated result.
- The recommended minimum ON pulse width ($t2$) of the low-side IGBT should be determined such that the time constant $R \cdot C$ will enable the discharged voltage (dV) to be fully recharged again during the ON period.
- In the case of the control mode which only the high-side IGBT performs switching operation (Fig. 3-10), the time constant should be set so that the discharged voltage can be fully recharged again during the high-side IGBT OFF (low-side FWD ON) period.
- The minimum pulse width is decided by the minimum ON pulse width of the low-side IGBT, or the minimum OFF pulse width of the high-side IGBT, whichever is longer.

$$t2 \geq \frac{R \cdot C \cdot dV}{V_{CC} - V_B(\min)}$$

* $t2$: Minimum ON pulse width of low-side IGBT
* R : Bootstrap circuit resistance $\Delta R_{F(BSD)}$
* C : Bootstrap capacitance
* dV : Allowable discharge voltage of $V_{B(*)}$
* V_{CC} : Voltage of high-side, low-side control power supply (ex.15V)
* V_B(min) : Minimum voltage of high-side bias voltage (add margin to $V_{B(ON)}$, ex.14V)

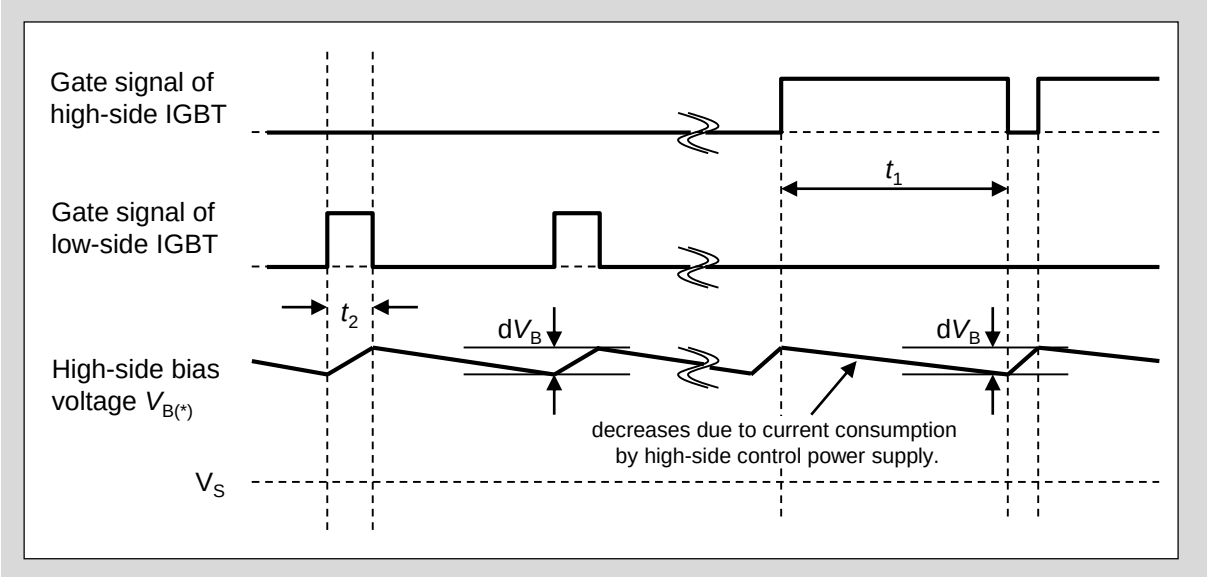


Fig. 3-10 Timing chart of charging and discharging operation

<Setting the initial charging of bootstrap capacitor>

- Initial charging of the bootstrap capacitor is required to start the inverter.
- The pulse width or the number of pulses should be long enough to fully charge the bootstrap capacitor.
- For reference, it takes about 10ms to charge a 47uF capacitor through the built-in bootstrap diode.

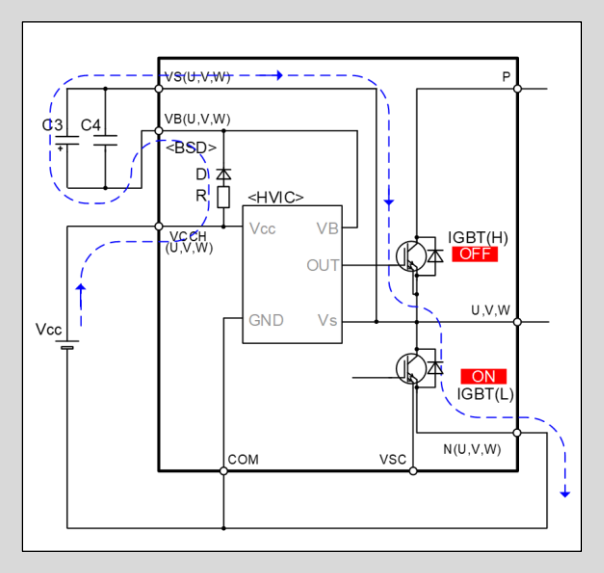


Fig. 3-11 Circuit diagram of initial charging operation

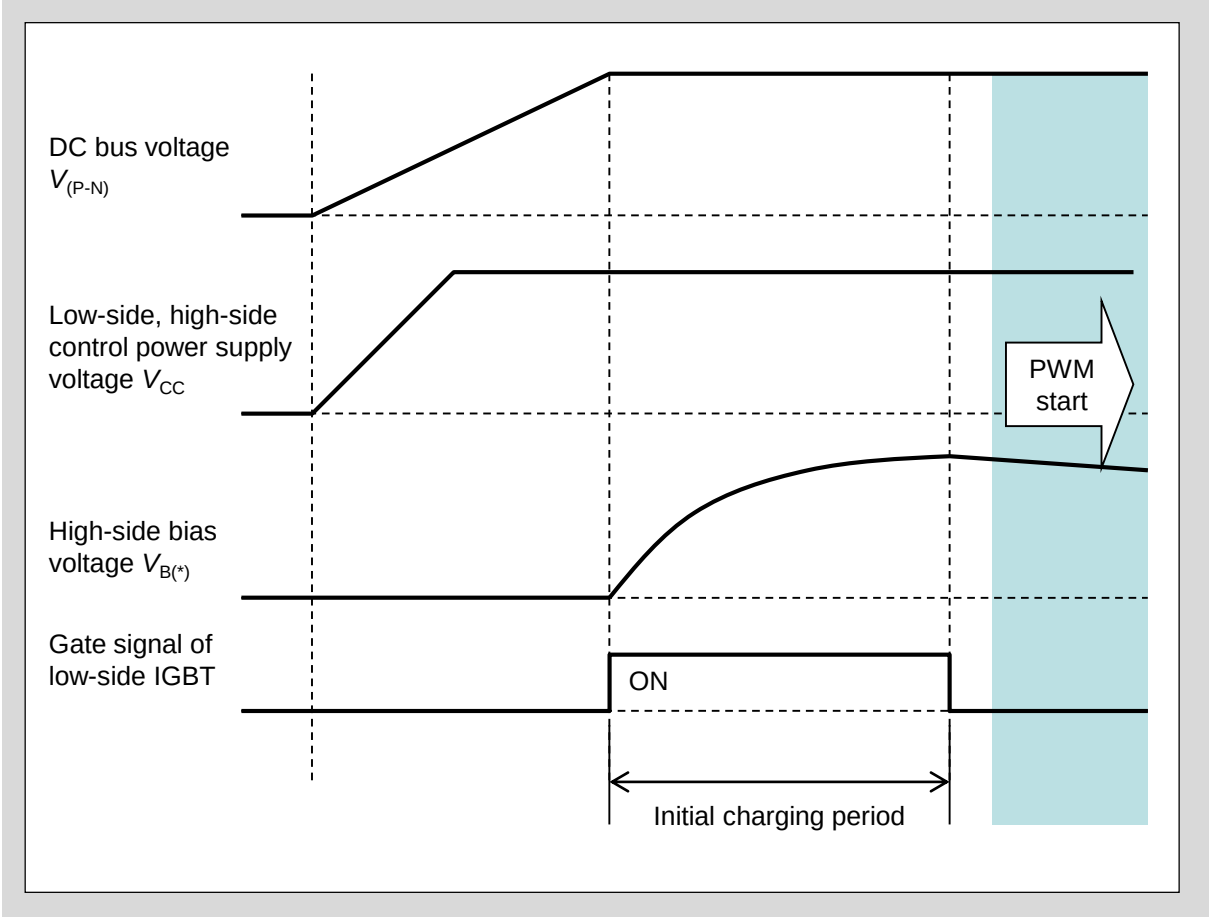


Fig. 3-12 Timing chart of initial charging operation

<BSD built-in current limiting resistance characteristic>

The bootstrap diode has built-in current limiting resistor of 20Ω (typ.). Fig. 3-13 and Fig. 3-14 show the V_F-I_F characteristics of the bootstrap diode.

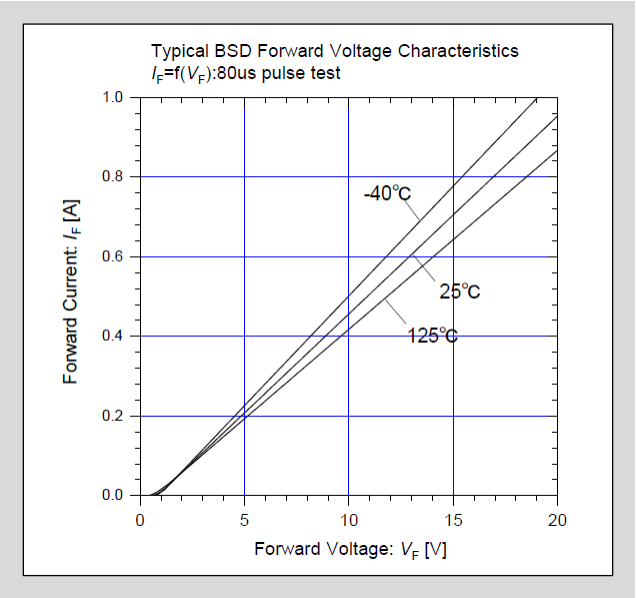


Fig. 3-13 V_F-I_F characteristic of BSD

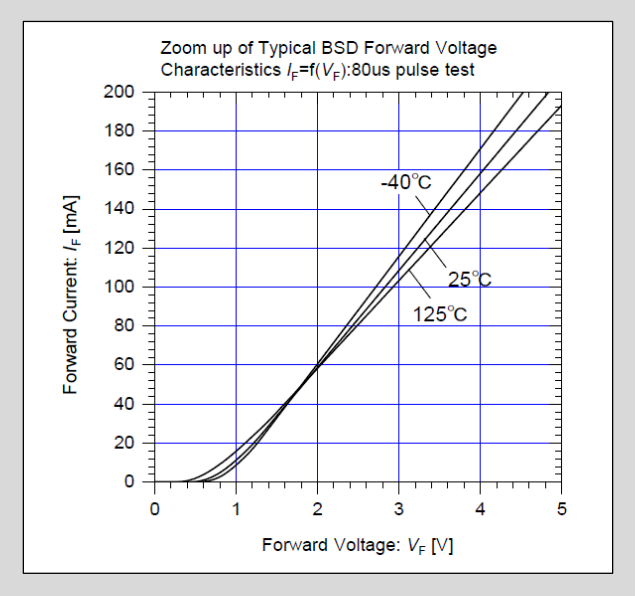


Fig. 3-14 V_F-I_F characteristic of BSD (zoom at low current range)

4. Signal Input, IN(HU,HV,HW), IN(LU,LV,LW)

<Input terminals connection>

- Fig. 3-15 shows an example of interface circuit between MPU and the product. The input terminals can be connected directly to the MPU. The input terminals have built-in pull-down resistors, so there is no need for external pull-down resistors. Also, the input logic is high active, thus there is no need for external pull-up resistors.
- Insert RC filter circuit as shown by the dotted line in Fig. 3-15 if noise is superimposed on long signal wire. Adjust the RC constant according to the PWM control method and the wiring pattern of the printed circuit board.

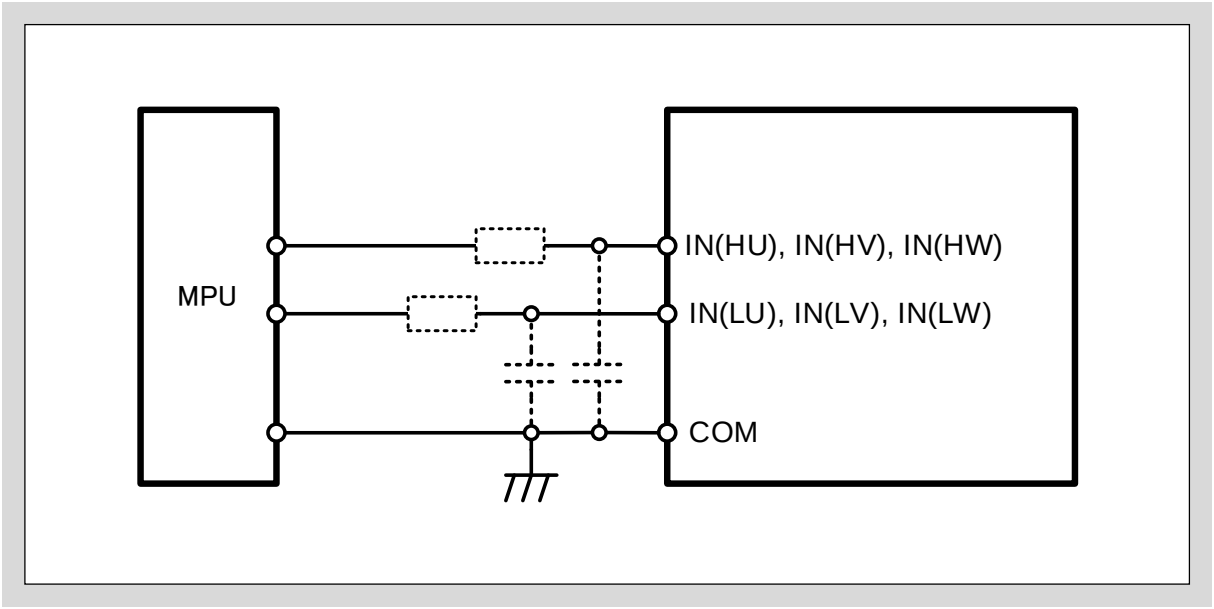


Fig. 3-15 Recommended MPU I/O interface circuit of IN(HU,HV,HW), IN(LU,LV,LW) terminals

<Input terminals circuit>

- The input logic of this product is high active. Thus, the input signal has no restriction on the power supply startup and shutdown sequence, so the system is fail safe. In addition, as shown in Fig. 3-16, the input terminals have built-in pull-down resistors, thus there is no need for external pull-down resistors, reducing the number of system components. Furthermore, a 3.3V-class MPU can be connected directly since the input signal threshold voltage is low.
- In the case of connecting an external filter resistor between the MPU and the input terminal of the product, make sure that the input terminal voltage is above the input signal threshold voltage in consideration of the built-in pull-down resistor.
- As shown in Fig.3-16, diodes are connected to the VCCL-IN(HU,HV,HW,LU,LV,LW) and IN(HU,HV,HW,LU,LV,LW)-COM terminals. These diodes are built-in to protect the product from input surge voltage. Do not use these diodes for voltage clamp purpose as it might damage the product.

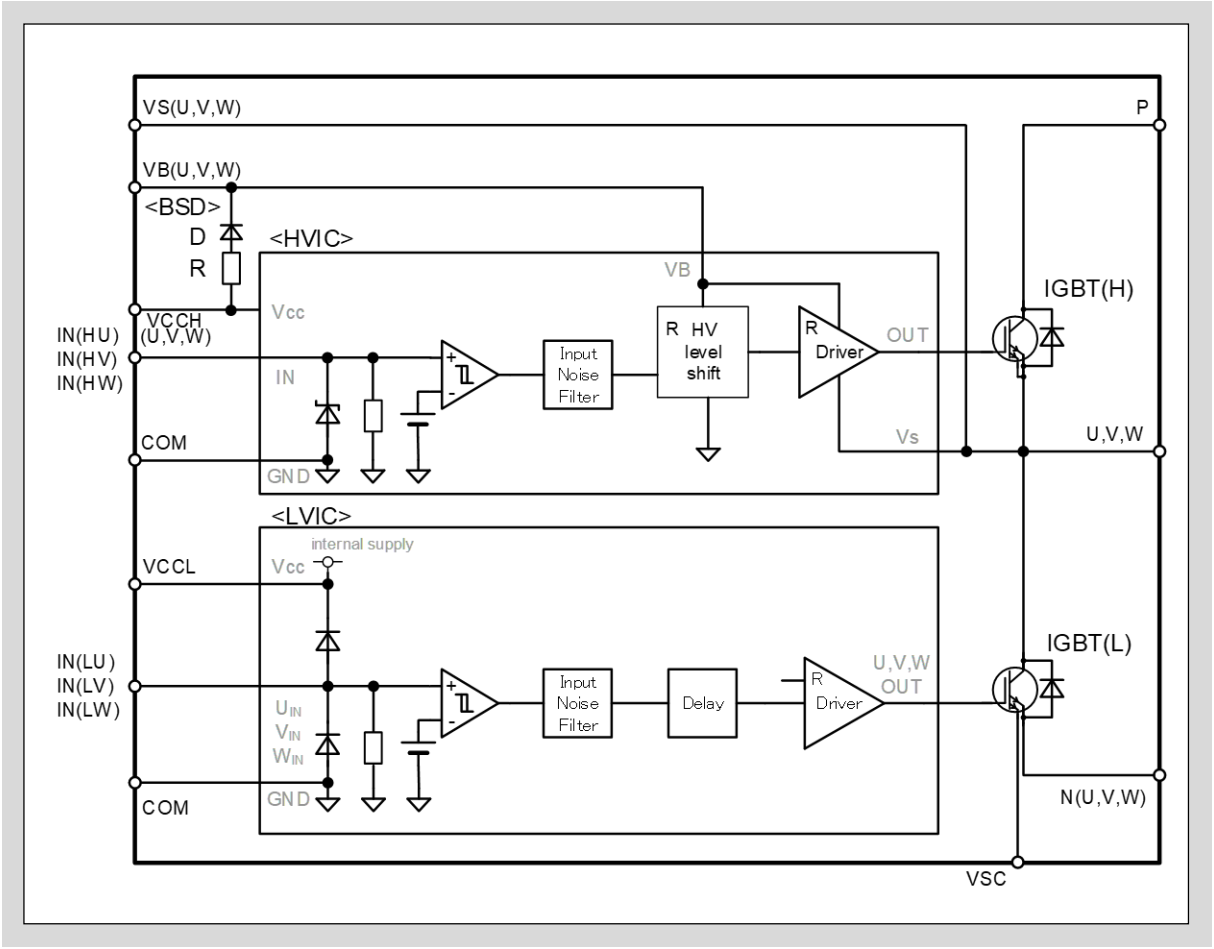


Fig.3-16 Circuit of IN(HU,HV,HW), IN(LU,LV,LW) terminals

<IGBT drive state and input signal pulse width>

$t_{IN(on)}$ is the recommended minimum ON pulse width required to turn-on the IGBT without malfunction, and $t_{IN(off)}$ is the recommended minimum OFF pulse width required to turn-off the IGBT without malfunction. Fig. 3-17 and Fig. 3-18 show the IGBT drive state at various input signal pulse width.

A : IGBT might turn-on even when the input signal ON pulse width is less than minimum $t_{IN(on)}$. In the case of input signal ON pulse width is less than minimum $t_{IN(on)}$ and a voltage below -5V is applied between U-COM, V-COM, W-COM terminals, not only the product might be broken but also the IGBT might not turn-off due to malfunction of the control circuit.

B : In steady state operation. IGBT operates in the linear region.

C : IGBT might turn-off even when the input signal OFF pulse width is less than minimum $t_{IN(off)}$. In the case of input signal OFF pulse width is less than minimum $t_{IN(off)}$ and a voltage below -5V is applied between U-COM, V-COM, W-COM terminals, not only the product might be broken but also the IGBT might not turn-on due to malfunction of the control circuit.

D : In steady state operation. IGBT is completely turned off.

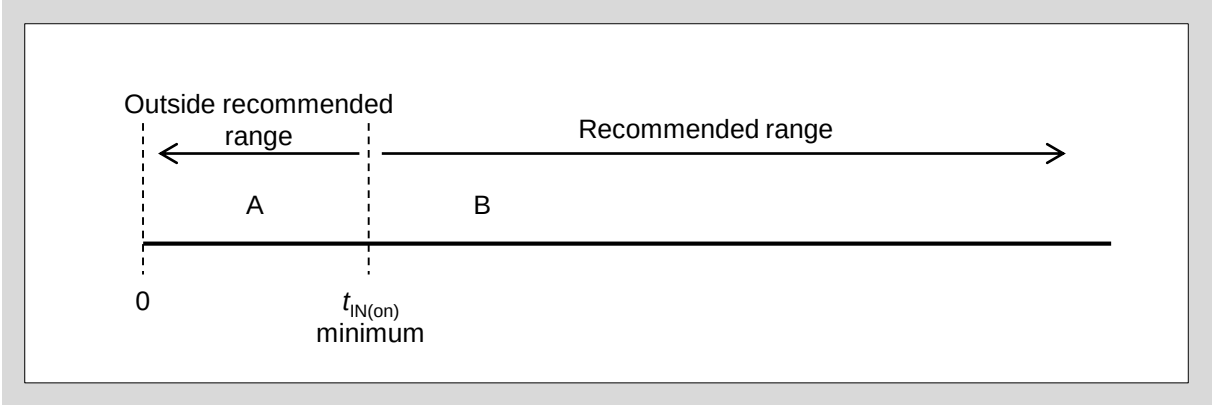


Fig. 3-17 IGBT drive state versus input signal ON pulse width

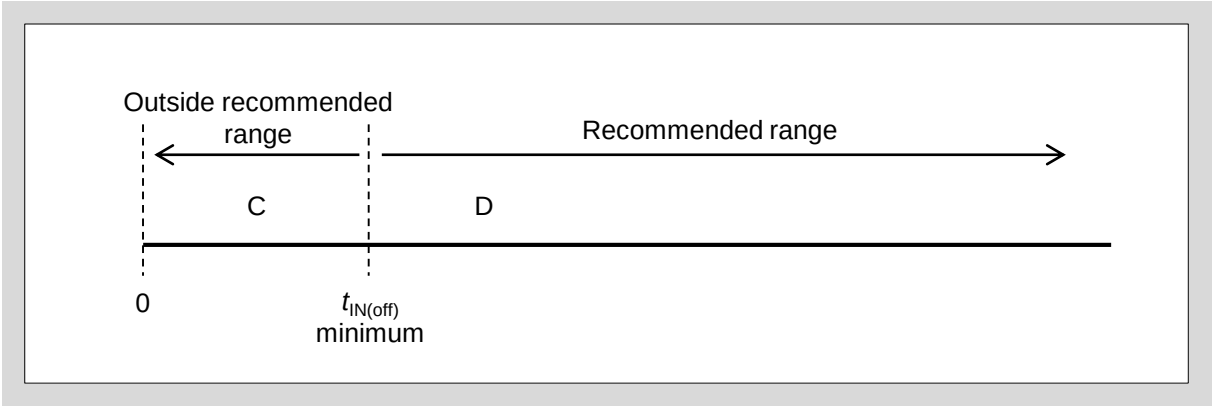


Fig. 3-18 IGBT drive state versus input signal OFF pulse width

5. Overcurrent Protection Function, IS

- The overcurrent (OC) protection works by detecting the voltage generated at the external shunt resistor connected between N(U,V,W) and COM terminal, or the voltage generated at the sense resistor connected between VSC and COM terminal, and input to IS terminal. When this voltage exceeds $V_{IS(ref)}$, all low-side IGBTs are turned-off and fault output is generated.
- Fig. 3-19 shows the OC protection detection circuit of IS terminal. Fig. 3-20 shows the OC protection operation sequence.
- To prevent the product from unnecessary operations due to switching noise or recovery current during normal operation, it is recommended to insert an external RC filter (time constant is approximately 1.1μs) to the IS terminal. Keep the wiring between the product and the shunt resistor as short as possible.
- As shown in Fig. 3-19, diodes are connected between VCCL-IS and IS-COM terminals. These diodes are built-in to protect the product from input surge voltage. Do not use these diodes for voltage clamp purpose as it might damage the product.

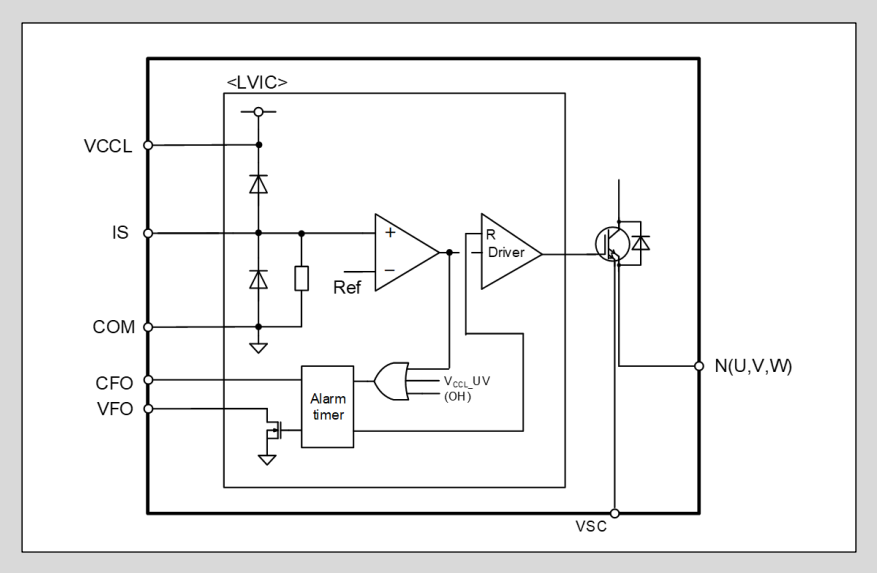


Fig. 3-19 OC protection detection circuit of IS terminal

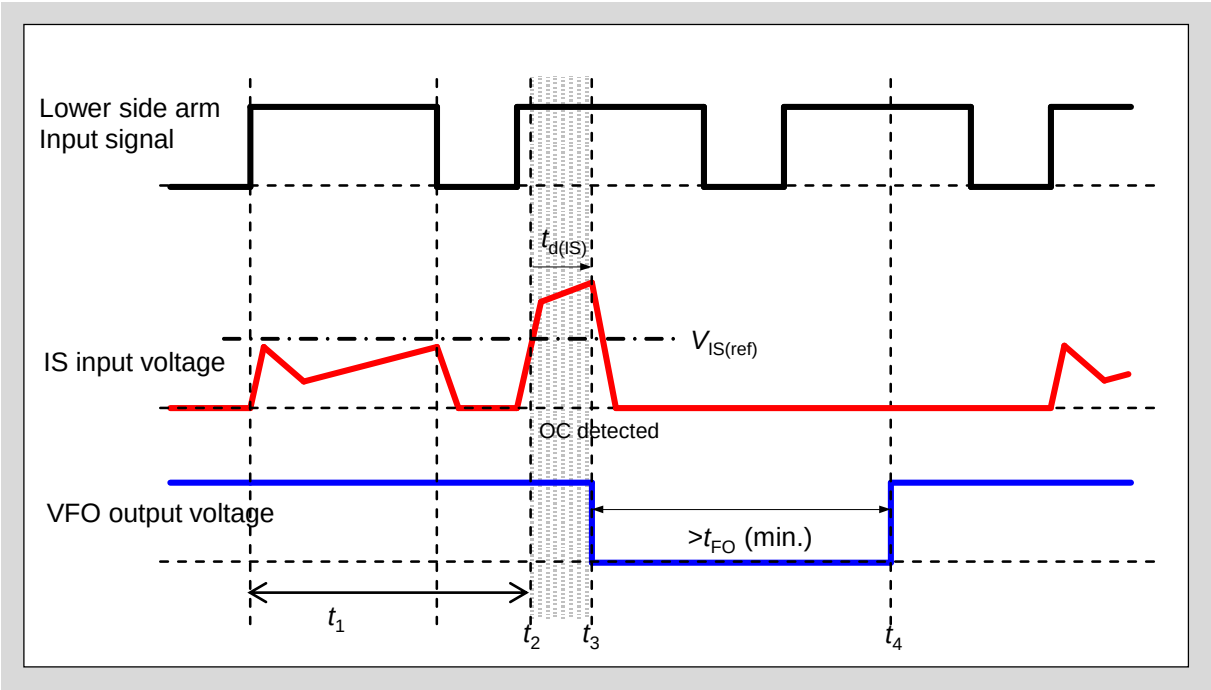


Fig. 3-20 OC protection operation sequence

*t*1: The IS input voltage is less than $V_{IS(ref)}$. All low-side IGBTs perform normal switching operation.

*t*2 :When IS input voltage exceeds $V_{IS(ref)}$, OC is detected.

*t*3: Fault output voltage is generated and all low-side IGBTs are turned off after the overcurrent protection delay time $t_{d(IS)}$. Propagation delay of LVIC is included in $t_{d(IS)}$.

*t*4: OC protection is reset after t_{FO}. LVIC restarts switching operation from the next input signal.

6. Fault Status Output Function, VFO, CFO

- As shown in Fig. 3-21, it is possible to connect the fault status output terminal VFO directly to the MPU.
- The VFO terminal is open drain configured, thus this terminal should be pulled up to 5V or 3.3V DC logic power supply with a 10kΩ resistor. It is also recommended to connect a bypass capacitor C1 and inrush current limiting resistor R1 of 5kΩ or more between the MPU and the VFO terminal. These signal lines should be as short as possible.
- VFO terminal generates fault status output during UV protection of VCCL, OC protection, and OH protection. (OH protection is built into “6MBP ** XTC065-50”)
- The pulse width of the fault status output (t_{FO}) can be adjusted by the capacitance of the capacitor between CFO and COM terminal. The fault status output pulse width is 2.4ms when the capacitor capacitance is 22nF. CFO is given by CFO (typ.) = t_{FO} x (9.1 x 10-6) [F].
- As shown in Fig. 3-21, diodes are connected between VCCL-VFO and VFO-COM terminals. These diodes are built-in to protect the product from input surge voltage. Do not use these diodes for voltage clamp purpose as it might damage the product.
- Fig. 3-22 shows the voltage-current characteristics of VFO terminal during fault status output. I_{FO} is the sink current of VFO terminal.

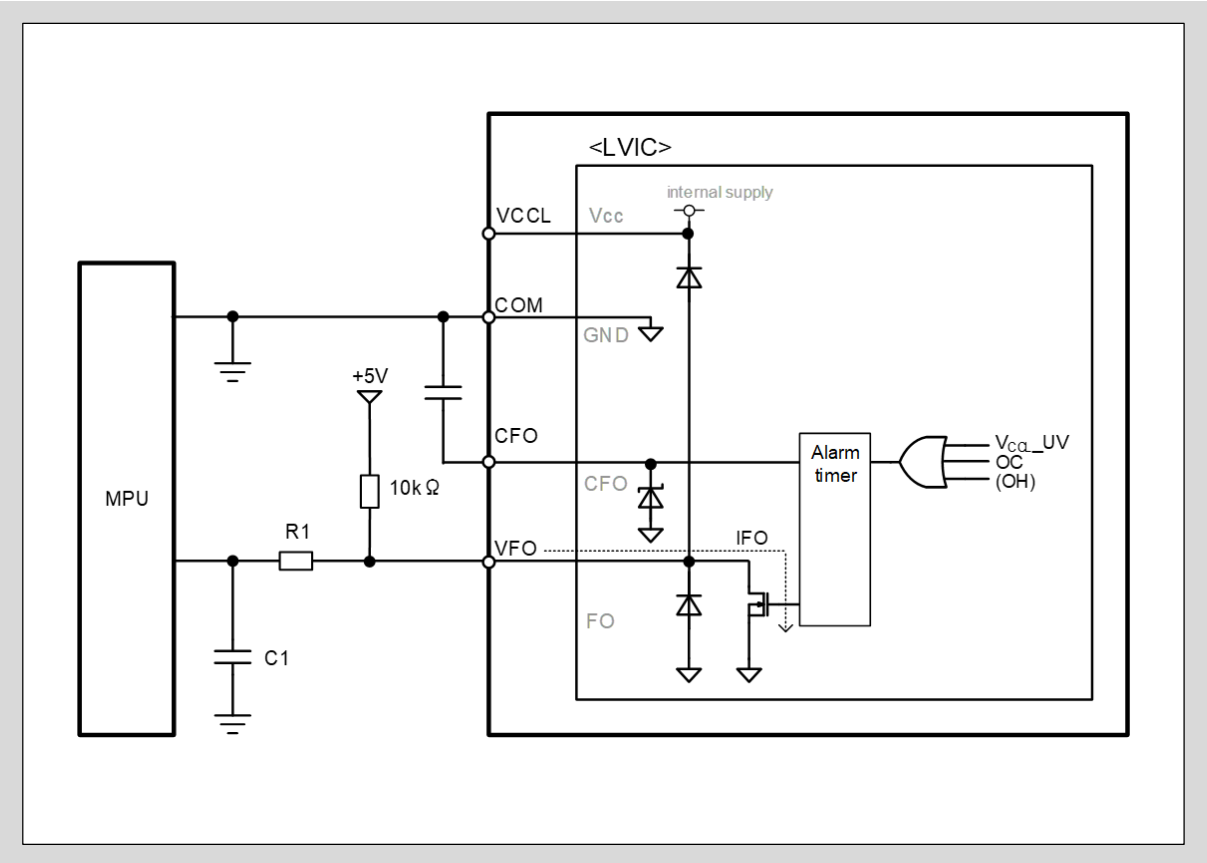


Fig. 3-21 Recommended MPU I/O interface circuit of VFO terminal

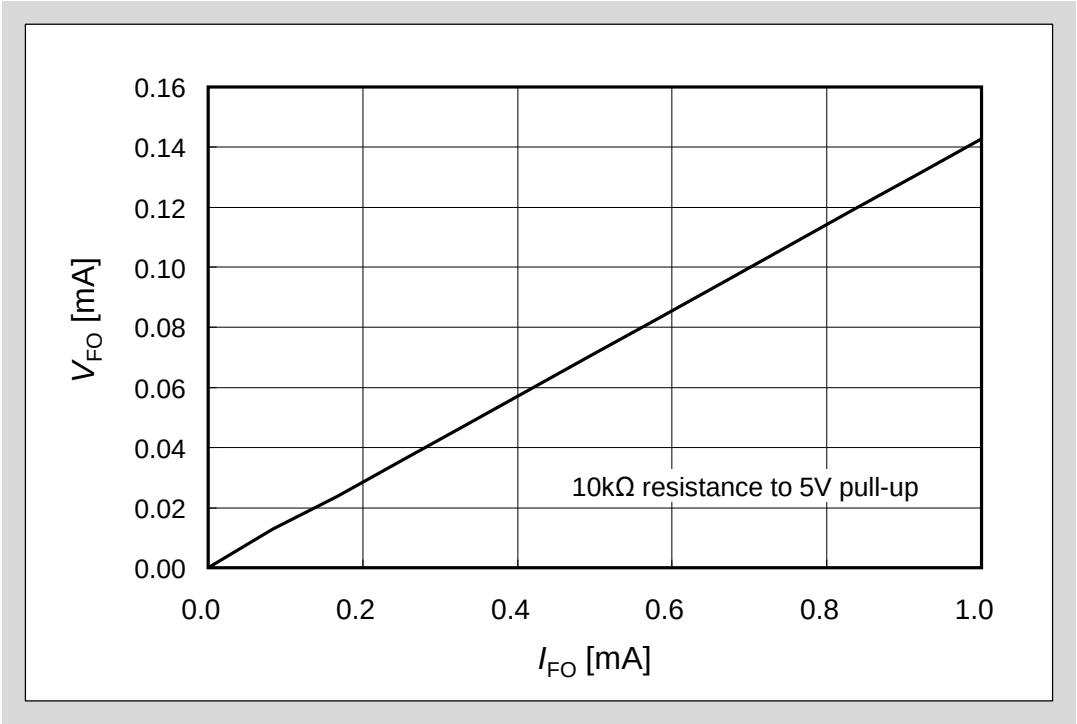


Fig. 3-22 Voltage-current characteristics of VFO terminal during fault status output

7. Temperature Output Function, TEMP

- As shown in Fig. 3-23, the temperature output terminal TEMP can be connected directly to the MPU. It is recommended to connect a bypass capacitor C_{TEMP} and an inrush current limiting resistor R_{TEMP} of 10kΩ or more between the MPU and the TEMP terminal. These signal lines should be as short as possible.
- This product has a built-in temperature sensor in LVIC that outputs analog voltage according to the LVIC virtual junction temperature. This function has no fault status output because it is not intended to protect the product. "6MBP ** XTC065-50" has built-in overheating (OH) protection. Fault status output is generated when the temperature exceeds T_{OH}.
- Since the position of the IGBT chip and the position of the temperature sensor are different, it is not possible to respond to sudden rise in T_{vj} such as during motor lock and short circuit.
- As shown in Fig. 3-23, a diode is connected between the TEMP-COM terminals. This diode is built-in to protect the product from input surge voltage. Do not use this diode for voltage clamp purpose as it might damage the product.
- Fig. 3-24 shows the LVIC virtual junction temperature versus TEMP output voltage characteristics. In the case of the MPU power supply voltage is 3.3V, connect a Zener diode to the TEMP terminal. The output voltage shows clamp characteristic at below room temperature. Connect a 5kΩ±10% pull-down resistor $R_{pulldown}$ to the TEMP terminal if linear characteristic is required.
- Fig. 3-25 shows the LVIC virtual junction temperature versus TEMP output voltage characteristics with 5kΩ pull-down resistor.
- Fig. 3-26 shows the operation sequence of the TEMP terminal during startup and shutdown of product.

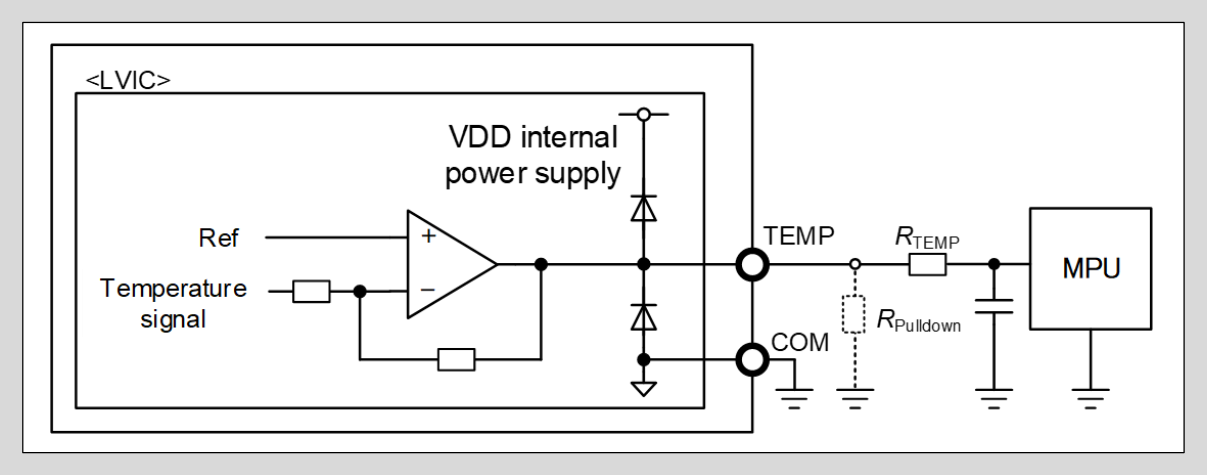


Fig. 3-23 Recommended MPU I/O interface circuit of TEMP terminal

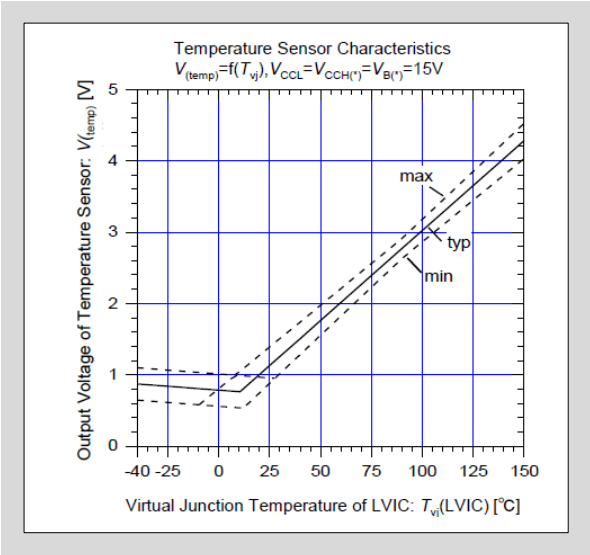


Fig. 3-24 LVIC virtual junction temperature vs. TEMP output voltage characteristic (without pull-down resistor)

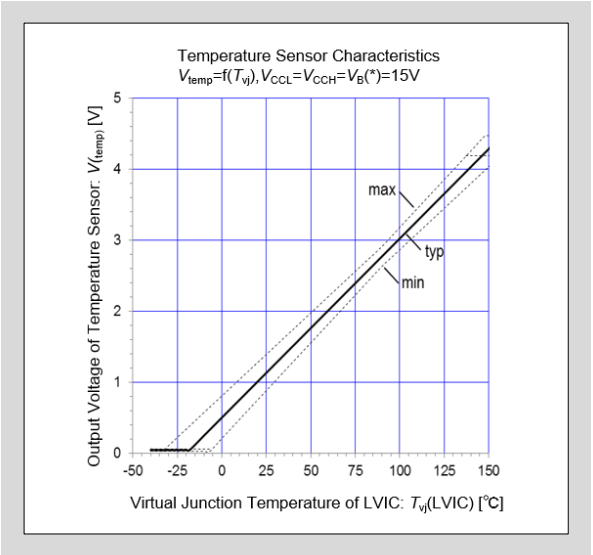


Fig. 3-25 LVIC virtual junction temperature vs. TEMP output voltage characteristic (with 5kΩ pull-down resistor)

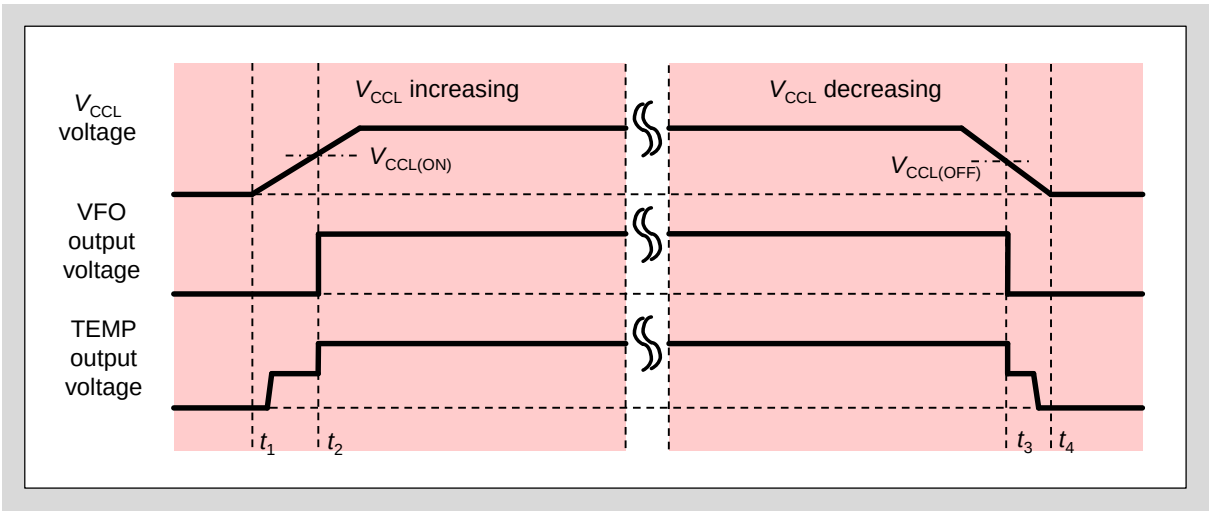


Fig. 3-26 Operation sequence of TEMP terminal during startup and shutdown

*t*1-*t*2 : TEMP output function is activated when V_{CCL} exceeds $V_{CCL(ON)}$. When V_{CCL} is lower than $V_{CCL(ON)}$, TEMP output voltage is the same as clamp voltage.

*t*2-*t*3 : TEMP output voltage rises to the voltage determined by LVIC virtual junction temperature. Under temperature condition that cause clamp operation, TEMP output voltage is the same as clamp voltage even if V_{CCL} exceeds $V_{CCL\ (ON)}$.

*t*3-*t*4 : TEMP output function is reset when V_{CCL} falls below $V_{CCL(OFF)}$. TEMP output voltage is the same as clamp voltage.

8. Overheating Protection Function

- The over heating (OH) protection functions is integrated into "6MBP**XTC065-50".
- The OH function monitors the LVIC junction temperature. Since the position of the IGBT chip and the position of the temperature sensor are different, it is not possible to respond to sudden rise in T_{vj} such as during motor lock and short circuit.
- The T_{OH} sensor position is shown in Fig.2-3.
- As shown in Fig.3-27, the product shuts down all low side IGBTs when the LVIC temperature exceeds T_{OH}. The fault status is reset when the LVIC temperature drops below $T_{OH} - T_{OH(hys)}$.

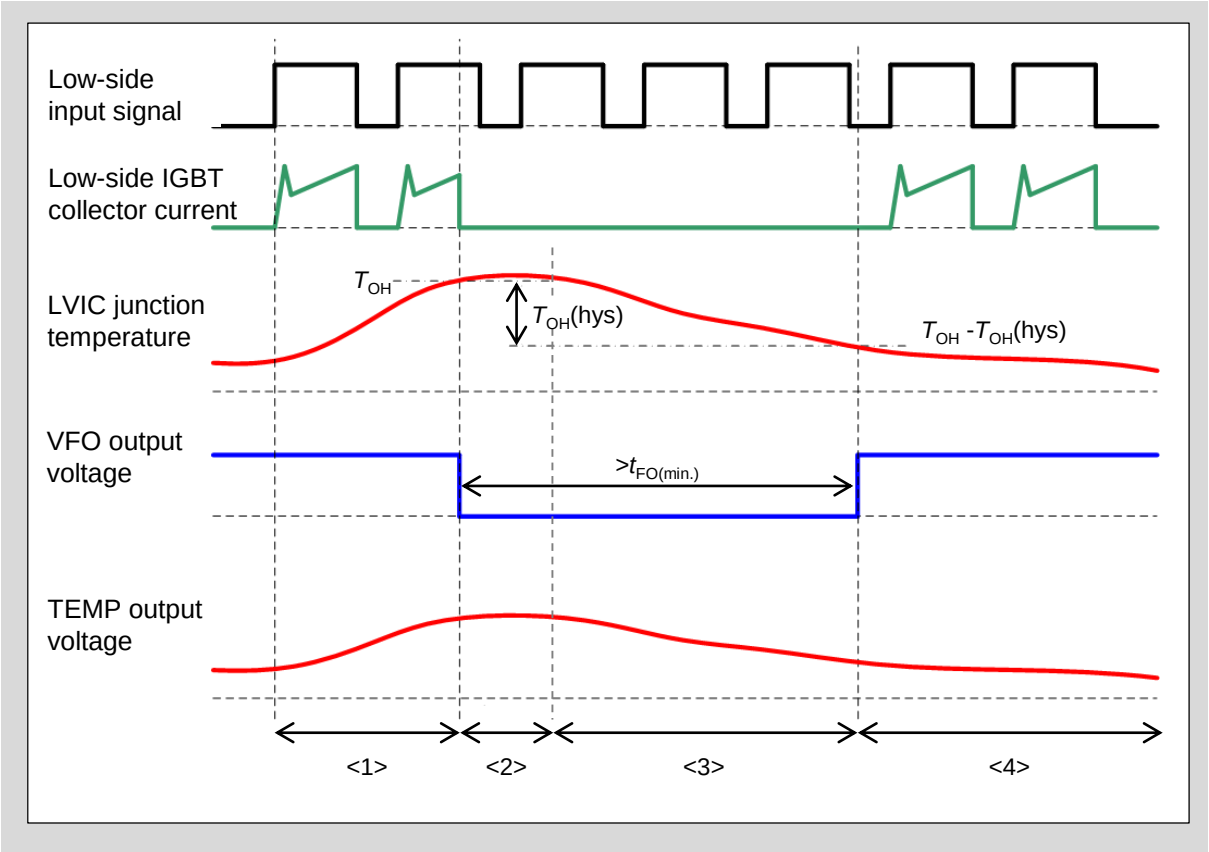


Fig. 3-27 OH protection operation sequence

<1> : When LVIC virtual junction temperature is below T_{OH}, all low-side IGBTs operate normally.

<2> : While LVIC virtual junction temperature is above T_{OH}, all low-side IGBTs are turned off and fault output voltage is generated.

<3> : During OH protection status, TEMP terminal continues to output voltage corresponding to LVIC virtual junction temperature.

<4> : Fault status and OH protection status are reset after LVIC virtual junction temperature falls below T_{OH}-$T_{OH(hys)}$ and t_{FO} has elapsed. The low-side IGBTs restart operation from the next input signal. $T_{OH(hys)}$ is the hysteresis temperature of overheating protection.

Chapter 4 Details of Inverter Block

This chapter describes the guidelines and precautions of circuit design for power terminals, such as how to determine the current sense resistor and external shunt resistor.

1. Connection of Bus Voltage Input Terminal and Low-side IGBTs Emitter

<Description of Power Terminals>

Table 4-1 shows the details of the power terminals

Table 4-1 Details of power terminals

Terminal Name	Description
P	Positive bus voltage input terminal. It is internally connected to the collector of the high side IGBTs. In order to suppress the surge voltage caused by the wiring or PCB pattern inductance of the bus voltage, connect a snubber capacitor close to this terminal. (Typically metal film capacitors are used)
U, V, W	Motor output terminal Inverter output terminals for connecting to motor load.
N(U), N(V), N(W)	Negative bus voltage input terminals These terminals are connected to the emitter of the low-side IGBTs of each phase. When using the external shunt resistor method to monitor the current of each phase, connect a shunt resistor between these terminals and power GND.
VSC	Low-side sense current detection terminal. This terminal is connected to the sense terminal of the low-side IGBTs. This terminal detects the sense current shunted from the main current. Connect a sense resistor between VSC terminal and control GND for short-circuit protection.

<Recommended wiring for shunt resistor and snubber capacitor>

- External shunt resistors are connected to detect overcurrent (OC) condition and phase current.
- Long wiring patterns between the shunt resistor and the product will cause excessive surge voltage that might damage the internal control IC and current detection components. To reduce the pattern inductance, the wiring between the shunt resistors and the product should be as short as possible.
- As shown in the Fig.4-1, snubber capacitors should be connected at the right location to suppress surge voltage effectively.
- Connecting the snubber capacitor at location "C" is recommended. If the snubber capacitor is connected at location "A" as shown in the Fig.4-1, the snubber capacitor cannot suppress the surge voltage effectively because the wiring inductance is not negligible. If the capacitor is connected at the location "B", the charging and discharging current of snubber capacitor will flow through the shunt resistor. This will impact the current detection signal and the OC protection level will be lower than the design value. Although the surge voltage suppression effect when the snubber capacitor is connected at location "B" is greater than that at location "A" or "C", location "C" is recommended considering the impact to the current detection accuracy.
- Snubber capacity of 0.1 ~ 0.22 μF is recommended.

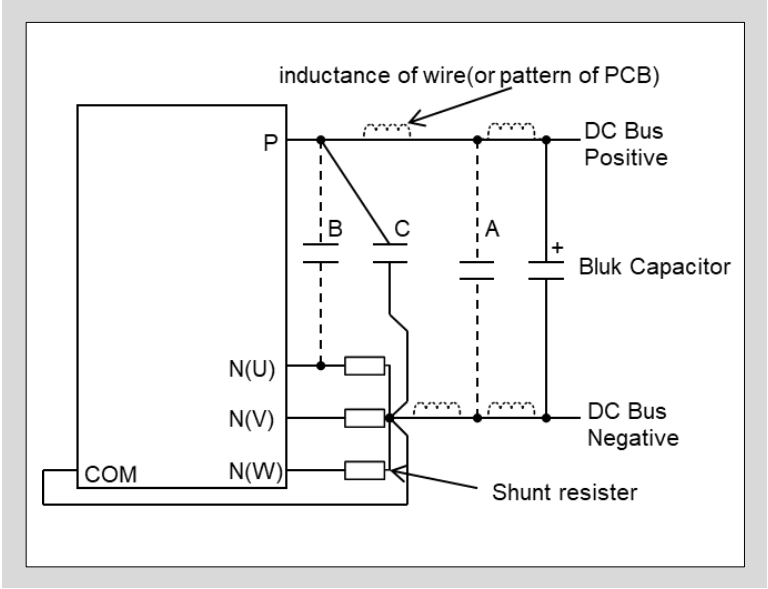
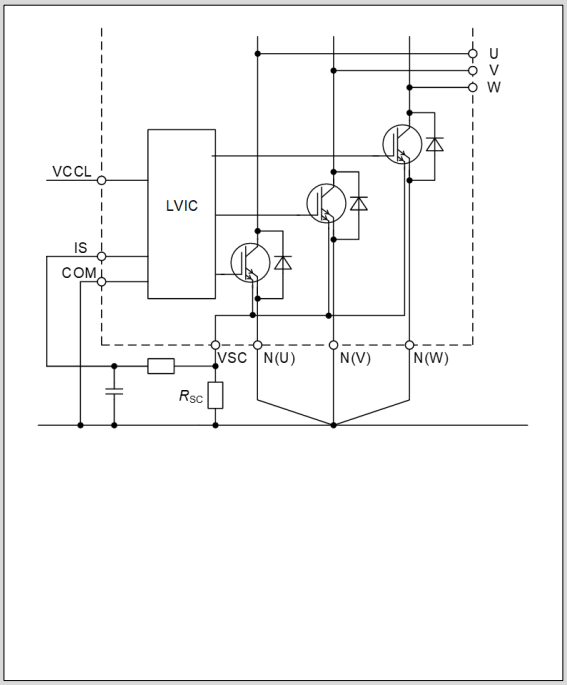


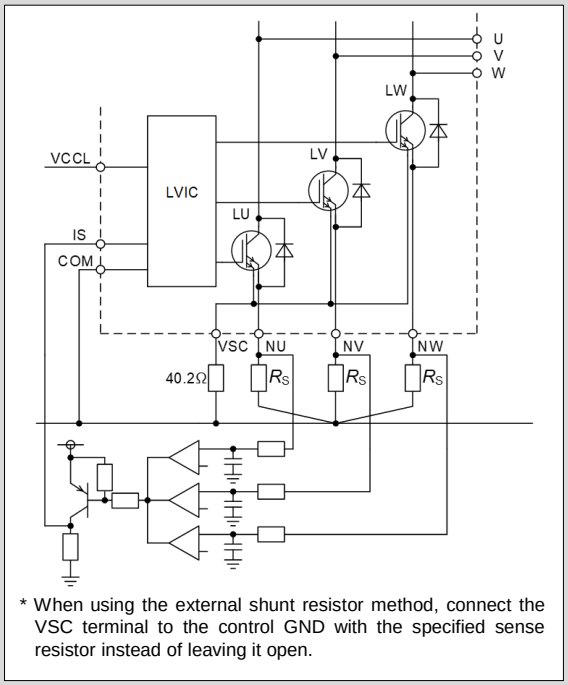
Fig. 4-1 Recommended wiring of shunt resistor and snubber capacitor

2. Short Circuit Protection

There are two methods for short circuit (SC) protection in this product. The first method is by detecting the sense current shunted from the main current flowing through the low-side IGBTs. The second method is to directly sensing the main current with external shunt resistors connected to the N(*) terminals.



Sense current method



* When using the external shunt resistor method, connect the VSC terminal to the control GND with the specified sense resistor instead of leaving it open.

External shunt resistor method

Fig. 4-2 SC detection circuits

<SC protection by sense current method>

SC protection works by feeding back the voltage generated by the sense resistor R_{sc} to the IS terminal. Table 4-2 shows the specified sense resistor value and short circuit protection current value.

Table. 4-2 SC protection current value (no external shunt resistor connected to N(*) terminals)

Type Name	Sense resistor R_{sc}	SC protection current (Min.)
6MBP50XTA065-50 6MBP50XTC065-50	40.2 Ω	85 A
6MBP75XTA065-50 6MBP75XTC065-50	23.2 Ω	127 A

- It is recommended to connect an RC filter to the input of IS terminal to prevent malfunction of the SC protection circuit caused by noise. The RC time constant is determined by the noise application time and the IGBT's short circuit capability. Time constant of 1.1μs is recommended.
- For example, to activate 6MBP50XT*065-50 SC protection, R_{sc} must be set to 40.2Ω or higher. For R_{sc}, it is recommended to use a resistor with small variation (1% or less) including temperature characteristics, low inductance, and wattage rating of 1/8W or more.

<SC protection by external shunt resistor method>

- The SC protection function by sense current method is intended for short circuit protection when an excessive short circuit current flows, such as arm short circuit or load short circuit.
- For OC protection that requires accuracy, such as demagnetization current protection of motor, external shunt resistor method is recommended.
- When external shunt resistor is connected, the current split ratio between the main and sense current varies, thus the SC protection current value by sense resistor changes too. Table 4-3 shows the minimum SC protection value with shunt resistors connected.
- If the external shunt resistance is too large, the IGBT saturation current will decrease due to the gate voltage of the low-side IGBT is lowered by the shunt resistor voltage drop. It is recommended to set the shunt resistance to 7mΩ or less for 6MBP50XT*065-50, and 4.5mΩ or less for 6MBP75XT*065-50.
- When using external shunt resistors, it is recommended to use low inductance chip resistors to reduce the surge voltage during short circuit. Do not use shunt resistors with large inductance, such as cement resistors.
- When using the external shunt resistor method, connect the VSC terminal to the control GND with the specified sense resistor instead of leaving it open.

Table 4-3 SC protection current value with shunt resistors (6MBP50XTA065-50, R_{sc}=40.2Ω)

External shunt resistance	OC protection current (Min.)
None	85 A
3 mΩ	57 A
5 mΩ	48 A

3. Setting of External Shunt Resistor for Overcurrent Protection

The following shows an example of selecting external shunt resistor for OC, SC protection, in which OC, SC detection is performed using only external shunt resistor instead of the current sensing method. When using the external shunt resistor method, connect the VSC terminal to the control GND with the specified sense resistor instead of leaving it open.

<Selecting shunt resistor>

The shunt resistance value is calculated by the following equation:

$$R_{Sh} = \frac{V_{IS(ref)}}{I_{OC}} \qquad (4.1)$$

- where $V_{IS(ref)}$ is the OC protection voltage level, and I_{OC} is the OC protection current level.
- $V_{IS(ref)}$ is 0.455V(min.), 0.48V(typ.), and 0.505V(max.).
- R_{sh} is the resistance of shunt resistor. The maximum OC detection level should be set lower than the repetitive peak collector current specified in the specification sheet of the product considering the variations in shunt resistance.
- For example, if the OC detection level is set to 100A, the recommended shunt resistance value can be calculated as:

$$R_{Sh(min)} = \frac{V_{IS(ref)(max)}}{I_{OC}} = \frac{0.505}{100} = 5.05[m\Omega] \qquad (4.2)$$

- where $R_{sh(min)}$ is the minimum shunt resistance.
- Based on the above expressions, the minimum shunt resistance is calculated. It is necessary to select a shunt resistance according to the required OC protection level in practical application.

<Setting the delay time of OC protection>

- An external RC filter is required to prevent malfunction of the OC protection circuit caused by noise. The RC time constant is determined by the noise application time and the IGBT's short circuit capability. Time constant of 1.1μs is recommended.
- When the voltage across the shunt resistor exceeds the OC level, the filter delay time $t_{(delay)}$, which is the time for the IS terminal input voltage to rises to the OC level, is determined by the time constant of the RC filter and is expressed by the following equation.

$$t_{(delay)} = -\tau \cdot \ln\left(1 - \frac{V_{IS(ref)(\max)}}{R_{Sh} \cdot I_P}\right) \qquad (4.3)$$

- where $\boldsymbol{t}$ is the RC time constant, and I_P is the peak current flowing through the shunt resistor.
- In addition, there is a shutdown propagation delay of OC ($t_{d(IS)}$), thus the total time t_{total} from OC detection until the shutdown of IGBT is given by the following equation.

$$t_{total} = t_{delay} + t_{d(IS)} \qquad (4.4)$$

- The short circuit capability of the IGBT must be considered for the total delay time. Please confirm the appropriate delay time in actual equipment.

Chapter 5 Recommended Wiring and Layout

This chapter describes the recommended wiring and layout. Please refer to the following application circuit examples for tips and precautions when designing PCB.

1. Examples of Application Circuit

Fig. 5-1, Fig. 5-2, and Fig. 5-3 show examples of application circuits using three types of current detection methods. The notes are common for all circuits.

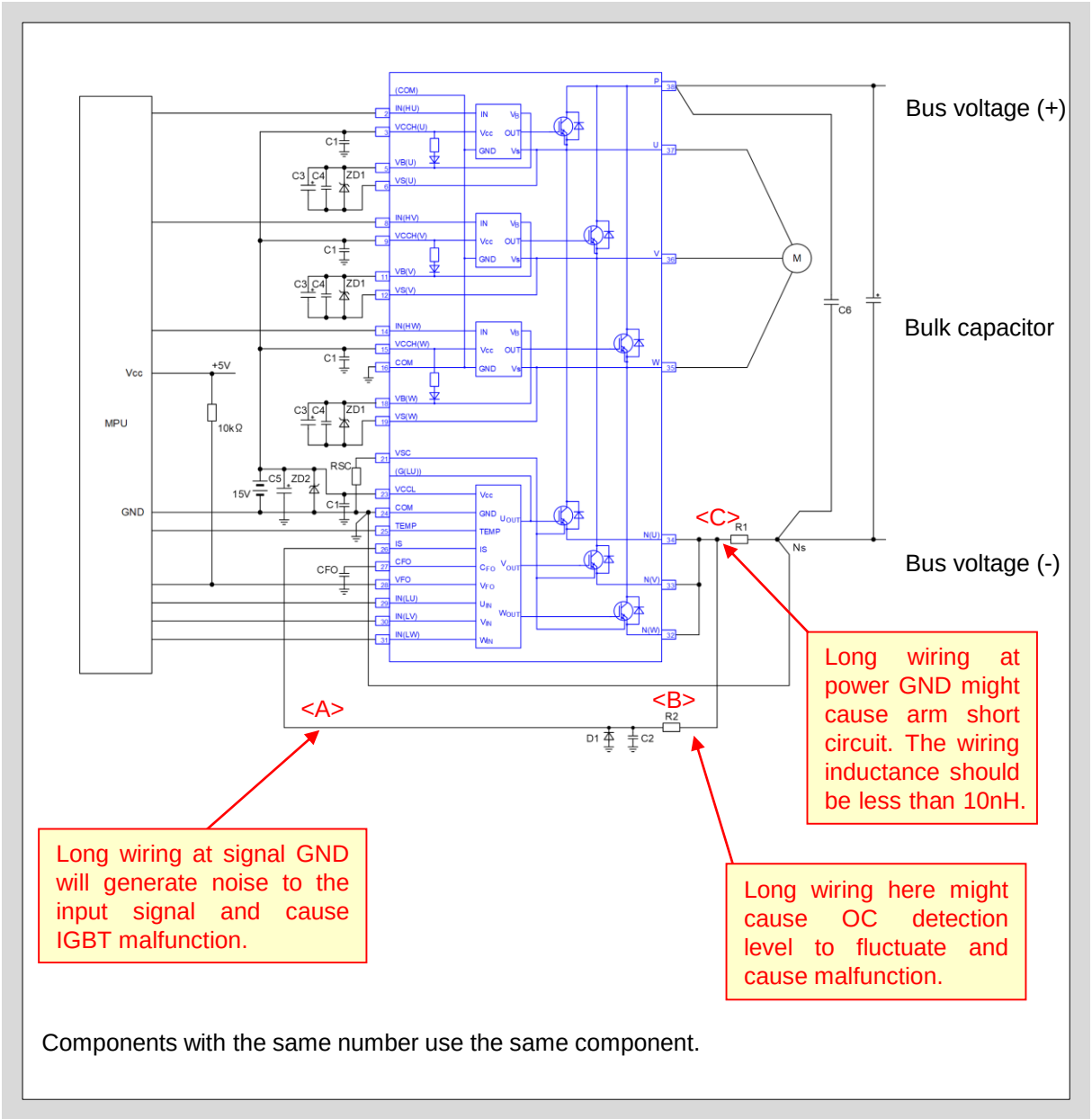


Fig. 5-1 Example of application circuit 1
(In the case of detecting all 3 phase current at once with a single shunt resistor)

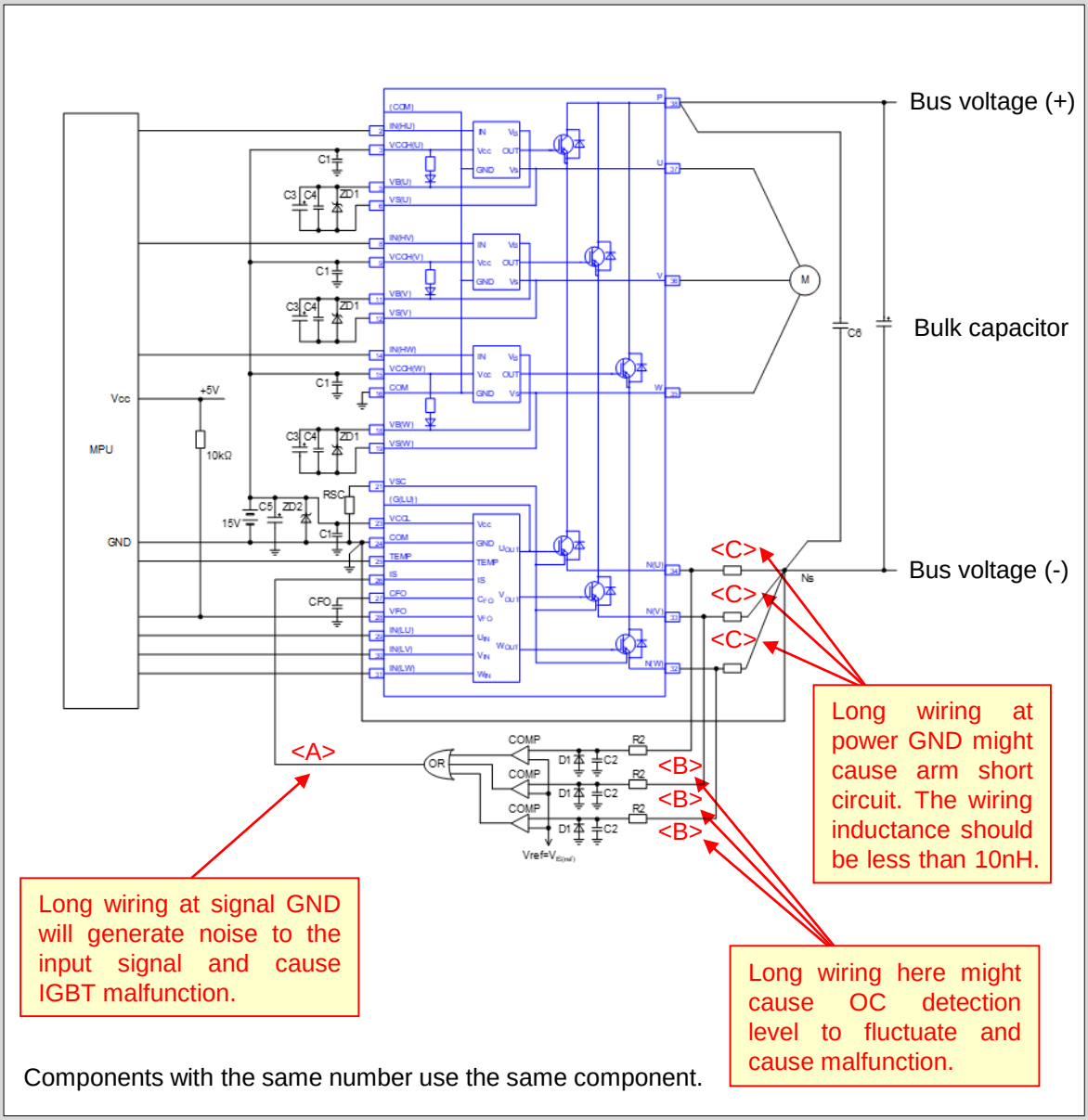


Fig. 5-2 Example of application circuit 2
(In the case of detecting each phase current with individual shunt resistor)

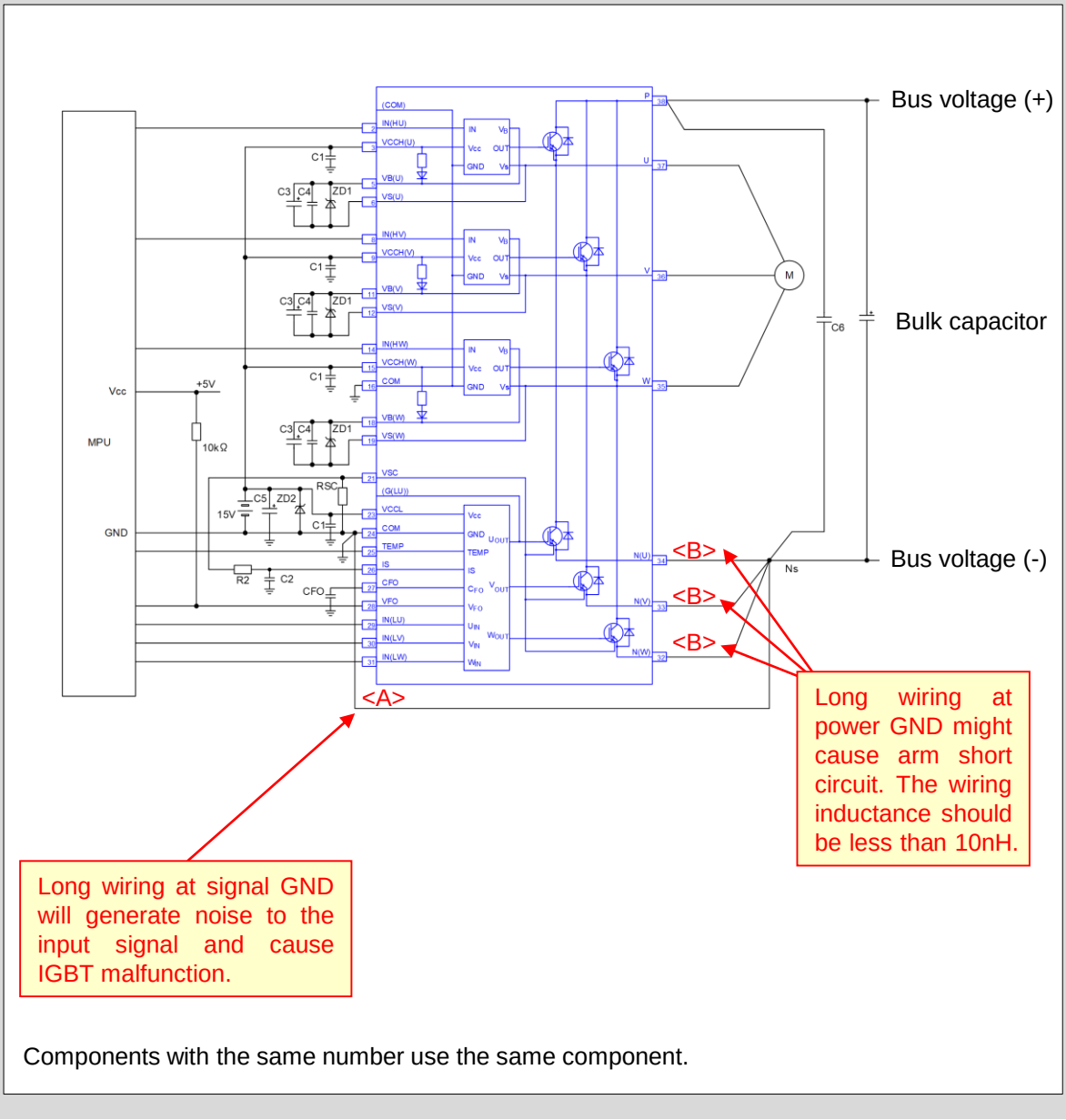


Fig. 5-3 Example of application circuit 3
(In the case of detecting sense current with sense resistor)

<Note>

1. The input signal of this product is high active. The input circuit of the control IC has built-in pull-down resistors. To prevent malfunction, the wiring of each input should be as short as possible. When using RC filter, set the input signal level to meet the turn-on and turn-off threshold voltages.
2. The built-in HVICs allow this product to be connected to MPU directly without any photocoupler or pulse transformer.
3. VFO output is open drain type. It should be pulled up to 5V power supply with a 10kΩ resistor.
4. To prevent malfunction, the wiring of <A>, <B> and <C> should be as short as possible.
5. Set the time constant of R2-C2 of the OC protection circuit to about 1.1μs. The OC shutdown time might vary depending on the wiring pattern. For R2 and C2, tight tolerance type is recommended.
6. It is recommended to set the OC protection circuit comparator reference voltage to the same level as the IPM OC protection threshold voltage $V_{IS(ref)}$.
7. Use high speed comparator and logic IC to detect OC condition quickly.
8. It is recommended to connect a Schottky barrier diode D1 if negative voltage is generated at R1 during switching operation.
9. All capacitors should be connected as close as possible to the terminals. Ceramic capacitors with excellent temperature, frequency and DC bias characteristics for C1 and C4, and electrolytic capacitors with excellent temperature and frequency characteristics for C3 and C5 are recommended.
10. To prevent destruction caused by surge voltage, the wiring between snubber capacitor C6, P terminal and Ns node should be as short as possible. Generally, the recommended snubber capacitance is 0.1uF to 0.22uF.
11. The two COM terminals (terminal no.16 & 24) are not connected internally. Connect both terminals to the signal GND at single point.
12. To prevent the destruction caused by surge voltage, it is recommended to connect a 22V Zener diode to each control power supply and high-side bias voltage terminal.
13. It is recommended that the signal GND and the power GND be wired separately, and to connect the snubber capacitor GND : Ns at a single point to avoid the effect of voltage fluctuation due to current flowing in the power line.
14. For R_{sc}, it is recommended to use a resistor with small variation (1% or less) including temperature characteristics, low inductance, and wattage rating of 1/8W or more. Please evaluate it sufficiently in actual system.
15. When using external shunt resistors, it is recommended to use low inductance chip resistors. Do not use shunt resistors with large inductance, such as cement resistors.

2. Recommendations and Precautions in PCB Design

In this section, the recommended pattern layout and precautions in PCB design are described.
Fig. 5-4 to Fig. 5-8 show the images of recommended PCB layout in examples of application circuit (Fig. 5-1, Fig. 5-2, Fig. 5-3). In these figures, the input signal from the system is represented by "IN(HU)". Recommended layouts and precautions are as follows.

<Overall design around the IPM>

- At boundary where the potential difference is high, secure an appropriate creepage distance. (Make a slit between there if necessary)
- Separate the pattern of power input (DC bus voltage) part and the high-side bias voltage part to prevent the increase of conduction noise. In the case of using a multilayer PCB and crossing these wirings on pattern, please take note of the stray capacitance between the wirings and the insulation performance of the PCB.
- Separate the high-side bias voltage and the input circuit pattern for each phase to prevent system malfunction. In the case of using a multilayer PCB, it is strongly recommended not to cross these wirings.

Details of each part are described in next page.

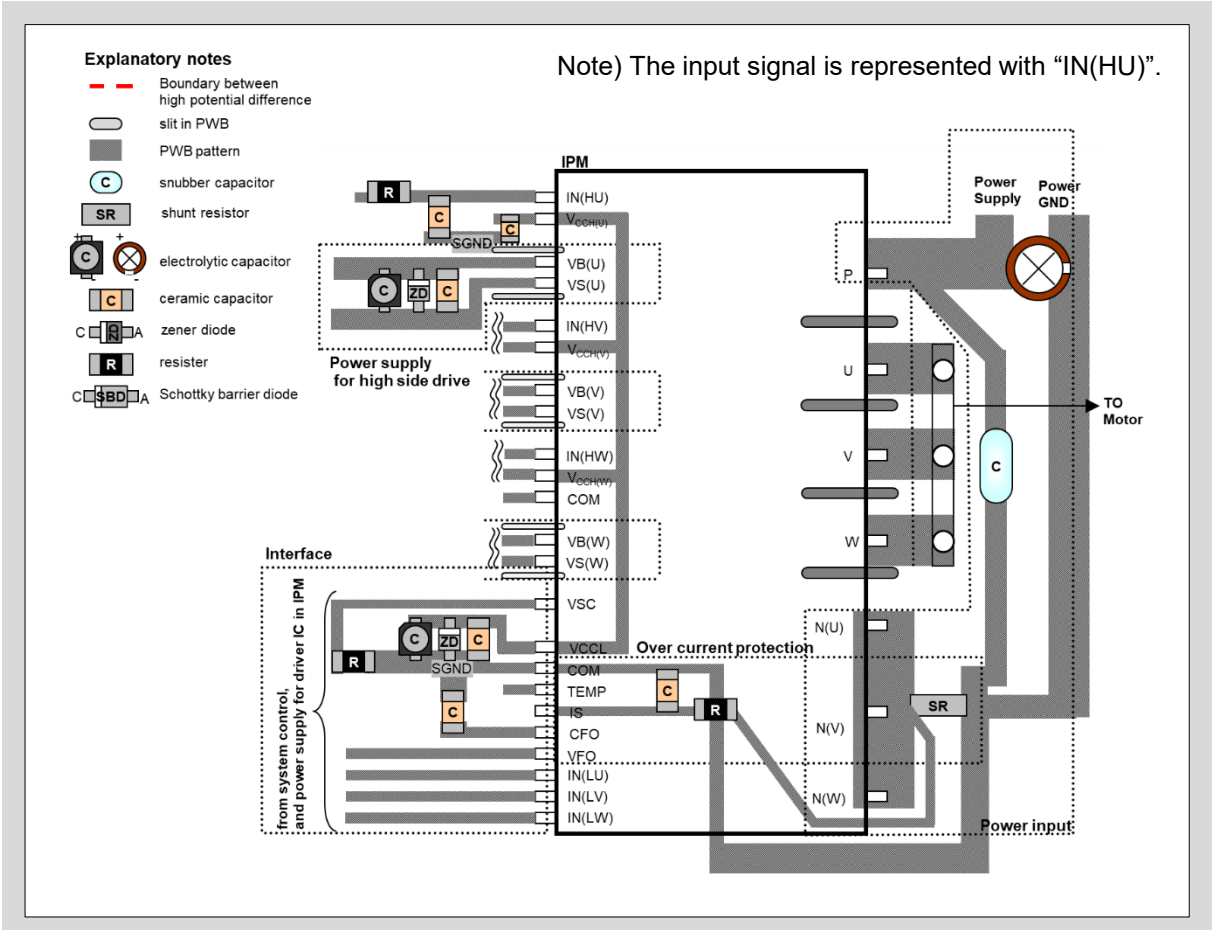


Fig. 5-4 Image of recommended PCB layout (Overall design around the Small IPM)

<Power input part>

(A) Connect the snubber capacitor between the P terminal and the GND of the shunt resistor as close as possible. To avoid the influence of pattern inductance, the pattern between snubber capacitor, P terminal and shunt resistor should be as short as possible.

(B) Separate the pattern of the bulk capacitor and the pattern of the snubber capacitor near to the P terminal and shunt resistor.

(C) The pattern from the power GND and COM terminal should be connected as close as possible to the shunt resistor at a single point ground.

(D) Please use low inductance type for shunt resistor.

(E) The pattern between the N(U), N(V), N(W) terminals and the shunt resistor should be as short as possible.

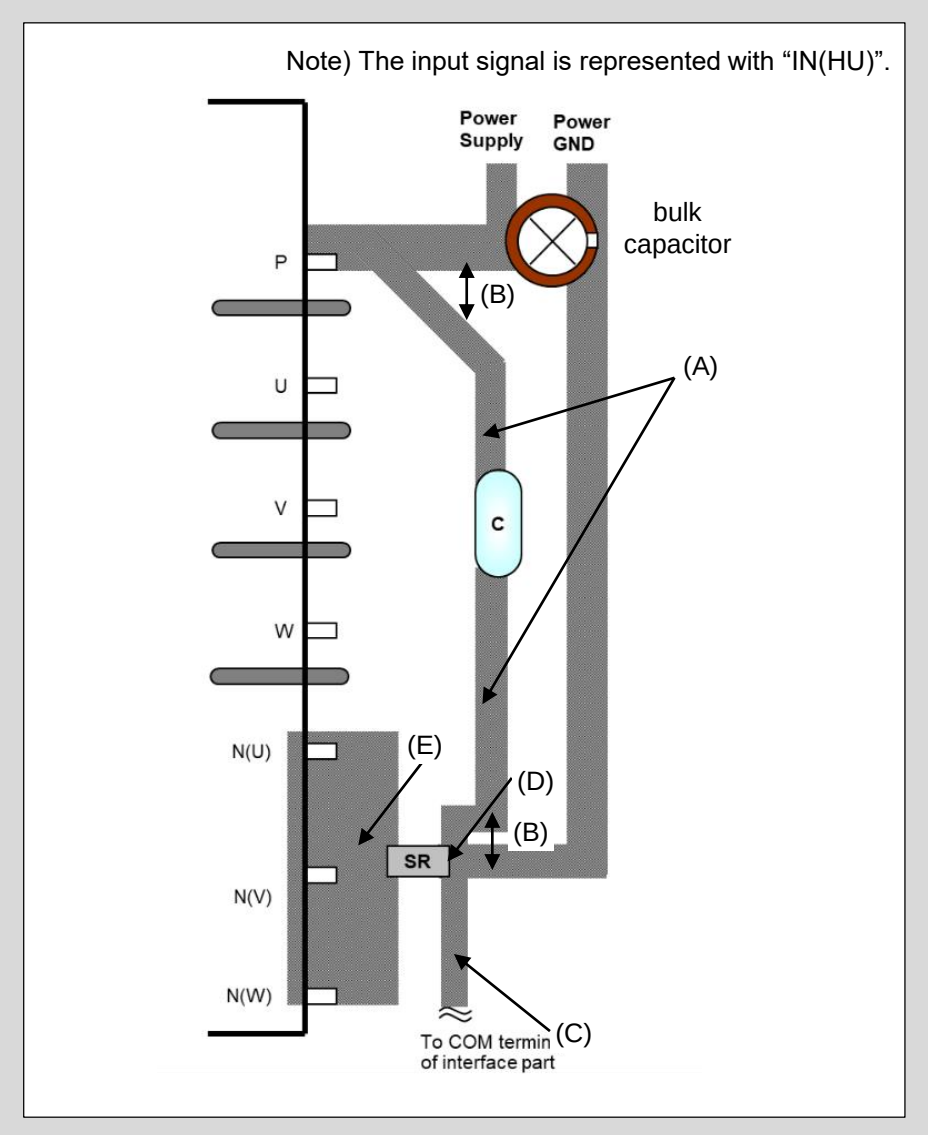


Fig. 5-5 Image of recommended PCB layout (Power input part)

<High-side bias voltage part>

(A) The pattern between VB(U,V,W) terminal and the electronic components (ceramic capacitor, electrolytic capacitor, Zener diode) should be as short as possible.

(B) Use an appropriate capacitor according to the application. In particular, use a ceramic capacitor or a low ESR capacitor close to the VB(U,V,W) terminals.

(C) If the stray capacitance between VB(U) and the power GND (or equal potential) terminal is large, the voltage between VB(U) and VS(U) terminals might become overvoltage or negative voltage due to the high dV/dt during IGBT turn-on and turn-off. Therefore, it is recommended to connect a Zener diode between VB(U) and VS(U) terminals. It should be connected as close as possible to VB (U) terminal. (The same applies to VB(V) and VB(W).)

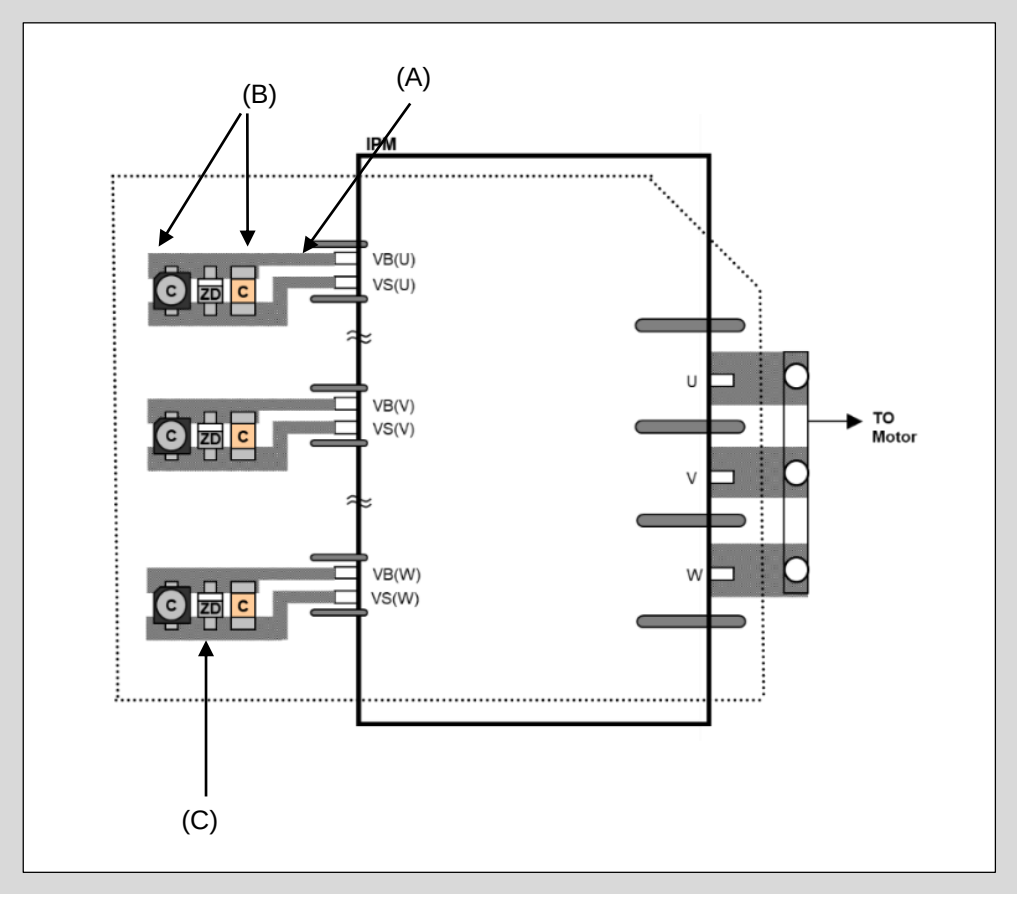


Fig. 5-6 Image of recommended PCB layout (High-side bias voltage part)

<Interface part>

(A) If the influence of noise from the high-side bias voltage is not negligible, connect a capacitor between the input signal and the COM terminal. The negative pole of the capacitor should be connected to the signal GND as close as possible to the COM terminal. In the case of connecting a filter resistor or capacitor, please take into account of the built-in pull-down resistor and confirm the input signal level in the actual system.

(B) The two COM terminals (terminal no.16 & 24) are not connected internally. Connect both terminals to the signal GND at single point.

(C) Connect an electrolytic capacitor and a ceramic capacitor between VCCL and COM, and between VCCH(U,V,W) and COM. Connect these capacitors as close as possible to each terminal.

(D) The output signal from the TEMP terminal should be in parallel with the signal GND in order to minimize the effect of noise.

(E) The pattern of signal GND from the system and the pattern from the COM terminal should be connected at a single point ground. The single point ground should be as close as possible to the COM terminal.

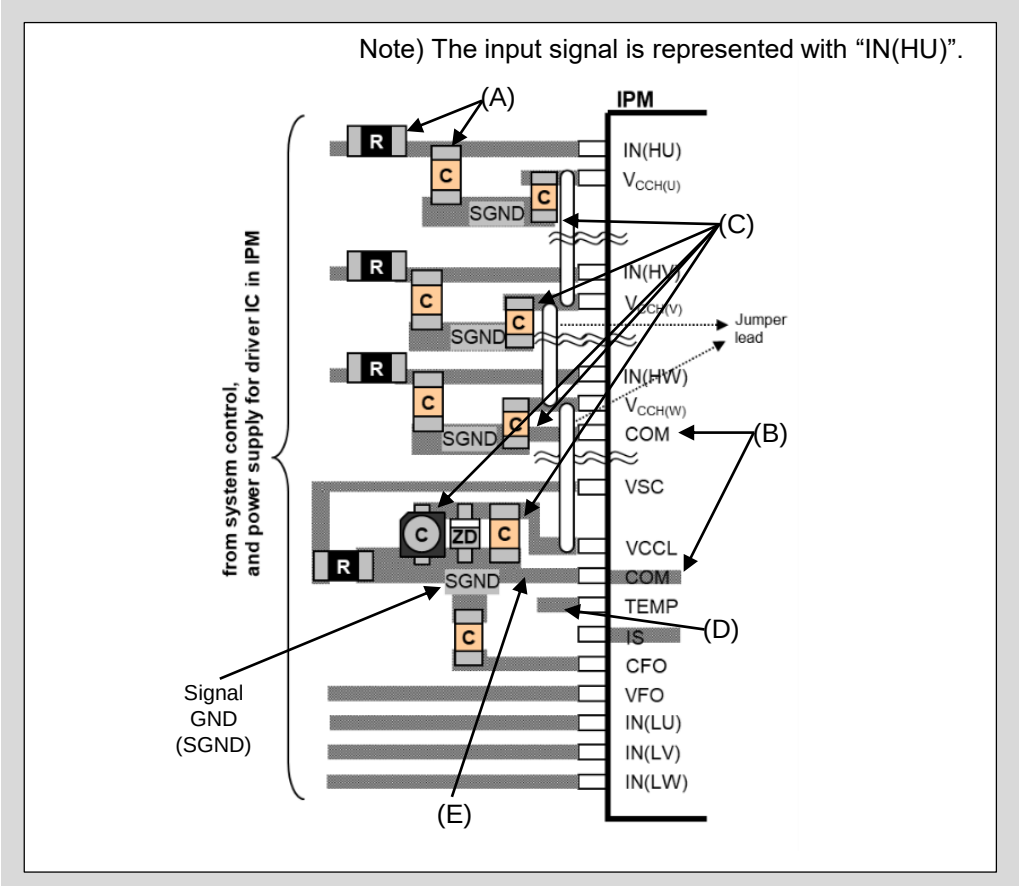


Fig. 5-7 Image of recommended PCB layout (Interface part)

<Overcurrent protection part>

As shown in Fig. 5-1, Fig. 5-2 and Fig. 5-3, there are three methods for OC detection and protection. They are “Detecting all 3 phase current at once with a single shunt resistor method” (Fig. 5-8), “Detecting each phase current with individual shunt resistor method” (Fig. 5-9), and “Detecting sense current with sense resistor method” (Fig. 5-10).

In Fig. 5-8

(A) The pattern between the negative pole of the shunt resistor and the COM terminal is very important. It is the reference potential for the control IC, and also the path for the high-side bootstrap capacitor charging current and the low-side IGBT gate drive current. Therefore, to minimize the effect of common impedance, this pattern should be as short as possible.

(B) The pattern of IS signal should be as short as possible to avoid OC level fluctuation.

(C) To prevent erroneous detection during switching operation, connect a RC filter to the IS terminal. The negative pole of the RC filter capacitor should be connected to the signal GND near the COM terminal.

(D) If negative voltage is applied to the IS terminal during switching operation, connect a Schottky barrier diode between the IS terminal and the COM terminal or in parallel with the shunt resistor.

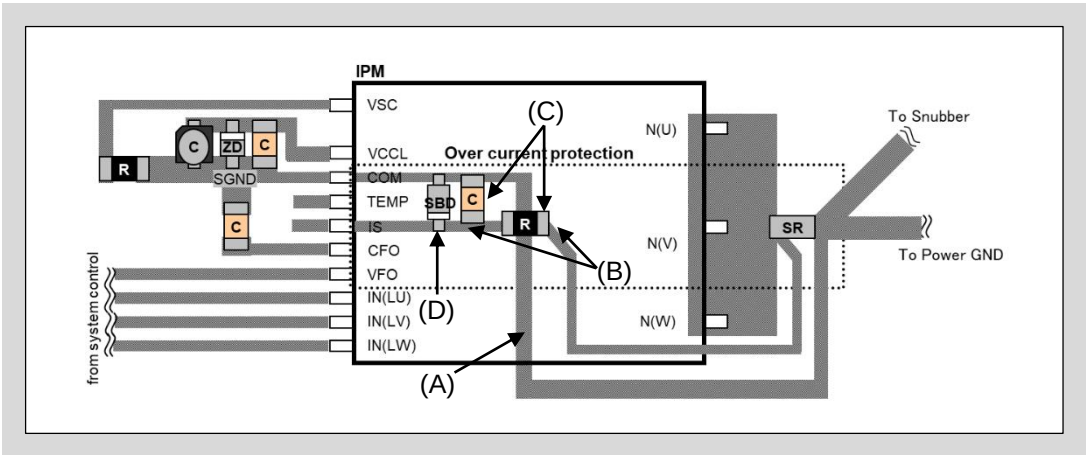


Fig. 5-8 Detecting all 3 phase current at once with a single shunt resistor method

In Fig. 5-9

(A) Use high speed comparator and logic IC to detect OC condition quickly

(B) The reference voltage of OC which is input to the comparator should be coupled by a capacitor to signal GND. The capacitor should be connected as close as possible to the comparator.

(C) Separate the signal GND pattern of COM terminal and the signal GND pattern of comparator.

(D) The signal GND pattern of COM terminal and the signal GND pattern of comparator should be connected at a single point ground. The single point ground should be as close as possible to the shunt resistor.

(E) Other precautions and recommended patterns are same as Fig. 5-7(a). Refer to Chapter 4, Section 2 for details on circuit constant determination.

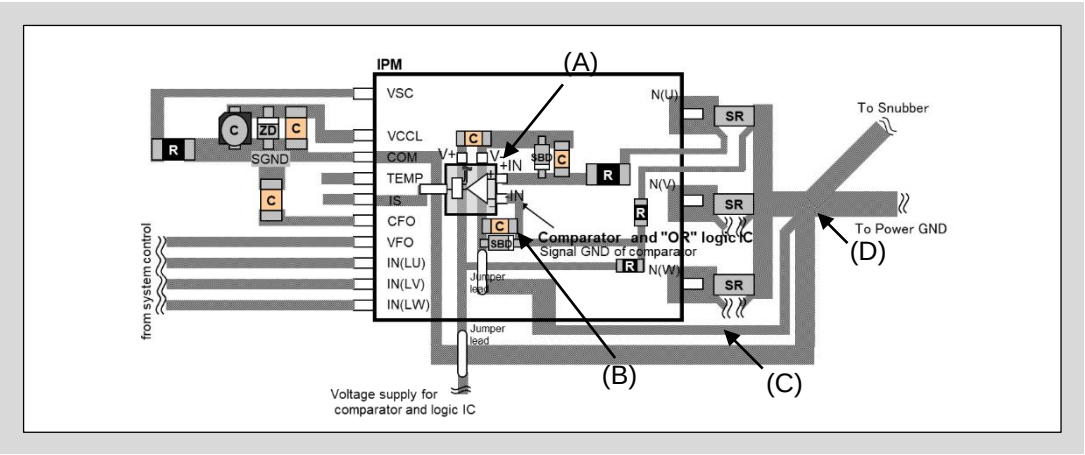


Fig. 5-9 Detecting each phase current with individual shunt resistor method

In Fig. 5-10

(A) To avoid voltage flucatuations caused by the current flowing in the power line, separate the control GND and power GND, and connect them at one point to the snubber capacitor GND.

(B) To prevent fluctuations of the OC protection level and malfunction, the IS signal pattern should be as short as possible.

(C) To prevent erroneous detection during switching operation, connect a RC filter to the IS terminal. The negative pole of the RC filter capacitor should be connected to the signal GND near the COM terminal.

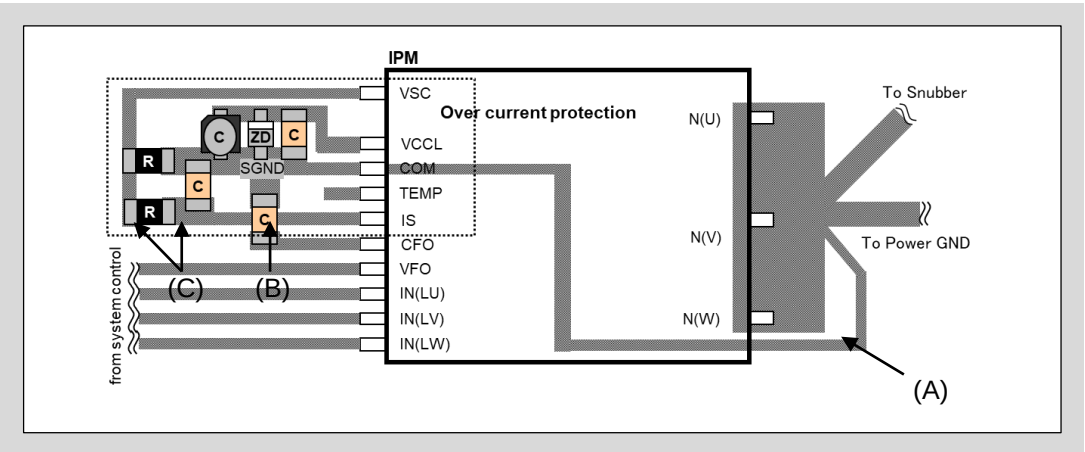


Fig. 5-10 Detecting sense current with sense resistor method

Chapter 6 Mounting Guidelines and Thermal Design

1. Soldering to PCB

- The product temperature during soldering might exceed the absolute maximum rating of the product. To prevent damage to the product and to ensure reliability, please do not use exceed the following soldering temperature.

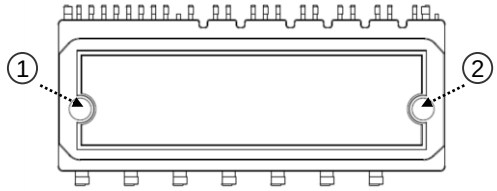
Table 6-1 Soldering temperature and immersion time

Method	Soldering temperature and time
Dip soldering	260±5°C, 10±1sec

- A stopper is provided on the terminal to prevent the immersion depth of the terminal from coming too close to the product body. Use this stopper to secure the required distance from the printed circuit board and prevent the product body from being immersed in the solder bath during flow soldering.
- It is not recommended to reuse the product after it is removed from the printed circuit board because there is a possibility that the removed product was subjected to thermal or mechanical damage during the removal process.

2. Mounting to Heat Sink

When mounting the product to a heat sink, please refer to the following recommended tightening sequence. Uneven tightening due to excessive torque might lead to destruction or degradation of the chip.



Recommended:
Pre-screwing: 1 → 2
Final screwing: 2 → 1

Note: The pre-screwing torque is set to 30% of the final screwing torque rating(0.59～0.98N·m)

Fig. 6-1 Recommended screw tightening sequence

- Fig. 6-2 shows the measurement position of the heat sink flatness.
- The flatness of the heat sink should be 0μm/100mm to +100μm/100mm, and the surface roughness (Rz) should be less than 10μm.
- If the heat sink has a concave surface, a gap occurs between the heat sink and the product, leading to reduced cooling efficiency.
- If the flatness is +100μm or more, the aluminum base of the product may be deformed and cracks could occur in the internal insulating substrate.

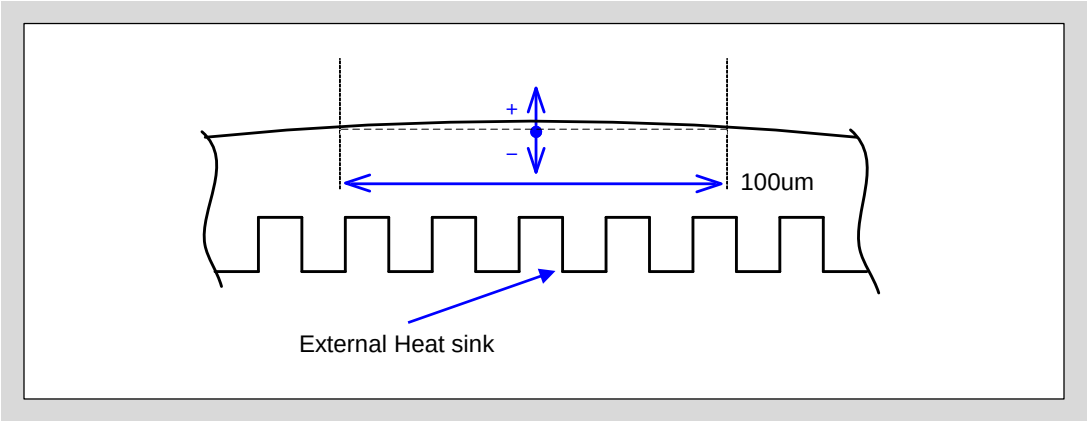


Fig. 6-2 The measurement position of heat sink flatness

It is recommended to apply thermal grease using a stencil mask to obtain the heat dissipation effect. The stencil mask is described in the mounting instructions (MT6M16534).

3. Heat Sink Selection

- Please design the cooling body (heat sink) so that the IGBT virtual junction temperature does not exceed the maximum virtual junction temperature T_{vj} for safe operation even during abnormal conditions such as overload.
- Operation of the IGBT at a temperature higher than the T_{vj} might cause damage to the chip. In 6MBP**XTC065-50 products, all low side IGBTs will shutdown when the LVIC temperature exceeds T_{OH}. However if the temperature rises rapidly, the IGBTs might not be protected.
- Similarly, please make sure that the FWD chip temperature does not exceed the T_{vj} too.
- When selecting a cooling body (heat sink), please verify the chip temperature by measuring at the position shown in Figure 2-3.

Please refer to Chapter 6, Section 2 and the following document for more details about thermal design:
“FUJI IGBT MODULES APPLICATION MANUAL (REH984)”

- Power dissipation loss calculation
- Selecting heat sinks
- Heat sink mounting precautions
- Troubleshooting

Chapter 7 Notes

1. Precautions for Use

- This product shall be used within its maximum rating (voltage, current, temperature, and so on) described in this specification. This product may be broken in case of using beyond the maximum ratings. The specified value in the absolute maximum ratings are guaranteed value for the rating, not for any combination of ratings or characteristics. Even if this product is used within absolute maximum ratings, expected product lifetime may not be obtained depending on the temperature or usage environment. Please refer to the absolute maximum rating of this product, and judge the suitability of this product for your system / equipment after evaluation and verification by yourself.
- It shall be confirmed that IGBT's operating locus of the turn-off voltage and current are within the RBSOA specification. If the IGBT is used beyond the range of RBSOA, this product may be destroyed.
- If a voltage exceeding $V_{CE(chip)}$ is applied, avalanche breakdown may occur and this product may be destroyed. Use this product so that $V_{CE(chip)}$ is within the maximum rating.
- FWD of this product is not designed to be used as a diode rectifier (AC-DC conversion circuit).
- If a transient overvoltage that exceeds the voltage rating of the device in this product is propagated from the electric power supply to this product due to a lightning strike, etc., the overvoltage may destroy this product. If any transient overvoltage is expected to be applied from the electric power supply to line-line or line-ground, insert a surge absorber, etc. to suppress the voltage applied to this product in order to avoid damage.
- This product is not designed for use in parallel connection, so it cannot be used in parallel connection.
- If applied Printed Circuit Board is not suitable, the main pin terminals may have higher temperature than T_C (Case temperature). Also the main pin terminals shall be used within temperature range of Tc (Case temperature).
- This product are made of incombustible material. However, if this product fails, it may emit smoke or flame. Also, operating this product near any flammable place or material may cause this product to emit smoke or flame in case this product become even hotter during operation. Design the arrangement to prevent the spread of fire.
- Install surely a adequate fuse or breaker between the commercial power supply (three-phase line) and this product in case the system / equipment is destroyed by an accident to prevent secondary destruction such as fire, explosion, and fire spread.
- Do not directly touch the leads or package of this product while power is supplied or during operation in order to avoid electric shock and burns.
- In any environment containing corrosive gases, corrosive liquids, corrosive solids (acids, alkalis, organic substances, etc., ex: hydrogen sulfide, sulfurous acid gas, cutting fluid, cement powder etc.), this product may oxidize or corrode, resulting in poor contact, disconnection, short circuit, ground fault, etc. In such cases, avoid to use this product as it may cause malfunctions. In the unlikely event that a short circuit or ground fault occurs to this product, there is a secondary risk of smoke, fire, or explosion, etc. If this product is used under conditions containing these corrosive substances, Fuji Electric Co., Ltd. is not responsible regardless of the conditions (temperature, humidity, concentration, etc.).

- If this product is used in an environment with sudden temperature changes, it is expected that short circuits and ground faults will occur due to dew condensation. In the unlikely event that a short circuit or ground fault occurs to this product, there is a secondary risk of smoke, fire, or explosion, etc. Fuji Electric Co., Ltd. is not responsible for any use of the product in an environment where condensation may occur.
- If the product is used in a high humidity environment or after storage the equipment after assembling, operate the equipment after sufficiently releasing the moisture. If the product is operated in a moisture-absorbed state, it may cause electrical wiring defects or insulation defects inside of this product, and Fuji Electric Co., Ltd. is not responsible for the matters.
- This product is not designed for use in a dusty environment. When used in an environment where dust is generated, heat dissipation may deteriorate due to clogging of the heat sink, and short circuits or ground faults may occur due to leaks between terminals or creeping discharge. (Even if the dust is an insulating material such as fiber, it may leak due to moisture absorption.)
- In general, semiconductor devices have accidental failure modes due to high-speed particles (cosmic rays) derived from space or radiation. The failure rate in this failure mode varies depending on the installation location (latitude, longitude, altitude), installation environment, and operating conditions (voltage). In case the product is used under high altitude and/or voltage condition, please contact to Fuji Electric Co., Ltd.
- Clearance distance and creepage distance of this product are designed for adapting use environment in 2000 m sea level or below, Fuji Electric Co., Ltd. is not responsible for the use in an environment where the altitude exceeds 2000 m above sea level or in an environment where the atmospheric pressure is similarly low.
- If this product is used beyond its lifetime, this product performance and quality of the product may deteriorate before the target lifetime of the system / equipment, and in the worst case, this product may be destroyed. Use this product after fully understanding the usage environment of the system / equipment in which this product is installed and considering that this product satisfies the target lifetime.
- Consider the possible temperature rise not only for the junction and case, but also for the outer leads.
- When designing a new equipment, always refer to the latest mounting instructions.
- Make sure you follow the instructions in the application manual for a detailed usage, PCB layout and the installation, etc.
- Please connect an adequate ceramic capacitor near the VCCH(U)-COM terminal, VCCH(V)-COM terminal, VCCH(W)-COM terminal and VCCL-COM terminal in order that VCCH(U), VCCH(V), VCCH(W) and VCCL terminal might be not directly impressed high frequency noise such as switching noise.
- When the noise is input to each control terminal of this product, this product may malfunction. Please confirm that neither the instable operation nor the malfunction occurs by the noise and use this product.
- When $V_{B(U)}$, $V_{B(V)}$ and $V_{B(W)}$ are less than $V_{B(off)}$ due to noise, the corresponding upper side IGBTs may turn OFF. Please connect an adequate ceramic capacitor near the VB(U)-VS(U) terminal , VB(V)-VS(V) terminal and VB(W)-VS(W) terminal, respectively.

- The voltage of input signal must exceeds the threshold voltage.
- Use this product below the power cycle lifetime curve (Technical Document No .: MT6M14324). Power cycle withstand capability is classified to ΔTvj mode which is stated as above and ΔT_C mode. Since the ΔT_C power cycle lifetime of this product depends on the thermal stress due to the rise and fall of the case temperature (T_C), the lifetime of this product is greatly affected by the cooling design of the equipment installing this product. If the case temperature rises and falls frequently, or if the operating time at high temperature is long, use this product with paying sufficient attention to the product lifetime.
- If excessive stress (tension, pushing, bending) is applied to the main terminal and control terminal, the terminal may be deformed and the case resin may crack, causing poor contact and poor insulation. For the maximum allowable stress of the main terminal and control terminal, refer to the application manual of each package.
- If excessive static electricity is applied to the terminals, this product may be broken.
- When handling this product, be careful to avoid any breakdown due to the static electricity, take measures against static electricity.
- When handling this product, hold the case (package body) and do not touch the terminals. In case of touching the terminals of this product, discharge static electricity adhering to body or clothing by grounding through a high impedance resistor (approx. 1MΩ) before touching.
- Work on grounded conductive floor or table mat are recommended.
- When soldering, in order to protect this product from static electricity, use antistatic soldering iron or soldering bath to prevent static electricity, and solder with low impedance resistor between soldering iron and ground.
- When jointing this product terminals with solder, soldering at an excessive high temperature may cause deterioration of the package. Please be careful about the soldering process. When used in the reflow soldering process, the solder inside this product may remelt and impair its quality. In this case, Fuji Electric Co., Ltd. is not responsible for this product performance and appearance.
- Use the tightening torque of the screws that mounting the product within the specified values. If the tightening torque is excessive, insulation failure may occur due to cracking of the case, and if the torque is small, the contact thermal resistance may increase and the heat generation of the device may increase. In addition, it is expected that the screws will loosen due to vibrations in the usage environment, so select screws that are difficult to loosen, tighten with appropriate torque, and retighten to prevent loosening.
- The product mounting surface of the heat sink should have flatness of 50 μm or less per 100 mm between the screw mounting positions and surface roughness of 10 μm or less. Excessive convex warpage may cause isolation breakdown of this product, resulting in a serious accident. Excessive concave warpage or distortion may create gaps between the product and the heat sink, resulting in poor heat dissipation and thermal destruction. When mounting this product on a heat sink, use thermal grease or equivalent to ensure cooling. In order to spread the thermal grease thinly and evenly, the flatness and surface roughness of the heat sink should be within the recommended values described in this specification. Due to insufficient applied amount or improper spreading method, thermal grease may not spread sufficiently over the entire mounting surface of this product, leading to thermal destruction due to poor heat dissipation. When applying thermal grease, make sure that the thermal grease is spread over the entire surface of the product. (By removing this product after mounting, the spread of thermal grease can be confirmed.)

- If the amount of thermal grease near this product mounting hole is excessive, the thermal grease acts as a spacer, hindering the spread of the thermal grease and causing deterioration of heat dissipation. In addition, depending on the type or application method of thermal grease, deterioration or depletion of thermal grease may occur during high-temperature operation or temperature cycle, which may shorten this product lifetime. Pay close attention to the selection and application method of the thermal grease. Please refer to the mounting instructions of this product for selection and application method of the thermal grease.

2. Precautions for Handling and Storage

- This product must be stored at a normal temperature of 5 to 35ºC and relative humidity of 45 to 75%. If the storage area is very dry, a humidifier may be required. In such a case, use only deionized water or boiled water, since the chlorine in tap water may corrode the leads.
- This product should not be subjected to rapid changes in temperature to avoid condensation on the surface of this product. Therefore store this product in a place where the temperature is steady.
- This product should not be stored on top of each other, since this may cause excessive external force on the case.
- This product should be stored with the lead terminals remaining unprocessed. Rust may cause presoldered connections to fail during later processing.
- This product should be stored in antistatic containers or antistatic shipping bags.
- Under the above storage condition, use this product within one year.