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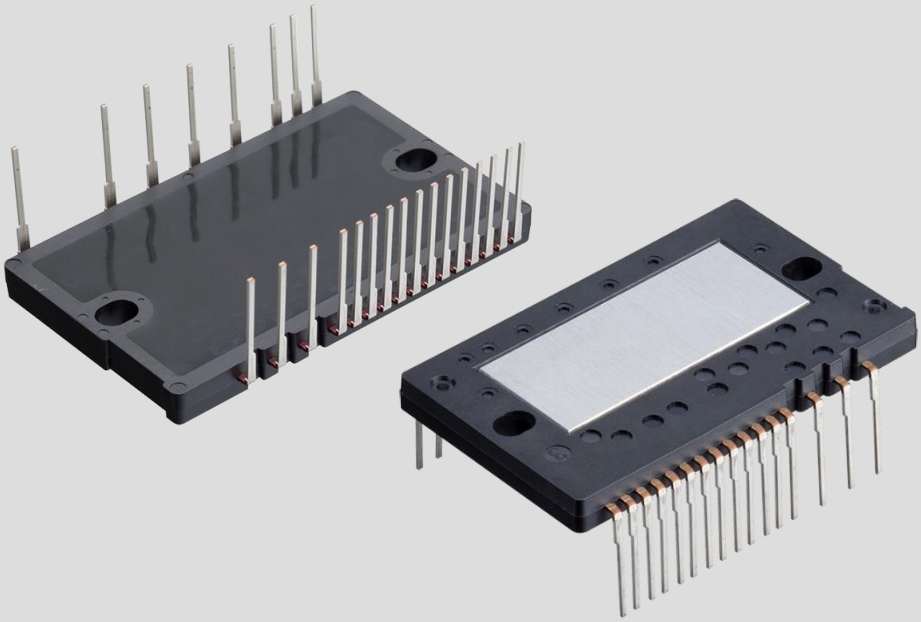

Small IPM (Intelligent Power Module)
P633A Series
6MBP**XS*060-50

Application Manual

June 2022

Fuji Electric Co., Ltd.

MT6M08855 b

Cautions

This Instruction contains the product specifications, characteristics, data, materials, and structures as of June 2022. The contents are subject to change without notice for specification changes or other reason. When using a product listed in this Instruction be sure to obtain the latest specifications.

The application examples in this note show the typical examples of using Fuji products and this note shall neither assure to enforce the industrial property including some other rights nor grant the license.

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The products described in this application manual are manufactured with the intention of being used in the following industrial electronic and electrical devices that require normal reliability.

- Compressor motor inverter
- Fan motor inverter for room air conditioner
- Compressor motor inverter for heat pump applications, etc.

If you need to use a semiconductor product in this application note for equipment requiring higher reliability than normal, such as listed below, be sure to contact Fuji Electric Co., Ltd. to obtain prior approval. When using these products, take adequate safety measures such as a backup system to prevent the equipment from malfunctioning when a Fuji Electric's product incorporated in the equipment becomes faulty.

- Transportation equipment (mounted on vehicles and ships)
- Trunk communications equipment
- Traffic-signal control equipment
- Gas leakage detectors with an auto-shutoff function
- Disaster prevention / security equipment
- Safety devices, etc.

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- Space equipment
- Airborne equipment
- Atomic control equipment
- Submarine repeater equipment
- Medical equipment

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CONTENTS

CONTENTS

Chapter 1 Product Outline

The objective of this manual is to introduce Fuji IGBT Intelligent-Power-Module “Small-IPM”.
First, the product outline of this module is described.
Next, the terminal symbols and terminology used in this manual and the specification sheet are explained. Then, the design guidelines for signal input terminals and power terminals are shown. Finally, the recommended wiring and layout, along with the mounting guidelines are given.

1. Introduction

<Product concept>

- 7th gen. IGBT technology offers high-efficiency and energy-saving operation.
- Guarantee T_{vjop}=150℃ allows expansion of output current.
- Higher accuracy of short circuit detection contribute to expansion of over load operating area.
- Compatible pin assignments, foot print size and mounting dimensions with 1st gen. Small IPM series.
- Product range: 15A – 35A / 600V.
- The total dissipation loss has been improved by improvement of the trade-off between the Collector-Emitter saturation voltage $V_{CE(sat)}$ and switching loss.

<Built-in drive circuit>

- Drives the IGBT under optimal conditions.
- The control IC of upper side arms (HVIC) have a built-in high voltage level shift circuit.
- This product can be driven directly by a microprocessor on both the upper side and lower side arms. The voltage level of input signals are 3.3V or 5V.
- Since the wiring length between the internal drive circuit and IGBT is short and the impedance of the drive circuit is low, no reverse bias DC source is required.
- Normally, IPM device requires a total of four isolated control power supplies: one for the lower sides and three for the upper sides. However, since this IPM has built-in bootstrap diodes (BSD), isolated power supplies for the upper sides are not needed.

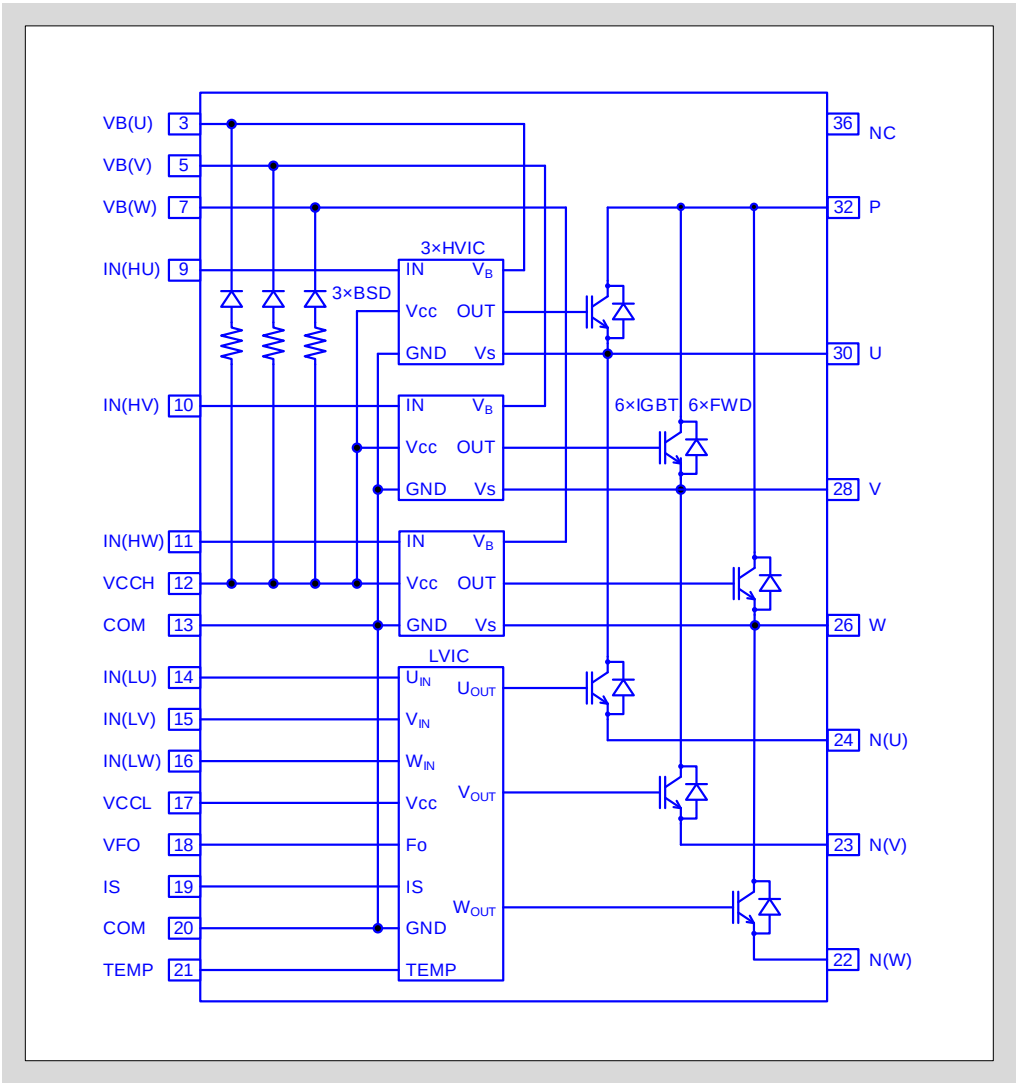


Fig.1-1 Block Diagram of Internal Circuit

<Built-in protection circuits>

- The following built-in protection circuits are incorporated in the product:
  (OC): Over current protection
  (UV): Under voltage protection for power supplies of control IC
  (LT): Temperature sensor output function
  (OH): Overheating protection (only applied to some products)
  (FO): Fault alarm signal output

- The OC protection circuits protect the IGBT against over current, load short-circuit or arm short-circuit.
- The protection circuit can monitor the emitter current using external shunt resistor in each lower side IGBT and thus it can protect the IGBT against arm short-circuit.
- The UV protection circuit operates when the control power supply voltage drops below the trip voltage level. It is built into all of the IGBT drive circuits.
- The OH protection circuit protects the product from overheating. The OH protection circuit is built into the control IC of the lower side arm (LVIC).
- The temperature sensor output function is built into the LVIC and converts the detected temperature into analog voltage output.
- The FO function outputs a fault signal when the circuit detects abnormal conditions, thus making it possible to shut down the system reliably and preventing destruction by outputting the fault signal to the microprocessor unit controlling the product.

<Compact package>

- This product uses high heat dissipation aluminum insulated metal substrate (IMS), which improves the heat radiation.
- The control input terminals have a shrink pitch of 1.778mm (70mil).
- The power terminals have a standard pitch of 2.54mm (100mil).

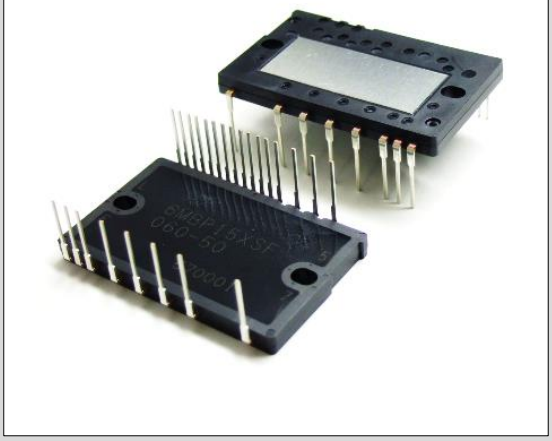


Fig.1-2 Package overview

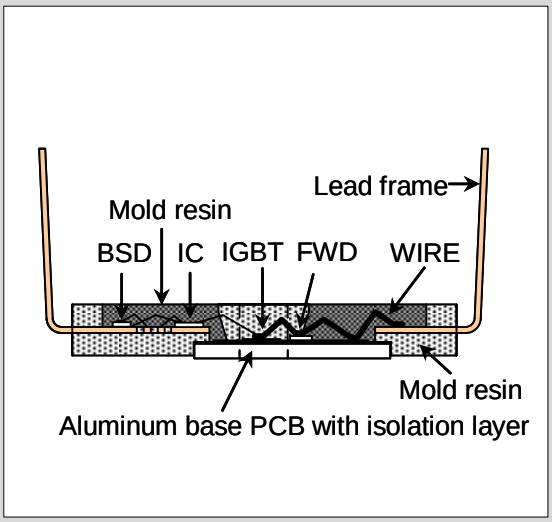


Fig.1-3 Package cross section diagram

2. Product line-up and applicable products for this manual

Table. 1-1 Line-up

Type name	Rating of IGBT		Isolation Voltage [Vrms]	Variation*1
	Voltage [V]	Current [A]		
6MBP15XSD060-50	600	15	1500Vrms Sinusoidal 60Hz, 1min. (Between all shorted terminals and case)	LT
6MBP15XSF060-50				LT OH
6MBP20XSD060-50		20		LT
6MBP20XSF060-50				LT OH
6MBP30XSD060-50		30		LT
6MBP30XSF060-50				LT OH
6MBP35XSD060-50		35		LT
6MBP35XSF060-50				LT OH

*1 LT: Temperature sensor output function
OH: Overheating protection function

3. Definition of Type Name and Marking Spec

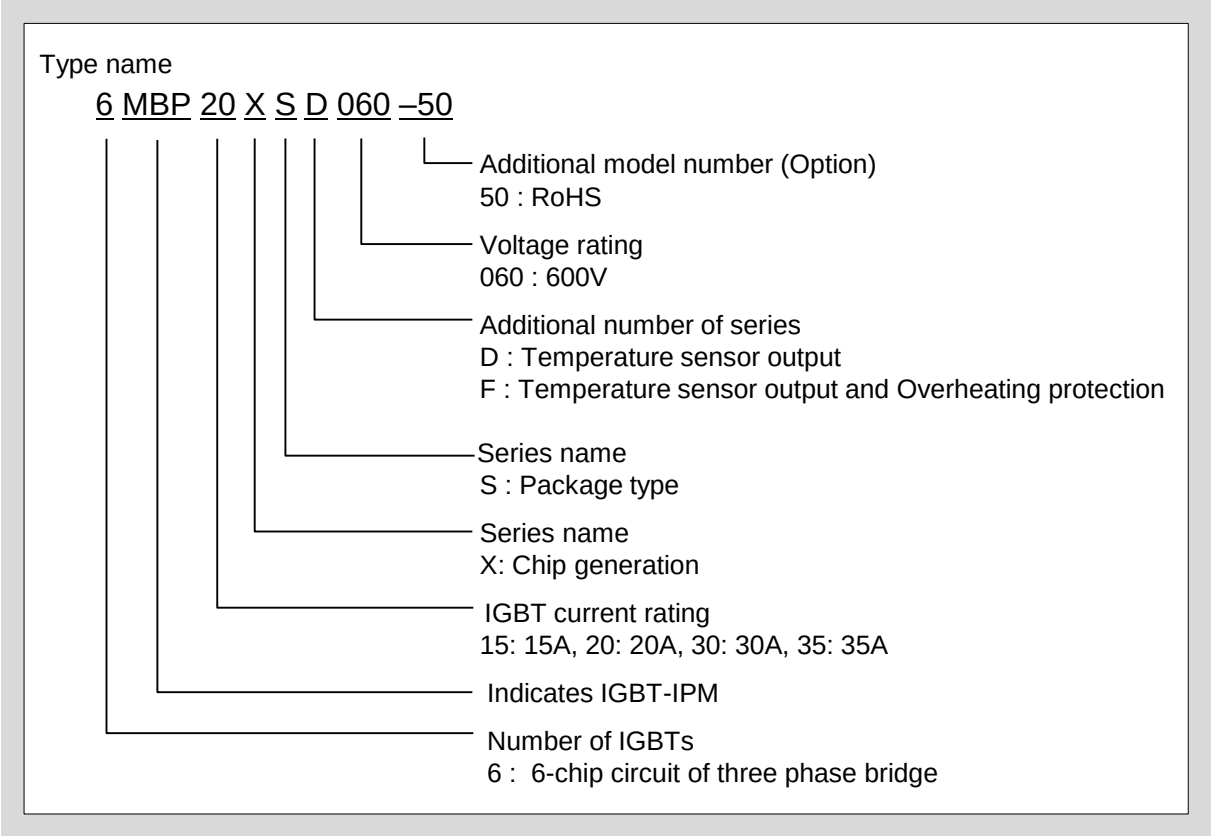


Fig.1-4 Part numbers

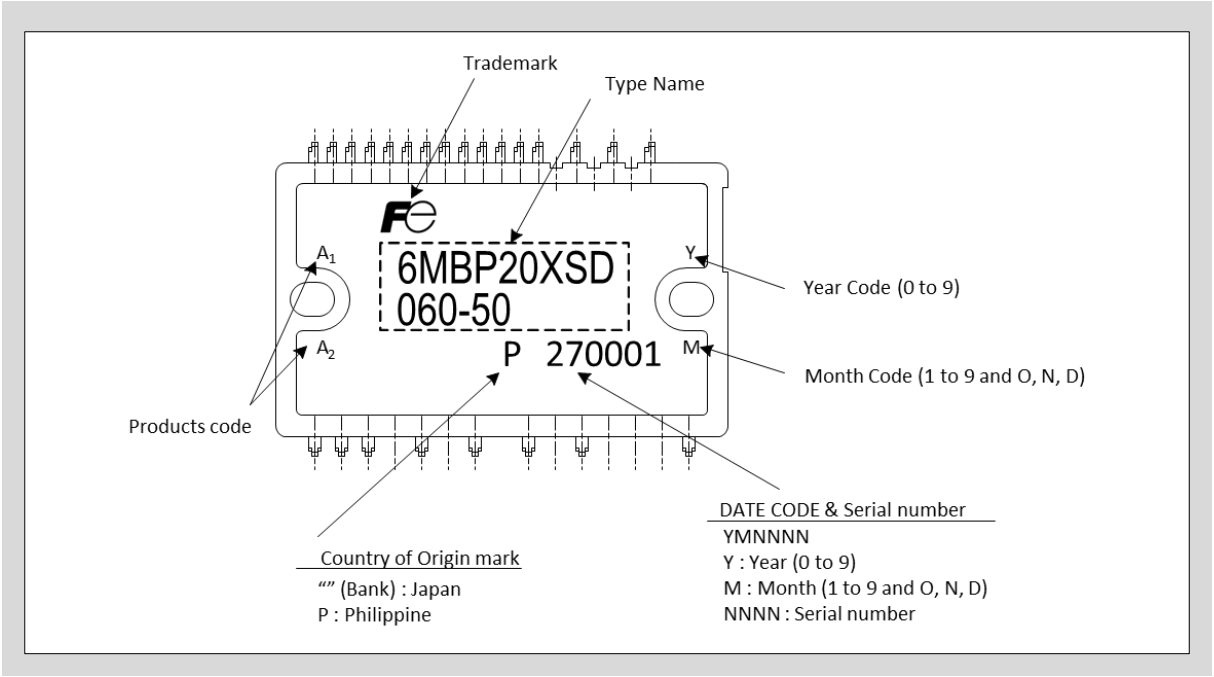
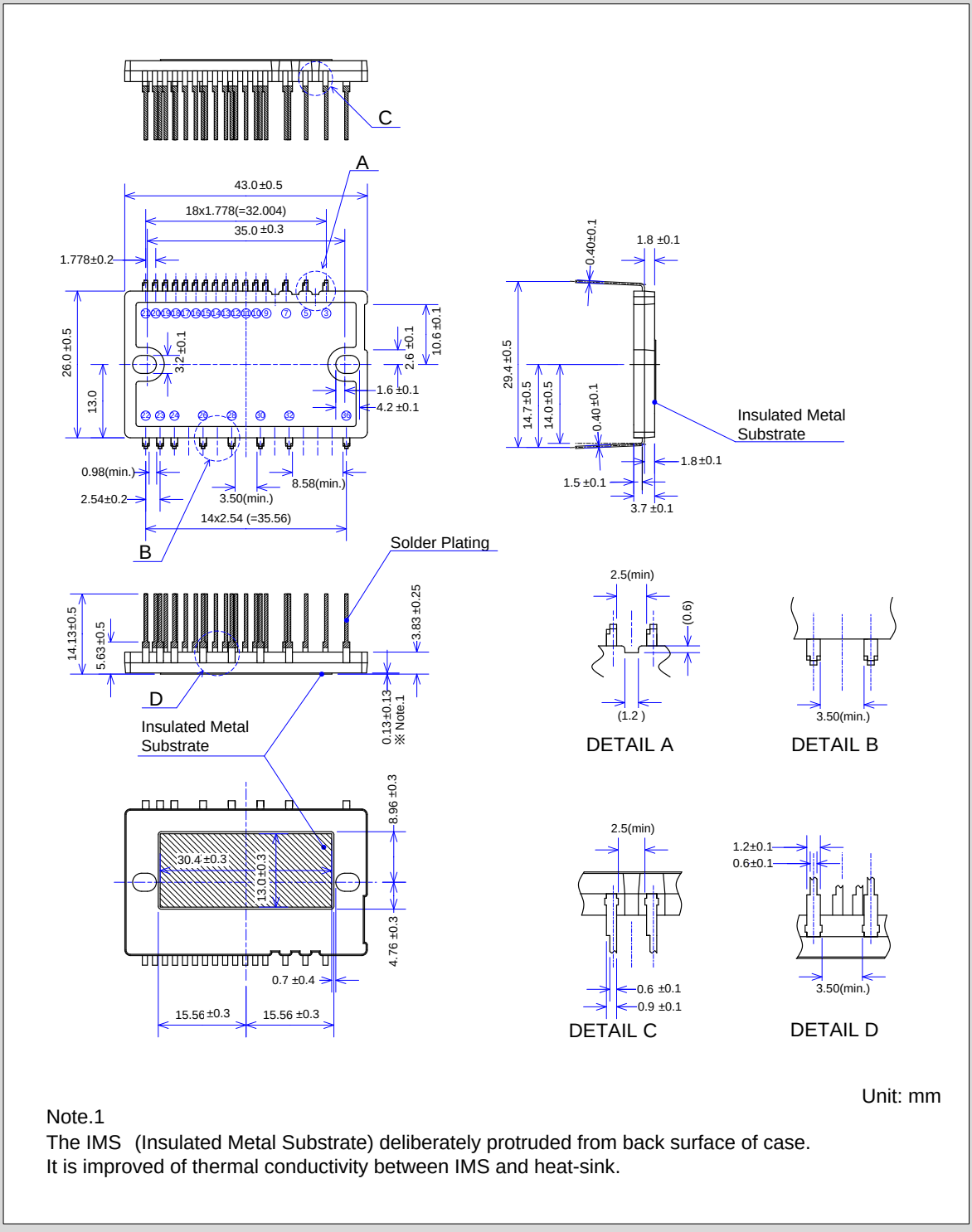


Fig.1-5 Marking Specification

Table. 1-2 Products code

TYPE NAME	PRODUCTS CODE	
	A1	A2
6MBP15XSD060-50	L	D
6MBP15XSF060-50	L	F
6MBP20XSD060-50	M	D
6MBP20XSF060-50	M	F
6MBP30XSD060-50	O	D
6MBP30XSF060-50	O	F
6MBP35XSD060-50	P	D
6MBP35XSF060-50	P	F

4. Package Outline dimensions



Unit: mm

Note.1
The IMS (Insulated Metal Substrate) deliberately protruded from back surface of case.
It is improved of thermal conductivity between IMS and heat-sink.

Fig.1-6 Case outline drawings

Table. 1-3 Case outline drawings

Pin No.	Pin Name	Pin No.	Pin Name
3	VB(U)	22	N(W)
5	VB(V)	23	N(V)
7	VB(W)	24	N(U)
9	IN(HU)	26	W
10	IN(HV)	28	V
11	IN(HW)	30	U
12	VCCH	32	P
13	COM	36	NC
14	IN(LU)		
15	IN(LV)		
16	IN(LW)		
17	VCCL		
18	VFO		
19	IS		
20	COM		
21	TEMP		

5. Absolute Maximum Ratings

An example of the absolute maximum ratings of 6MBP20XSD060-50 is shown in Table 1-4.

Table 1-4 Absolute Maximum Ratings at T_{vj}=25°C,V_{CC}=15V (unless otherwise specified)

Item	Symbol	Rating	Unit	Description
DC Bus Voltage	V_{DC}	450	V	DC voltage that can be applied between P-N(U),N(V),N(W) terminals
Bus Voltage (Surge)	$V_{DC(Surge)}$	500	V	Peak value of the surge voltage that can be applied between P-N(U),N(V),N(W) terminals during switching operation
Collector-Emitter Voltage	V_{CES}	600	V	Maximum voltage that can be applied between collector and emitter with V_{IN}-COM shorted
Collector Current	I_C	20	A	Maximum collector current for the IGBT chip T_c=25°C, T_{vj}=150°C
Peak Collector Current	I_{CP}	40	A	Maximum pulse collector current for the IGBT chip T_c=25°C, T_{vj}=150°C
Forward Current	I_F	20	A	Maximum forward current for the FWD chip T_c=25°C, T_{vj}=150°C
Peak Forward Current	I_{FP}	40	A	Maximum pulse forward current for the FWD chip T_c=25°C, T_{vj}=150°C
Collector Power Dissipation	P_{D_IGBT}	41.0	W	Maximum power dissipation for one IGBT element at T_c=25°C, T_{vj}=150°C
FWD Power Dissipation	P_{D_FWD}	27.8	W	Maximum power dissipation for one FWD element at T_c=25°C, T_{vj}=150°C
Virtual Junction Temperature of Inverter Block	T_{vj}	+150	°C	Maximum virtual junction temperature of the IGBT chips and the FWD chips. Operating life is limited by junction temperature and power cycle.
Operating Virtual Junction Temperature of Inverter Block	T_{vjOP}	-40 ~ +150	°C	Junction temperature of the IGBT and FWD chips during continuous operation. Operating life is limited by junction temperature and power cycle.

Table 1-5 Absolute Maximum Ratings at T_{vj}=25°C,V_{CC}=15V (Continued)

Item	Symbol	Rating	Unit	Descriptions
High-side Supply Voltage	V_{CCH}	-0.5 ~ 20	V	Voltage that can be applied between COM and V_{CCH} terminal
Low-side Supply Voltage	V_{CCL}	-0.5 ~ 20	V	Voltage that can be applied between COM and V_{CCL} terminal
High-side Bias Absolute Voltage	$V_{B(U)-COM}$ $V_{B(V)-COM}$ $V_{B(W)-COM}$	-0.5 ~ 620	V	Voltage that can be applied between VB(U)-COM, VB(V)-COM,VB(W)-COM terminal
High-side Bias Voltage for IGBT Gate Driving	$V_{B(U)}$ $V_{B(V)}$ $V_{B(W)}$	20	V	Voltage that can be applied between U-VB(U), V-VB(V), W-VB(W) terminal
Input Signal Voltage	V_{IN}	-0.5 ~ V_{CCH}+0.5 -0.5 ~ V_{CCL}+0.5	V	Voltage that can be applied between IN(*)-COM terminal
Input Signal Current	I_{IN}	3	mA	Maximum input current that flows from IN(*) to COM terminal
Fault Signal Voltage	V_{FO}	-0.5 ~ V_{CCL}+0.5	V	Voltage that can be applied between COM and VFO terminal
Fault Signal Current	I_{FO}	1	mA	Sink current that flows from VFO to COM terminal
Over Current Sensing Input Voltage	V_{IS}	-0.5 ~ V_{CCL}+0.5	V	Voltage that can be applied between IS and COM terminal
Maximum Junction Temperature of Control Circuit Block	T_{vj}	+150	°C	Maximum junction temperature of the control circuit block
Operating Case Temperature	T_c	-40 ~ +125	°C	Operating case temperature (temperature of the aluminum plate directly under the IGBT or the FWD)
Storage Temperature	T_{stg}	-40 ~ +125	°C	Range of ambient temperature for storage or transportation, when there is no electrical load
Isolation Voltage	V_{iso}	AC 1500	Vrms	Maximum effective value of the sine-wave voltage between the terminals and the heat sink, when all terminals are shorted simultaneously. (Sine wave = 60Hz / 1min)

<Absolute Maximum Rating of Collector-Emitter Voltage>

During operation of the Small IPM, the voltage between P-N(U, V, W) is usually applied to one phase of upper or lower side IGBT. Therefore, the voltage applied between P-N(U, V, W) must not exceed the absolute maximum ratings of IGBT.

V_{CES} : Absolute Maximum rating of IGBT Collector-Emitter Voltage.

V_{DC} : DC bus voltage applied between P-N(U, V, W) .

$V_{DC(Surge)}$: The total of DC bus voltage and surge voltage generated by the wiring (or pattern) inductance between P-N(U, V, W) terminal and bulk capacitor.

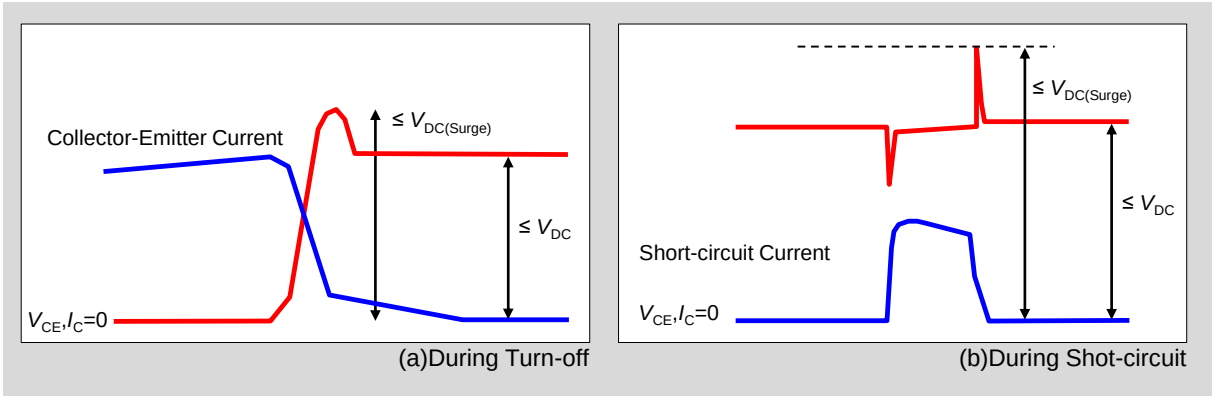


Fig. 1-7 Collector-Emitter voltage

Fig. 1-7 shows example of (a) turn-off and (b) short-circuit waveforms.
The $V_{DC(surge)}$ is different in each situation, therefore V_{DC} should be set considering these situations.
V_{CES} represents the absolute maximum rating of IGBT Collector-Emitter voltage.
$V_{DC(Surge)}$ is specified considering the margin of the surge voltage generated by wiring inductance.
V_{DC} is specified considering the margin of the surge voltage generated by wiring (or pattern) stray inductance between the P-N(U, V, W) terminal and bulk capacitor.

Chapter 2 Description of Terminal Symbols and Terminology

1. Description of Terminal Symbols

Table 2-1 describes the terminal symbols, and Table 2-2 to 2-6 explain the definitions.

Table 2-1 Description of Terminal Symbols

Pin No.	Pin Name	Pin Description
3	VB(U)	High side bias voltage for U-phase IGBT driving
5	VB(V)	High side bias voltage for V-phase IGBT driving
7	VB(W)	High side bias voltage for W-phase IGBT driving
9	IN(HU)	Signal input for high side U-phase
10	IN(HV)	Signal input for high side V-phase
11	IN(HW)	Signal input for high side W-phase
12	VCCH	High side control supply
13	COM	Common supply ground
14	IN(LU)	Signal input for low side U-phase
15	IN(LV)	Signal input for low side V-phase
16	IN(LW)	Signal input for low side W-phase
17	VCCL	Low side control supply
18	VFO	Fault output
19	IS	Over current sensing voltage input
20	COM	Common supply ground
21	TEMP	Temperature sensor output
22	N(W)	Negative bus voltage input for W-phase
23	N(V)	Negative bus voltage input for V-phase
24	N(U)	Negative bus voltage input for U-phase
26	W	Motor W-phase output
28	V	Motor V-phase output
30	U	Motor U-phase output
32	P	Positive bus voltage input
36	NC	No Connection

2. Description of Terminology

Table 2-2 Description of Terminology(Inverter block)

Item	Symbol	Description
Zero gate Voltage Collector current	I_{CES}	Collector current when a specified voltage is applied between the collector and emitter of an IGBT with all input signals L (=0V)
Collector-Emitter saturation voltage	$V_{CE(sat)}$	Collector-emitter voltage at a specified collector current when the input signal of only the element to be measured is H (= 5V) and the inputs of all other elements are L (=0V)
Forward voltage	V_F	Forward voltage at a specified forward current with all input signals L (=0V)
Turn-on time	t_{on}	The time from the input signal rising above the threshold value until the collector current becomes 90% of the rating. See Fig. 2-1.
Turn-on delay time	$t_{d(on)}$	The time from the input signal rising above the threshold value until the collector current decreases to 10% of the rating. See Fig. 2-1.
Turn-on rise time	t_r	The time from the collector current becoming 10% at the time of IGBT turn-on until the collector current becomes 90%. See Fig. 2-1.
V_{CE}-I_C Cross time of turn-on	$t_{c(on)}$	The time from the collector current becoming 10% at the time of IGBT turn-on until the V_{CE} voltage of IGBT dropping below 10% of the rating. See Fig. 2-1.
Turn-off time	t_{off}	The time from the input signal dropping below the threshold value until the V_{CE} voltage of IGBT becomes 90% of the rating. See Fig. 2-1.
Turn-off delay time	$t_{d(off)}$	The time from the input signal dropping below the threshold value until the collector current decreases to 90%. See Fig. 2-1.
Turn-on fall time	t_f	The time from the collector current becoming 90% at the time of IGBT turn-off until the collector current decreases to 10%. See Fig. 2-1.
V_{CE}-I_C Cross time of turn-off	$t_{c(off)}$	The time from the V_{CE} voltage becoming 10% at the time of IGBT turn-off until the collector current dropping below 10% of the rating. See Fig. 2-1.
Reverse Recovery time	t_{rr}	The time required for the reverse recovery current of the built-in diode to disappear. See Fig. 2-1.

Table 2-3 Description of Terminology(Control circuit block)

Item	Symbol	Description
Circuit current of Low-side drive IC	I_{CCL}	Current flowing between control power supply V_{CCL} and COM
Circuit current of High-side drive IC	I_{CCH}	Current flowing between control power supply V_{CCH} and COM

Table 2-3 (Continued)

Item	Symbol	Description
Circuit current of Bootstrap circuit	I_{CCHB}	Current flowing between upper side IGBT bias voltage supply VB(U) and U,VB(V) and V or VB(W) and W on the P-side (per one unit)
Input Signal threshold voltage	$V_{th(on)}$	Control signal voltage when IGBT changes from OFF to ON
	$V_{th(off)}$	Control signal voltage when IGBT changes from ON to OFF
Input Signal threshold hysteresis voltage	$V_{th(hys)}$	The hysteresis voltage between $V_{th(on)}$ and $V_{th(off)}$.
Operational input pulse width of turn-on	$t_{IN(on)}$	Control signal pulse width necessary to change IGBT from OFF to ON. Refer to Chapter 3 section 4.
Operational input pulse width of turn-off	$t_{IN(off)}$	Control signal pulse width necessary to change IGBT from ON to OFF. Refer to Chapter 3 section 4.
Input current	I_{IN}	Current flowing between signal input IN(HU,HV,HW,LU,LV,LW) and COM.
Input pull-down resistance	R_{IN}	Resistance of resistor connected between each input terminals IN(HU,HV,HW,LU,LV,LW) and COM.
Fault Output voltage	$V_{FO(H)}$	Output voltage level of VFO terminal under the normal operation (The lower side arm protection function is not actuated.) with pull-up resistor 10kW.
	$V_{FO(L)}$	Output voltage level of VFO terminal after the lower side arm protection function is actuated.
Fault Output pulse width	t_{FO}	Period in which an fault status continues to be output (V_{FO}) from the VFO terminal after the lower side arm protection function is actuated. Refer to Chapter 3 section 6.
Over Current Protection voltage level	$V_{IS(ref)}$	Threshold voltage of IS terminal at the over current protection. Refer to Chapter 3 section 5.
Over Current Protection delay time	$t_{d(IS)}$	The time from the Over current protection triggered until the collector current becomes 50% of the rating. Refer to Chapter 3 section 5.
Output Voltage of temperature sensor	$V_{(temp)}$	The output voltage of temp. It is applied to the temperature sensor output model. Refer to Chapter 3 section 7.
LVIC overheating protection	T_{OH}	Tripping temperature of overheating protection. The temperature is monitored by LVIC. All low side IGBTs are shut down when the LVIC temperature exceeds T_{OH}. See Fig.2-2 and refer to Chapter 3 section 8.
LVIC overheating protection hysteresis	$T_{OH(hys)}$	Hysteresis temperature that does not reset the overheating protection operation. See Fig.2-2 and refer to Chapter 3 section 8. T_{OH} and $T_{OH(hys)}$ are applied to the overheating protection model.
V_{CC} Under Voltage Trip Level of Low-side	$V_{CCL(OFF)}$	Tripping voltage of the low-side control IC power supply. All low side IGBTs are shut down when the voltage of V_{CCL} drops below this threshold. Refer to Chapter 3 section 1.

Table 2-3 (Continued)

Item	Symbol	Description
V_{CC} under voltage reset level of Low-side	$V_{CCL(ON)}$	Resetting threshold voltage from under voltage trip status of V_{CCL}. Refer to Chapter 3 section 1.
V_{CC} under voltage hysteresis of Low-side	$V_{CCL(hys)}$	Hysteresis voltage between $V_{CCL(OFF)}$ and $V_{CCL(ON)}$.
V_{CC} Under Voltage Trip Level of High-side	$V_{CCH(OFF)}$	Tripping voltage of high-side control IC power supply. The IGBTs of high-side are shut down when the voltage of V_{CCH} drops below this threshold. Refer to Chapter 3 section 1.
V_{CC} Under Voltage Reset Level of High-side	$V_{CCH(ON)}$	Resetting threshold voltage from under voltage trip status of V_{CCH}. See Fig.3-3 Resetting voltage at which the IGBT performs shut down when the high-side control power supply voltage V_{CCH} drops. Refer to Chapter 3 section 1.
V_{CC} Under Voltage hysteresis of High-side	$V_{CCH(hys)}$	Hysteresis voltage between $V_{CCH(OFF)}$ and $V_{CCH(ON)}$.
V_B Under Voltage Trip Level	$V_{B(OFF)}$	Tripping voltage V_B(*) under voltage. The high-side IGBTs are shut down when the voltage of V_B(*) drops below this threshold. Refer chapter 3 section 2.
V_B Under Voltage Reset Level	$V_{B(ON)}$	Resetting voltage at which the IGBT performs shut down when the upper side arm IGBT bias voltage V_B(*) drops. Refer to Chapter 3 section 2.
V_B Under Voltage hysteresis	$V_{B(hys)}$	Hysteresis voltage between $V_{B(OFF)}$ and $V_{B(ON)}$.

*1 : V_B(*) is applied between VB(U)-U, VB(V)-V, VB(W)-W.

Table 2-4 BSD block

Item	Symbol	Description
Forward voltage of Bootstrap diode	$V_{F(BSD)}$	BSD Forward voltage at a specified forward current.

Table 2-5 Thermal Characteristics

Item	Symbol	Description
Junction to Case Thermal Resistance (per single IGBT)	$R_{th(j-c)\_IGBT}$	Thermal resistance from the junction to the case of a single IGBT.
Junction to Case Thermal Resistance (per single FWD)	$R_{th(j-c)\_FWD}$	Thermal resistance from the junction to the case of a single FWD.

Table 2-6 Mechanical Characteristics

Item	Symbol	Description
Mounting torque	–	Screwing torque when mounting the Small IPM to a heat sink with a specified screw.
Heat-sink side flatness	–	Flatness of a heat sink side. See Fig.2-3.

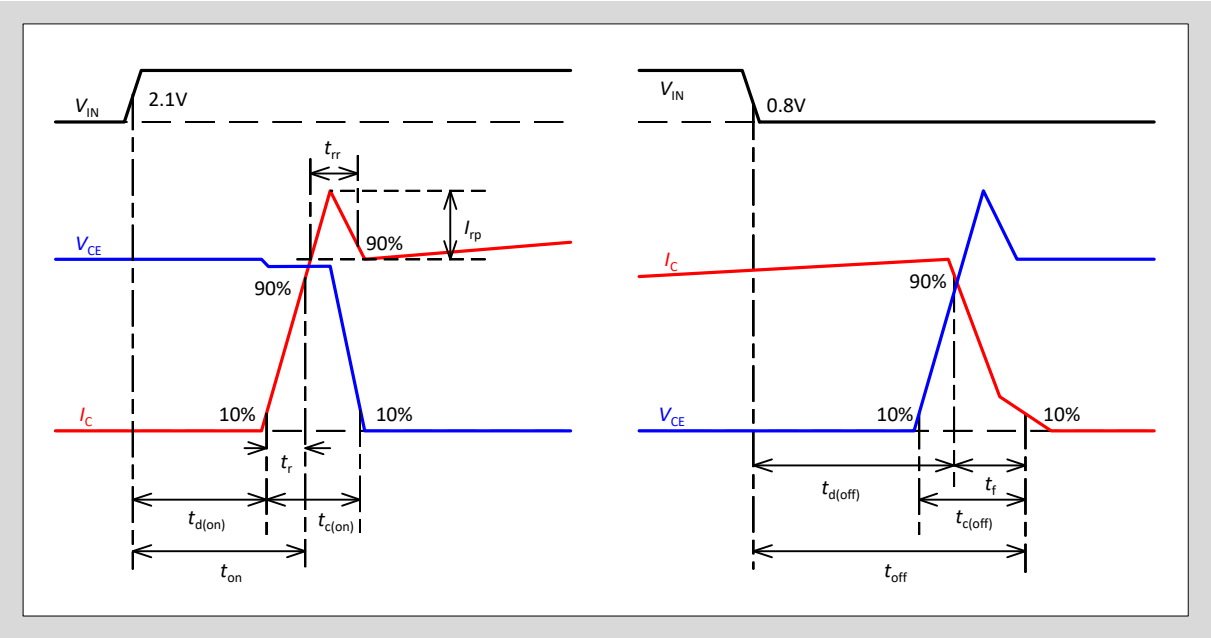


Fig.2-1 Switching waveforms

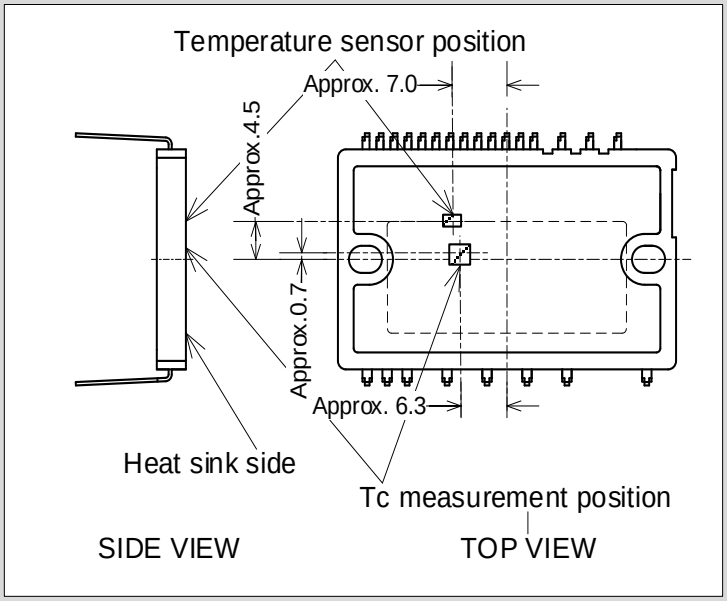


Fig.2-2 The measurement position of temperature sensor and Tc.

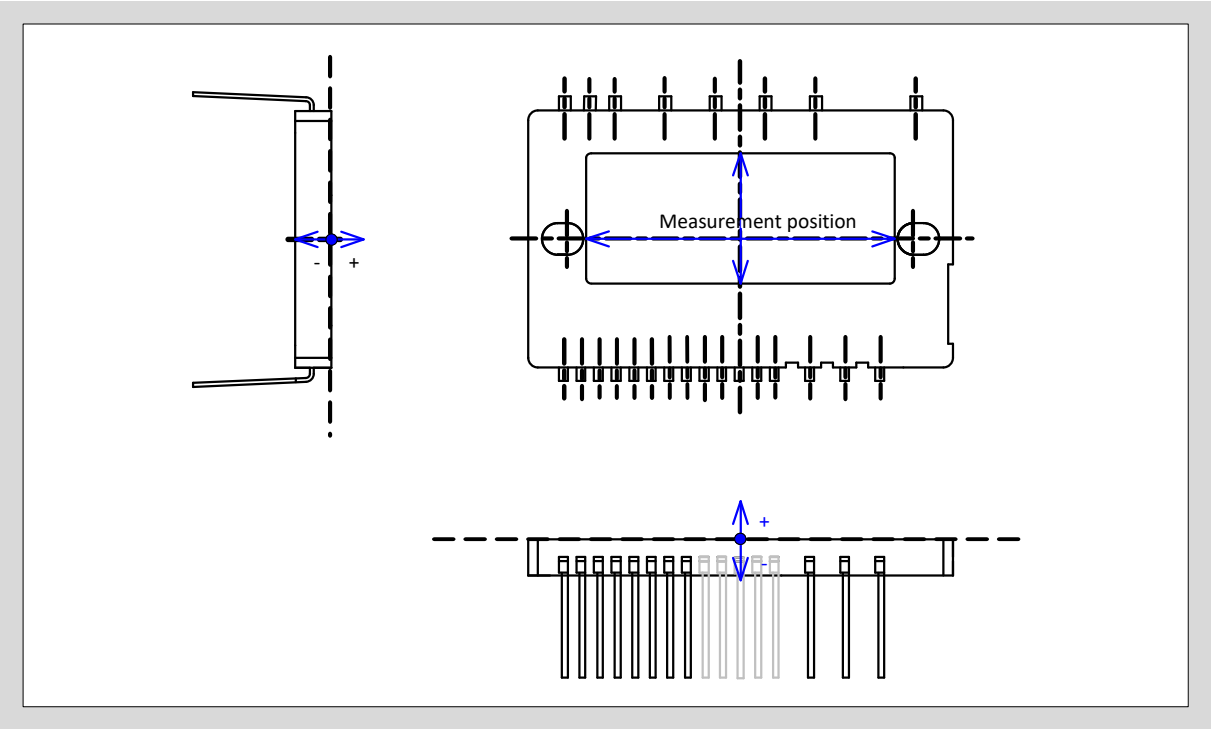


Fig.2-3 The measurement point of heat-sink side flatness.

Chapter 3 Details of Signal Input/Output Terminals

1. Control Power Supply Terminals VCCH, VCCL, COM

<Voltage Range of control power supply terminals VCCH, VCCL>

- For control supply voltage, please connect a 15V±10% DC power supply between VCCH, VCCL and COM terminals.
- Table 3-1 describes the operation of the product for various control supply voltages. A low impedance capacitor and a high frequency decoupling capacitor should be connected close to the terminals of the power supply.
- High frequency noise on the power supply might cause malfunction of the internal control IC or erroneous fault signal output. To avoid these problems, the maximum amplitude of voltage ripple on the power supply should be less than ±1V/μs.
- The potential at the COM terminal is different from that at the N(U, V, W) power terminal. It is very important that all control circuits and power supplies are referred to the COM terminal and not to the N(U, V, W) terminals. If circuits are improperly connected, current might flow through the shunt resistor and cause improper operation of the short-circuit protection function. In general, it is recommended to make the COM terminal as the ground potential in the PCB layout.
- The main control power supply is also connected to the bootstrap circuit which provide a power to floating supplies for the high side gate drivers.
- When high-side control supply voltage V_{CCH} falls below $V_{CCH(OFF)}$, only the IGBT which occurred the under voltage condition becomes off-state even though input signal is ON condition.
- When low-side control supply voltage V_{CCL} falls below $V_{CCL(OFF)}$, all lower side IGBTs become off-state even though the input signal is ON condition.

Table 3-1 Functions versus supply voltage V_{CCH}, V_{CCL}

Control Voltage Range [V]	Operations and functions
0 ~ 4	The product doesn't operate. UV and fault output are not activated. *dV*/*d*t noise on the main P-N supply might cause malfunction of the IGBTs.
4 ~ 13	The product starts to operate. UV is activated, control input signals are blocked and fault output VFO is generated.
13 ~ 13.5	UV is reset. IGBTs perform switching in accordance to input signal. Drive voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition. High side IGBTs do not switch until V_B(*)*1 reaches $V_{B(ON)}$ after initial charging.
13.5 ~ 16.5	Normal operation. This is the recommended operating condition.
16.5 ~ 20	IGBTs perform switching. Because drive voltage is above the recommended range, IGBT's switching is faster and causes an increase in system noise. Even with proper overcurrent protection design, the short-circuit peak current can become very large and might lead to failure.
Over 20	Control circuit in the product might be damaged. It is recommended to insert a Zener diode between each pair of control supply terminals if necessary.

*1 : V_B(*) is applied between VB(U)-U, VB(V)-V, VB(W)-W.

<Under Voltage (UV) protection of control power supply terminals VCCH, VCCL>

- Fig.3-1 shows the UV protection circuit of VCCH and VCCL.
- Fig.3-2 and Fig.3-3 shows the operation sequence of UV operation of V_{CCH} and V_{CCL}.
- As shown in Fig.3-1, a diode is connected between VCCH-COM and VCCL-COM terminals. The diode is connected to protect the Small IPM from the input surge voltage. Do not use the diode for voltage clamp purpose otherwise the product might be damaged.

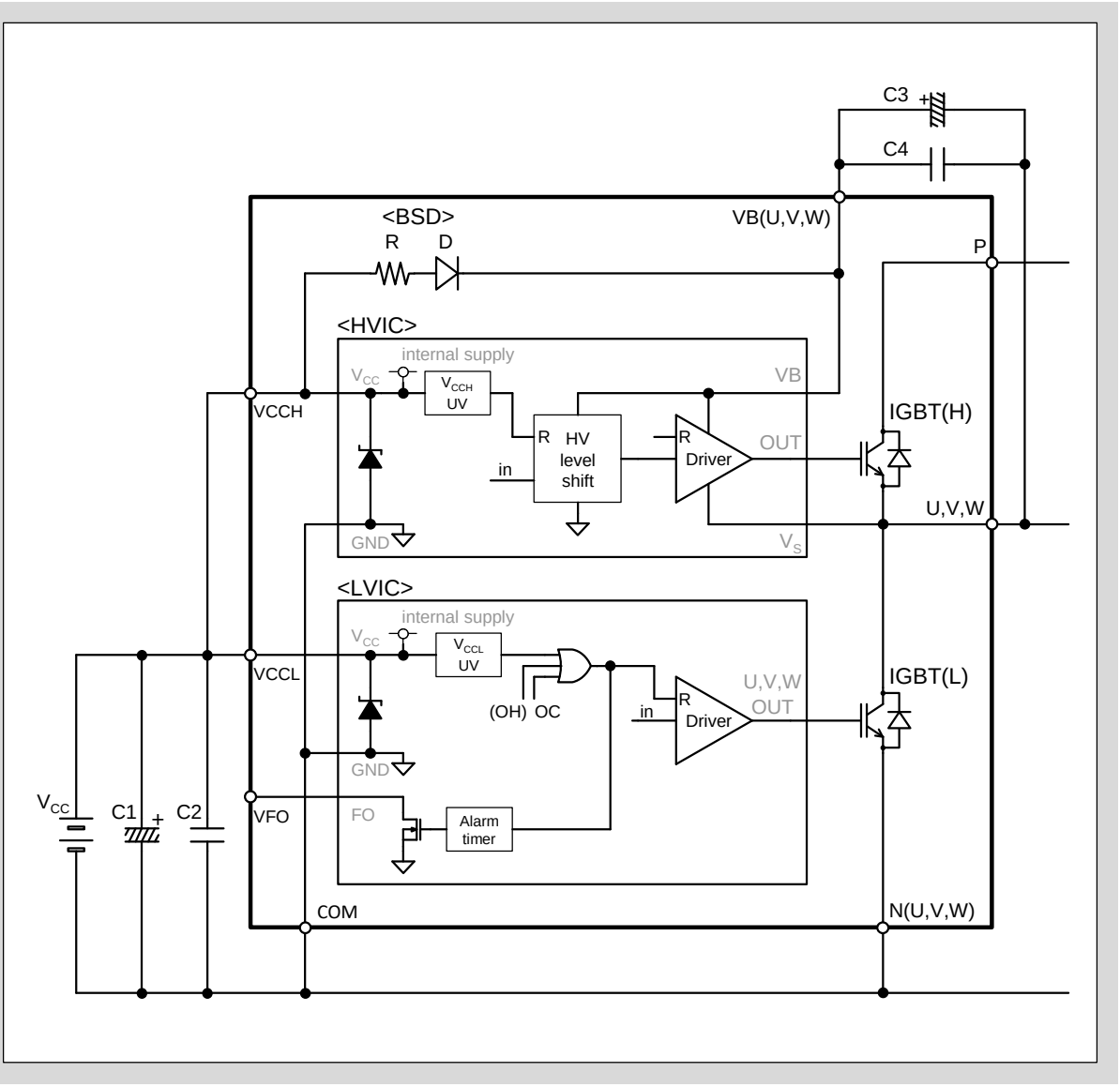


Fig.3-1 UV protection circuit of VCCH, VCCL

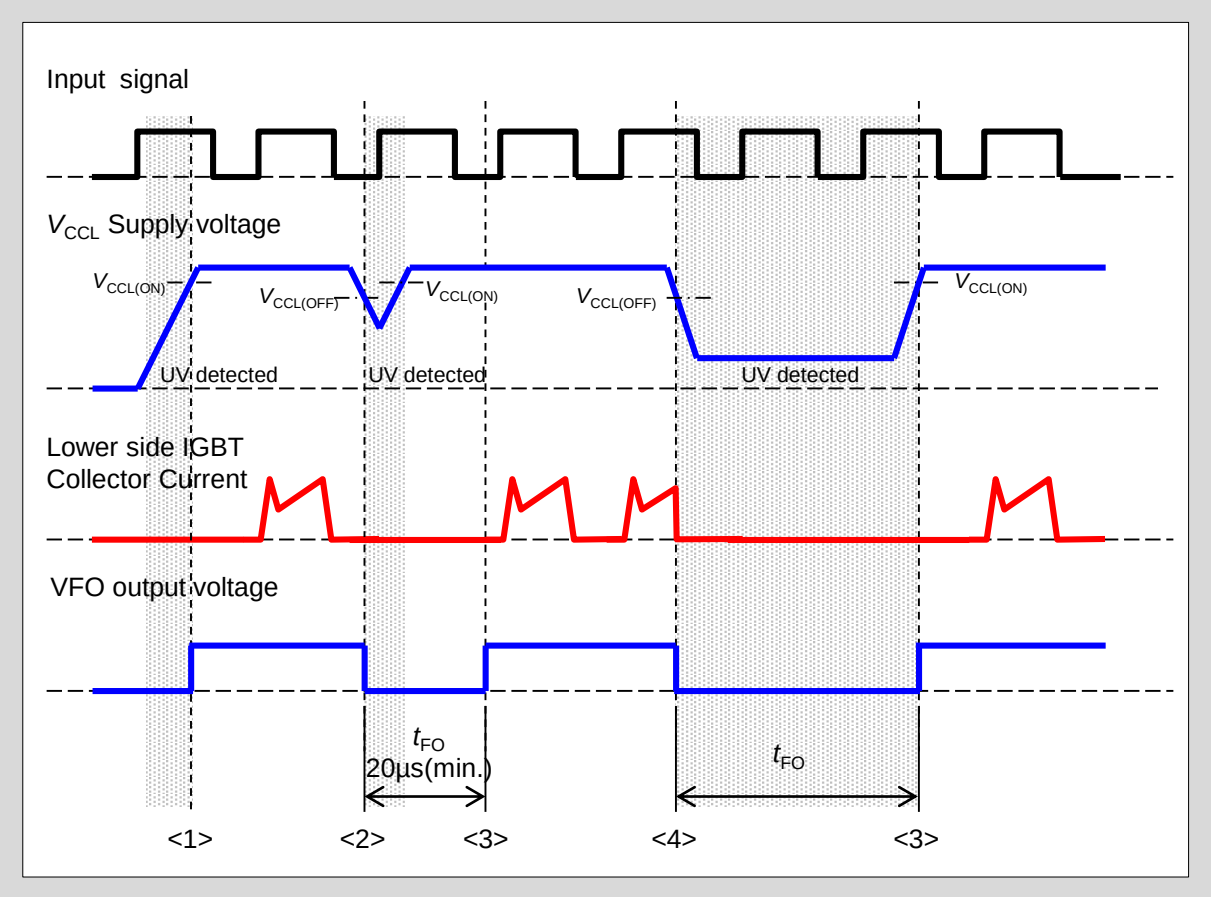


Fig.3-2 Operation sequence of V_{CCL} Under Voltage protection (lower side arm)

<1> When V_{CCL} is lower than $V_{CCL(ON)}$, all lower side IGBTs are OFF state.
After V_{CCL} exceeding $V_{CCL(ON)}$, the fault output VFO is released (high level).
And the LVIC starts to operate, then next input is activated.

<2> The fault output VFO is activated when V_{CCL} falls below $V_{CCL(OFF)}$, and all lower side IGBT remains OFF state.
If the voltage drop time is less than 20µs, the minimum pulse width of the fault output signal is 20µs and all lower side IGBTs are OFF state regardless of the input signal condition.

<3> UV is reset after t_{FO} and V_{CCL} exceeding $V_{CCL(ON)}$, then the fault output VFO is reset simultaneously.
After that the LVIC starts to operate from the next input signal.

<4> When the voltage drop time is more than t_{FO}, the fault output pulse width is generated and all lower side IGBTs are OFF state regardless of the input signal condition during the same time.

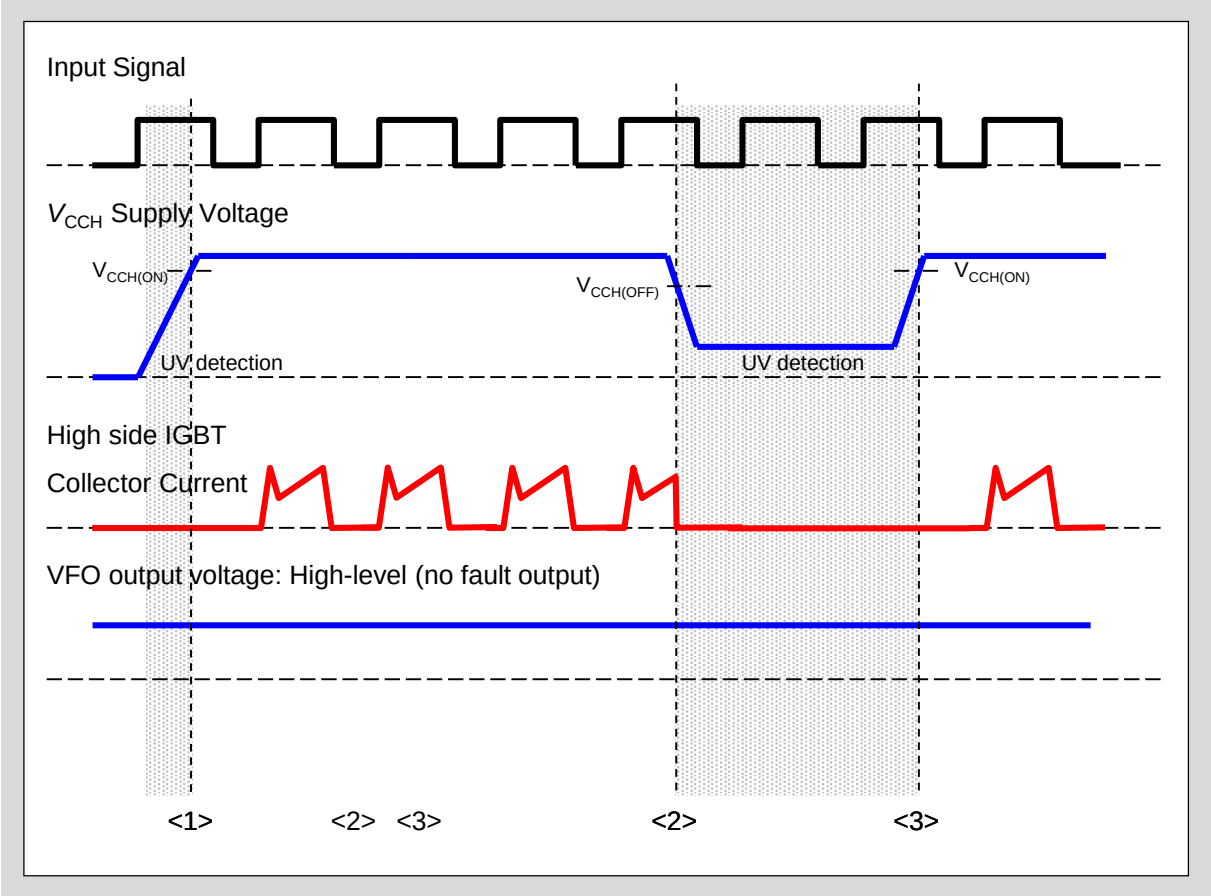


Fig.3-3 Operation sequence of V_{CCH} Under Voltage protection (high side)

<1> When V_{CCH} is lower than $V_{CCH(ON)}$, the upper side IGBT is OFF state.
After V_{CCH} exceeds $V_{CCH(ON)}$, the HVIC starts to operate from the next input signals.
The fault output VFO is constant (high level) regardless of V_{CCH}.
<2> After V_{CCH} falls below $V_{CCH(OFF)}$, the upper side IGBT remains OFF state.
But the fault output VFO keeps high level.
<3> The HVIC starts to operate from the next input signal after UV is reset.

2. Power Supply Terminals of High-Side VB(U, V, W)

<Voltage range of high-side bias voltage for IGBT driving terminals VB(U, V, W)>

- The V_B(*) voltage, which is the voltage difference between VB(U,V,W) and U,V,W, provides the power supply to the HVICs within the product.
- This power supply must be in the range of 13.0~18.5V to ensure that the HVICs can fully drive the high-side IGBTs. The product includes UV protection for V_B(*) to ensure that the HVICs do not drive the high-side IGBTs when V_B(*) drops below a specified voltage (refer to the datasheet). This function prevents the IGBT from operating in a high dissipation mode. Please note that the UV protection only works on the triggered phase and doesn't generate fault output.
- Conventionally, three isolated power supplies are necessary for IGBT drive at the high-side. In case of using bootstrap circuit, the IGBT drive power supply for high-side can be generated from the high-side/low-side control power supply.
- The power supply of the high-side is charged when the low-side IGBT is turned on or when freewheel current flows through the low-side FWD. Table 3-2 describes the operation of the product for various control supply voltages. The control supply should be well filtered with a low impedance capacitor and a high frequency decoupling capacitor connected close to the terminals in order to prevent malfunction of the internal control IC caused by a high frequency noise on the power supply.
- When V_B(*) falls below $V_{B(OFF)}$, only the triggered phase IGBT is off-state even though the input signal is provided.

Table 3-2 Functions versus high side bias voltage for IGBT driving V_B(*)

Control Voltage Range [V]	Operations and functions
0 ~ 4	HVICs are not activated. UV does not operate. d*V*/d*t* noise on the main P-N supply might trigger the IGBTs.
4 ~ 12.5	HVICs start to operate. As the UV is activated, control input signals are blocked.
12.5 ~ 13	UV is reset. The high side IGBTs perform switching in accordance to input signal. Driving voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition.
13 ~ 18.5	Normal operation. This is the recommended operating condition.
18.5 ~ 20	The high side IGBTs perform switching. Because drive voltage is above the recommended range, IGBT's switching is faster and causes an increase in system noise. Even with proper overcurrent protection design, the short-circuit peak current can become very large and might lead to failure.
Over 20	Control circuit in the product might be damaged. It is recommended to insert a Zener diode between each pair of high side power supply terminals.

<Under Voltage (UV) protection of high-side power supply terminals VB(U,V,W)>

- Fig.3-4 shows the UV protection circuit of high-side power supply VB(U, V, W).
- Fig.3-5 shows the operation sequence of UV operation of V_B(U), V_B(V), V_B(W).
- As shown in Fig.3-4, diodes are electrically connected to the VB(U,V,W)-(U,V,W) and VB(U,V,W)-COM terminals. These diodes protect the product from input surge voltage. Do not use these diodes for voltage clamp purpose otherwise the product might be damaged.

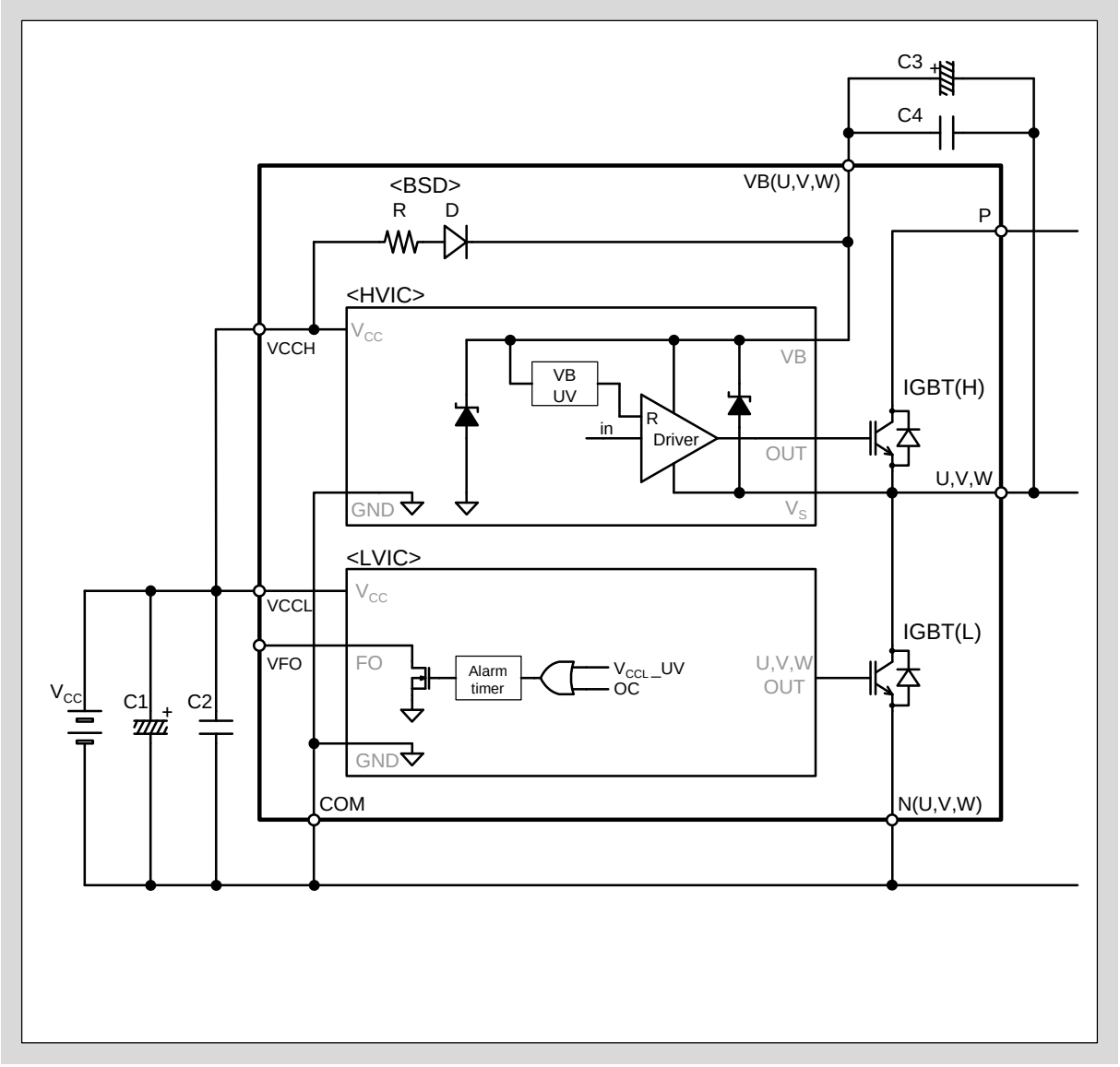


Fig.3-4 UV protection circuit of V_B(U, V, W)

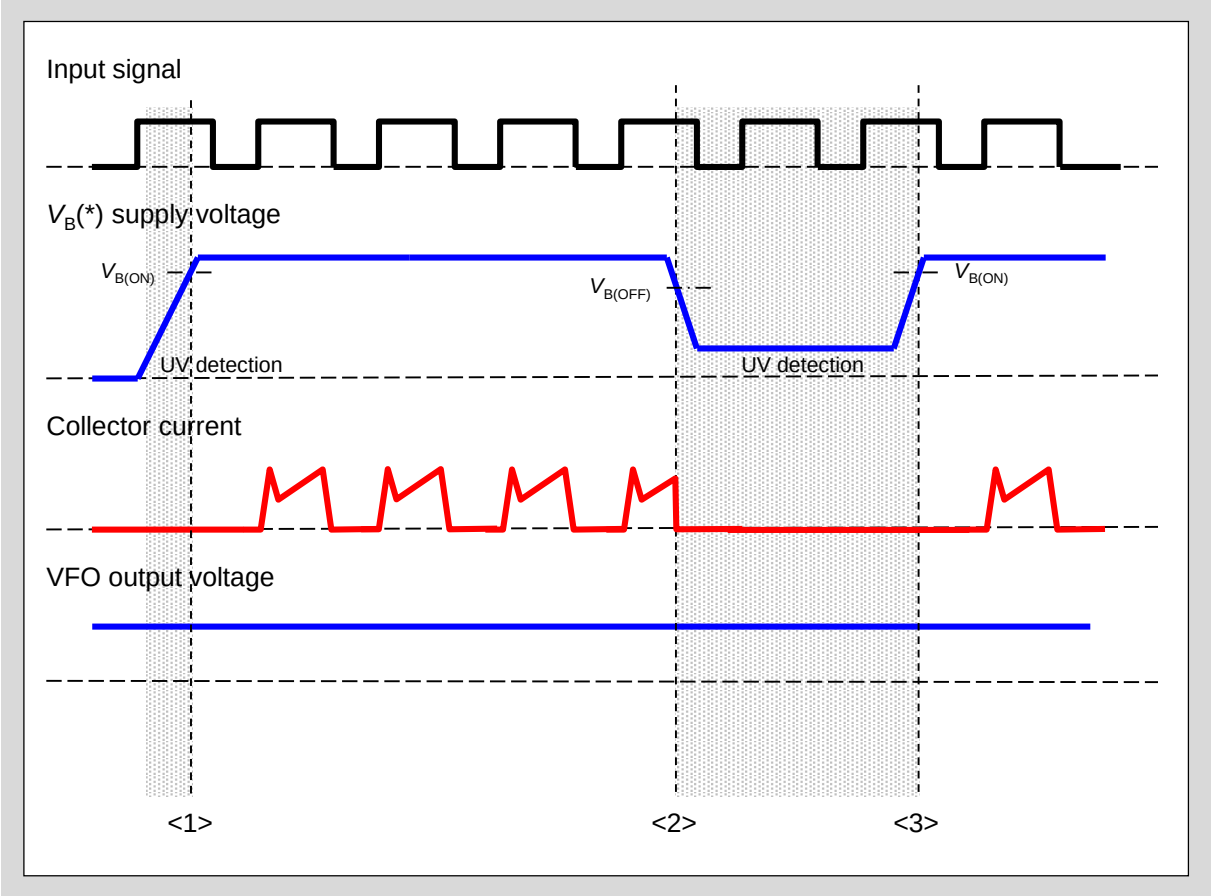


Fig.3-5 Operation sequence of V_B(*) Under voltage protection (high side)

<1> When V_B(*) is lower than $V_{B(ON)}$, the upper side IGBT is OFF state.
After V_B(*) exceeds $V_{B(ON)}$, the HVIC starts to operate from the next input signal.
The fault output VFO is constant (high level) regardless of V_B(*).
<2> After V_B(*) falls below $V_{B(OFF)}$, the high side IGBT remains OFF state.
But the fault output VFO keeps high level.
<3> The HVIC starts to operate from the next input signal after UV is reset.

*1 : V_B(*) is applied between VB(U)-U, VB(V)-V, VB(W)-W.

3. Function of Internal BSDs (bootstrap Diodes)

There are several ways in which the VB(U, V, W)-(U, V, W) floating supply can be generated. Bootstrap method is described here. The bootstrap method is a simple and cheap solution. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. As shown in Fig. 3-6, Fig. 3-8 and Fig. 3-11, the bootstrap circuit consists of bootstrap diode with current limiting resistor which are integrated in the Small IPM and an external capacitor.

<Charging and Discharging of Bootstrap Capacitor During Inverter Operation>

When low-side IGBT is ON state, the charging voltage on the bootstrap capacitance $V_{C(t1)}$ is calculated by the following equations. Fig.3-6 shows the circuit diagram of charging operation, and Fig.3-7 shows the timing chart.

$V_{C(t1)} = V_{CC} - V_{F(D)} - V_{CE(sat)} - I_b \cdot R$.....Transient state

$V_{C(t1)} \approx V_{CC}$.....Steady state

$V_{F(D)}$: Forward voltage of Boost strap diode D
$V_{CE(sat)}$: Saturation voltage of low side IGBT
R : Bootstrap resistance
I_b : Bootstrap charging current

When low-side IGBT is turned off, the motor current flows through the freewheel path of the high-side FWD. Once V_S rises above V_{CC}, the charging of C stops, and the voltage of C gradually declines due to current consumed by the drive circuit.

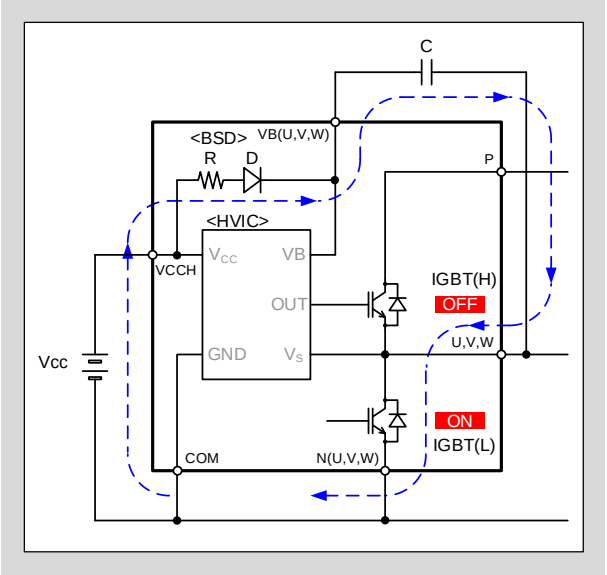


Fig.3-6 Circuit diagram of charging operation

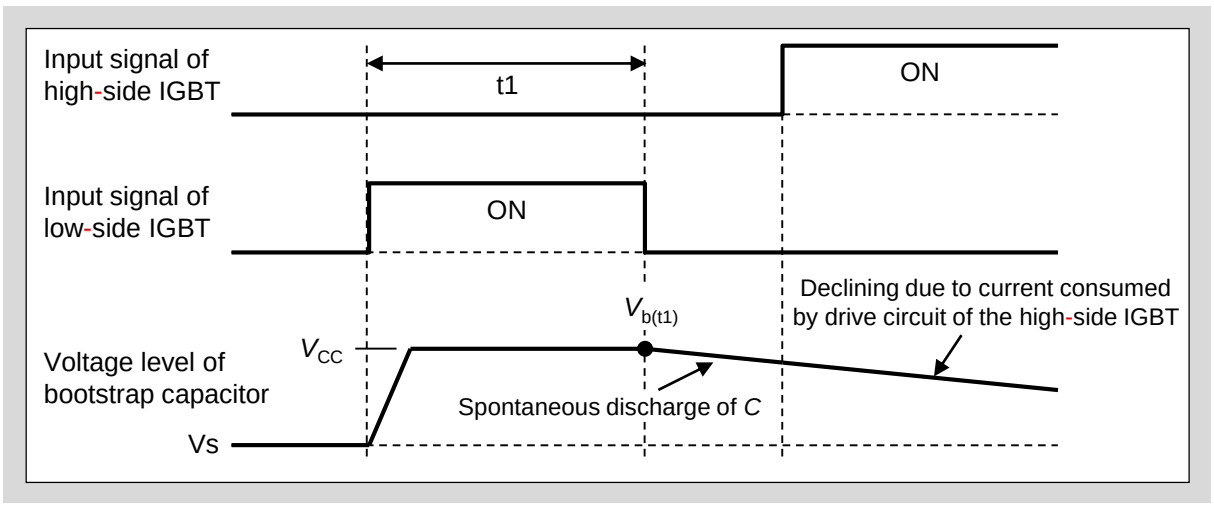


Fig.3-7 Timing chart of charging operation

When the low-side IGBT is OFF and the low-side FWD is ON, freewheeling current flows through the low-side FWD. The voltage on the bootstrap capacitance $V_{C(t2)}$ is calculated by the following equations. Fig.3-8 shows the circuit diagram of charging operation, and Fig.3-9 shows the timing chart.

$V_{C(t2)} = V_{CC} - V_F + V_{F(FWD)} - I_b \cdot R$.....Transient state
$V_{C(t2)} \approx V_{CC}$.....Steady state

$V_{F(D)}$: Forward voltage of Boost strap diode D
$V_{F(FWD)}$: Forward voltage of lower side FWD
R : Bootstrap resistance
I_b : Bootstrap charging current

When both the low-side and high-side IGBTs are OFF, a regenerative current flows continuously through the low-side FWD. Therefore V_s drops to $-V_F$ of FWD, then the bootstrap capacitor is re-charged to restore the declined potential. When the high-side IGBT is turned ON and V_s exceeds V_{CC}, the charging of the C stops, and the voltage of the C gradually declines due to current consumed by the drive circuit.

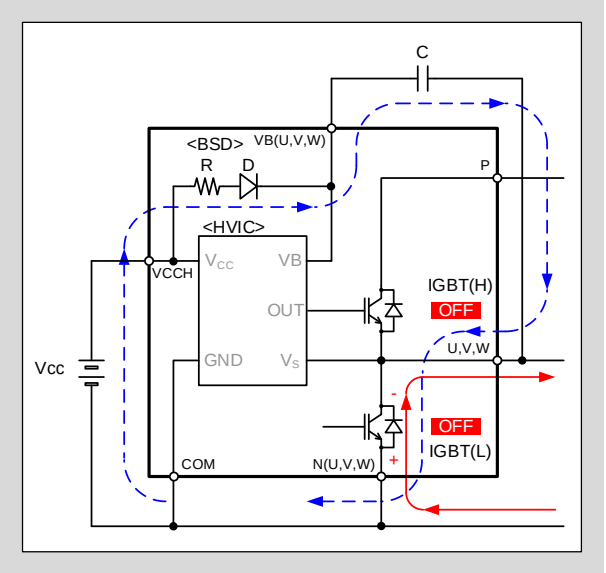


Fig.3-8 Circuit diagram of charging operation when the low-side FWD is ON

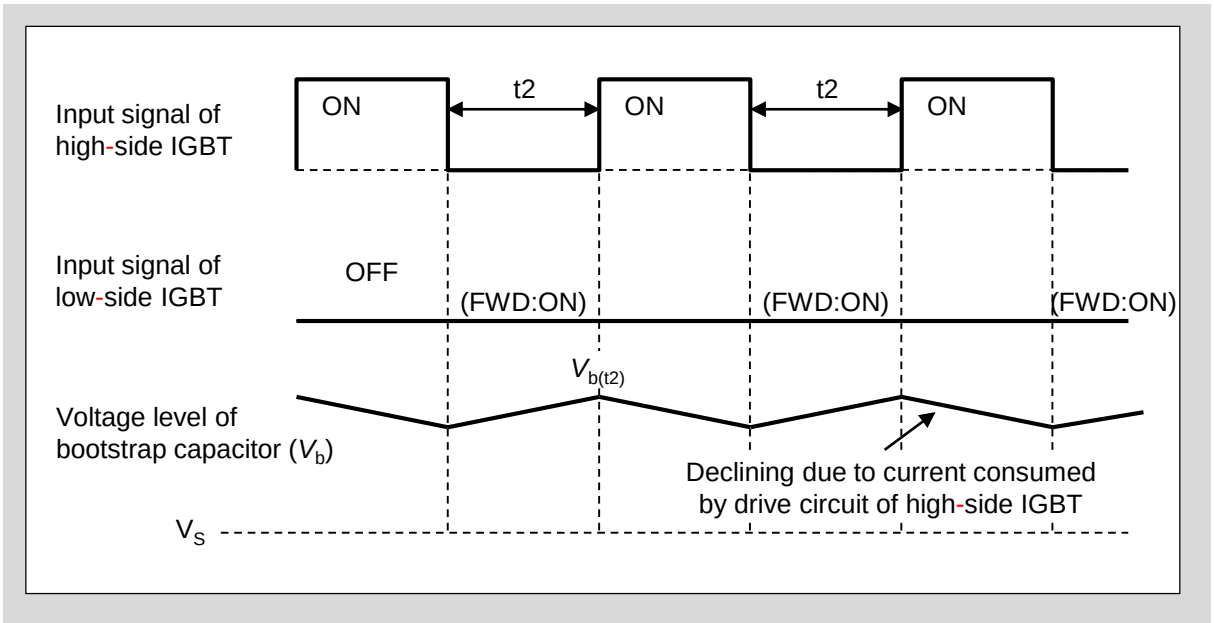


Fig.3-9 Timing chart of charging operation when the low-side FWD is ON

<Setting the bootstrap capacitance and minimum ON/OFF pulse width>

The parameter of bootstrap capacitor can be calculated by the following equation:

$$C = I_b \cdot \frac{t_1}{dV_b}$$

t_1 the maximum ON pulse width of the high-side IGBT

I_b: the drive current of the HVIC (depends on temperature and frequency characteristics)

dV_b: the allowable discharge voltage. (see Fig.3-10)

- A certain margin should be added to the calculated capacitance.
- The bootstrap capacitance is generally selected 2~3 times the value of the calculated result.
- The recommended minimum ON pulse width (t_2) of the low-side IGBT should be basically determined such that the time constant $C \cdot R$ will enable the discharged voltage (dV) to be fully charged again during the ON period.
- However, if the control mode only has the high-side IGBT switching (Sequence Fig.3-10), the time constant should be set so that the consumed energy during the ON period can be charged during the OFF period.
- The minimum pulse width is decided by the minimum ON pulse width of the low-side IGBT or the minimum OFF pulse width of the high-side IGBT, whichever is shorter.

$$t_2 \geq \frac{R \cdot C \cdot dV_b}{V_{CC} - V_{b(min)}}$$

R: Series resistance of Bootstrap diode ΔRF(BSD)

C: Bootstrap capacitance

dV: the allowable discharge voltage.

V_{CC} Voltage of HVICs and LVIC power supply (ex.15V)

$V_{b(min)}$: the minimum voltage of the high-side IGBT drive voltage (Added margin to UV. ex. 14V)

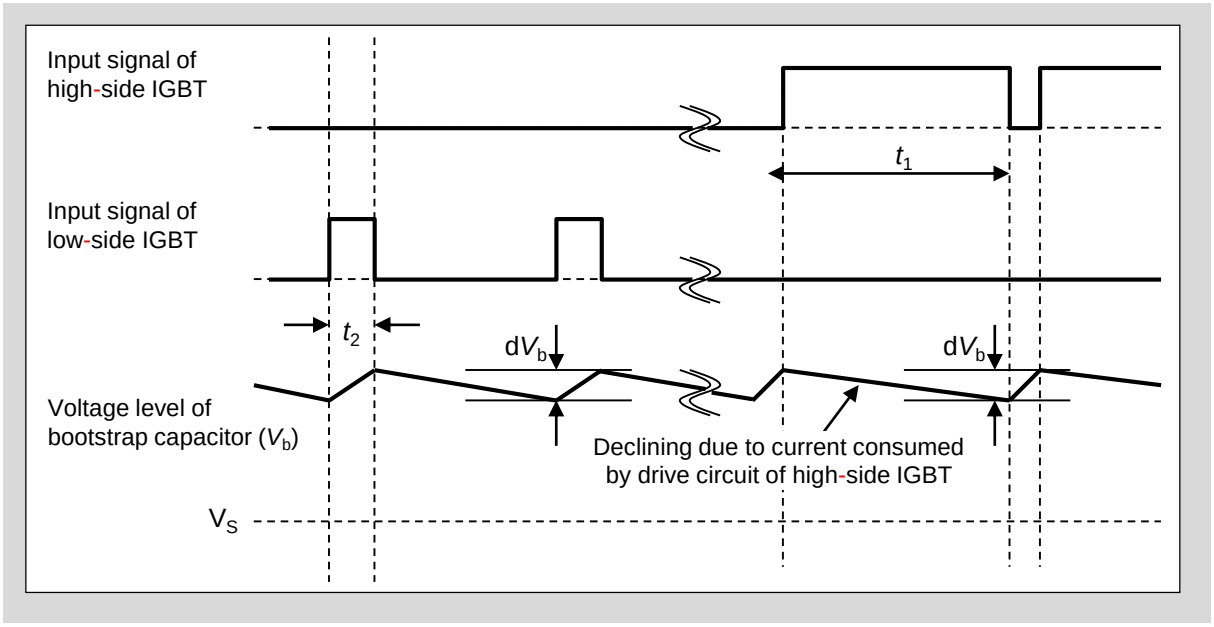


Fig.3-10 Timing chart of charging and discharging operation

<Setting the bootstrap capacitance for Initial charging>

- The initial charge of the bootstrap capacitor is required to start-up the inverter.
- The pulse width or pulse number should be large enough to make a full charge of the bootstrap capacitor.
- For reference, the charging time of 10μF capacitor through the internal bootstrap diode is about 2ms.

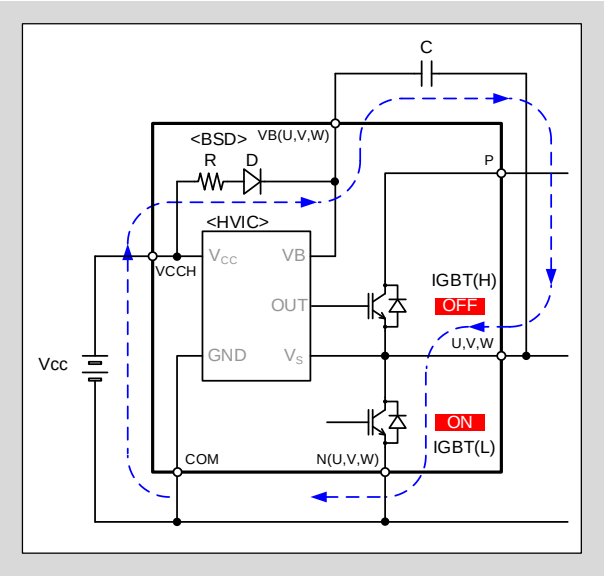


Fig.3-11 Circuit diagram of initial charging operation

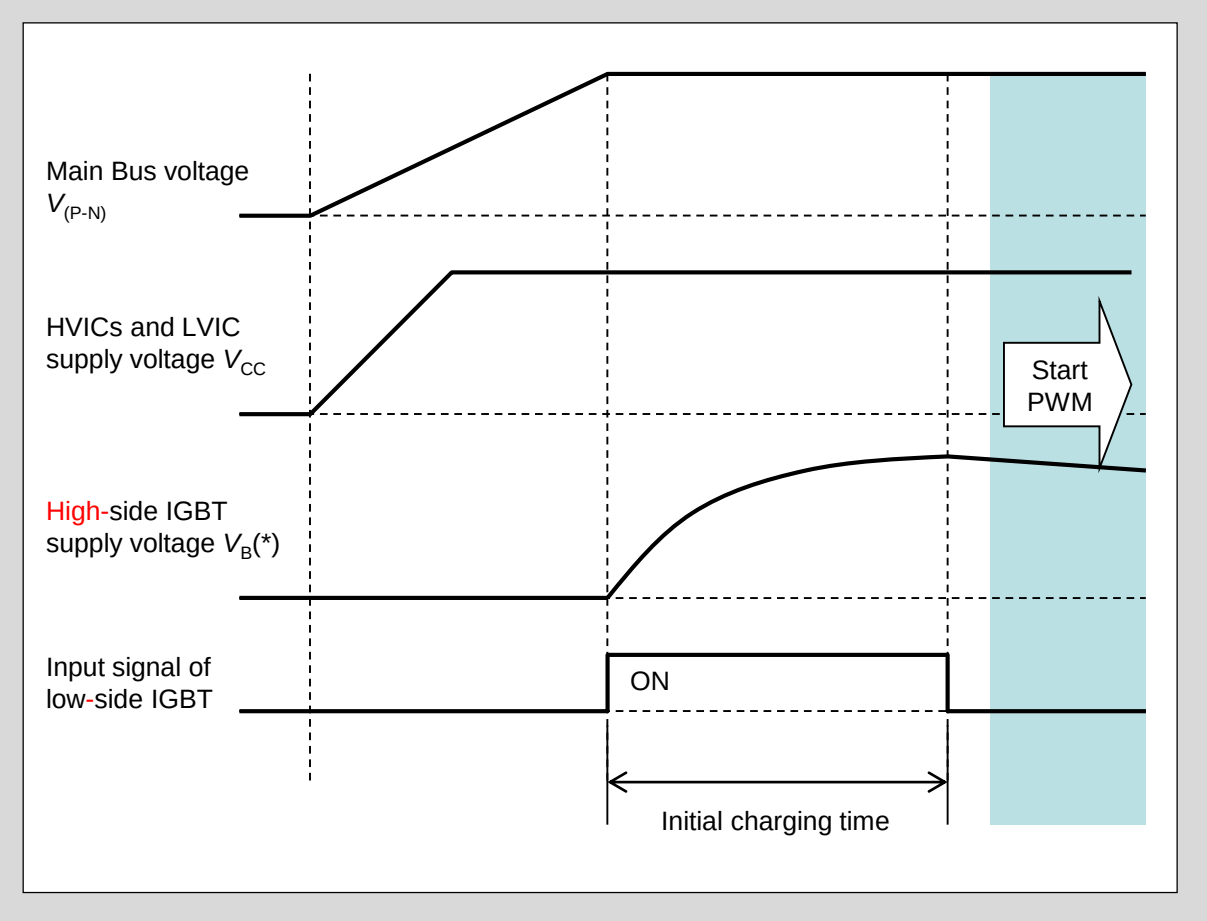


Fig.3-12 Timing chart of initial charging operation

<BSD built-in limiting resistance characteristic>

The BSD has non-linear V_F-I_F characteristic as shown in Fig. 3-13 because the diode forms a built-in current limiting resistor in the silicon. The equivalent dc-resistance against the charging voltage is shown in Fig.3-14.

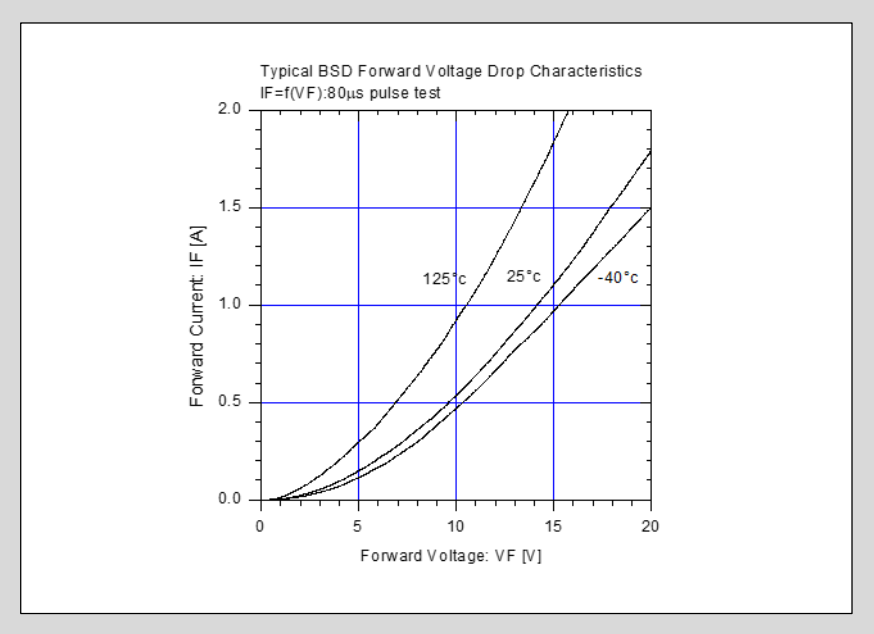


Fig.3-13 V_F-I_F curve of boot strap diode

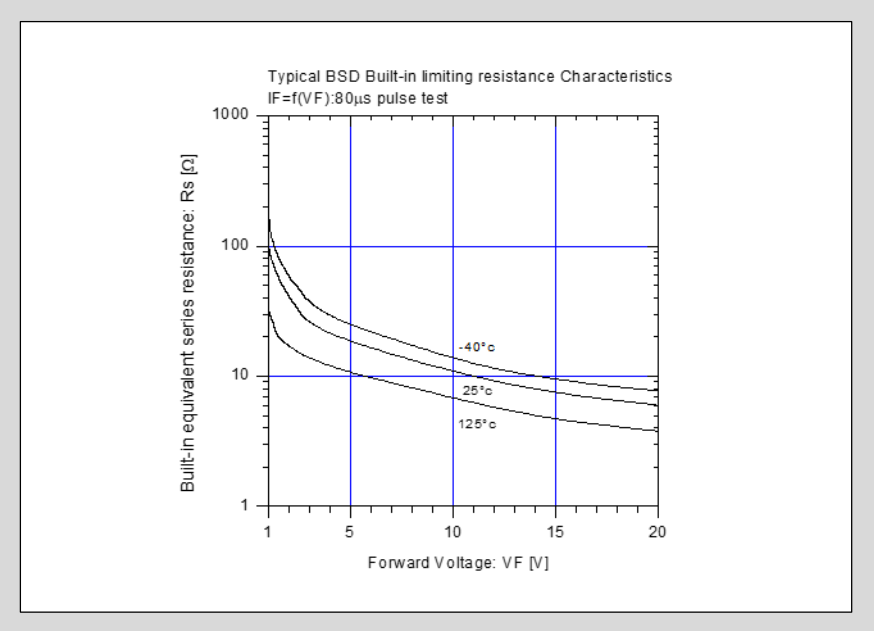


Fig.3-14 Equivalent series resistance of boot strap diode

4. Input Terminals IN(HU,HV,HW), IN(LU,LV,LW)

<Input terminals Connection>

- Fig.3-15 shows the input interface circuit between the MPU and the product. It is possible that the input terminals connect directly to the MPU. It should not need the external pull up and down resistors connected to the input terminals, input logic is active high and the pull down resistors are built in.
- The RC coupling at each input (parts shown dotted in Fig.3-15) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's PCB layout.

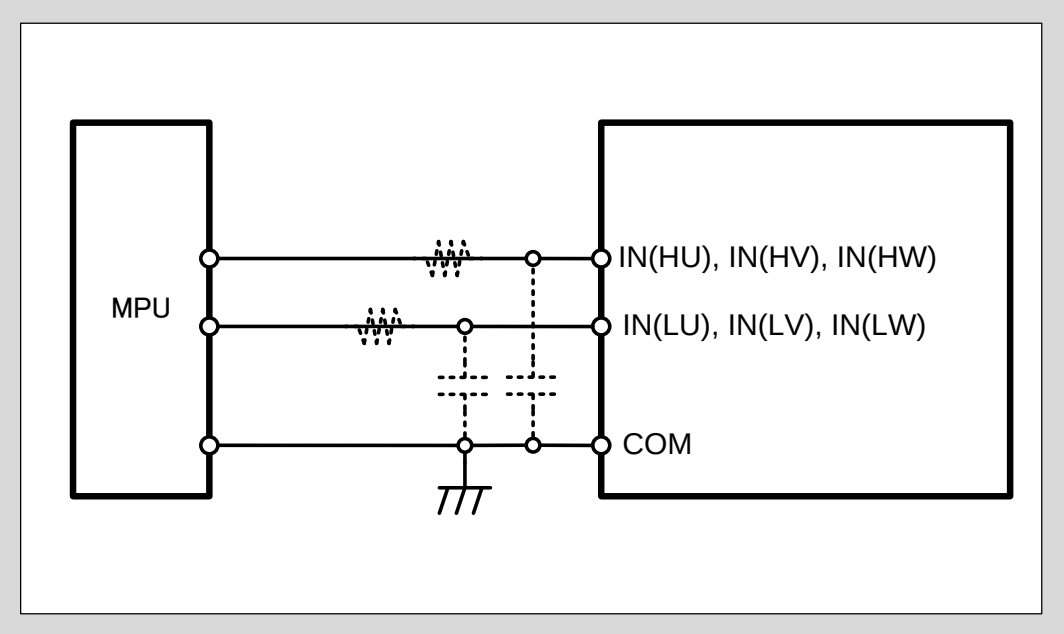


Fig.3-15 Recommended MPU I/O Interface Circuit of IN(HU,HV,HW), IN(LU,LV,LW) terminals

<Input terminal circuit>

- The input logic of this product is active high. This logic has removed the sequence restriction between the control power supply and the input signal during startup or shut down operation. Therefore it makes the system fail safe. In addition, pull-down resistors are built into each input terminals in Fig.3-16. Thus, external pull-down resistors are not needed and reduces the number of system components. Furthermore, by setting the input threshold voltage low,. a 3.3V-class MPU can be connected directly.
- As shown in Fig.3-16, the input circuit integrates a pull-down resistor. Therefore, when using an external filtering resistor between the MPU output and input of the product, please consider the signal voltage drop at the input terminals to satisfy the turn-on threshold voltage requirement. For instance, *R*=100Ω and *C*=1000pF for the parts shown dotted in Fig.3-15.
- Fig.3-16 shows that the internal diodes are connected to the VCCL-IN(LU, LV, LW) and IN(HU, HV, HW, LU, LV, LW)-COM terminals. Do not use these diodes for voltage clamp purpose otherwise the product might be damaged.

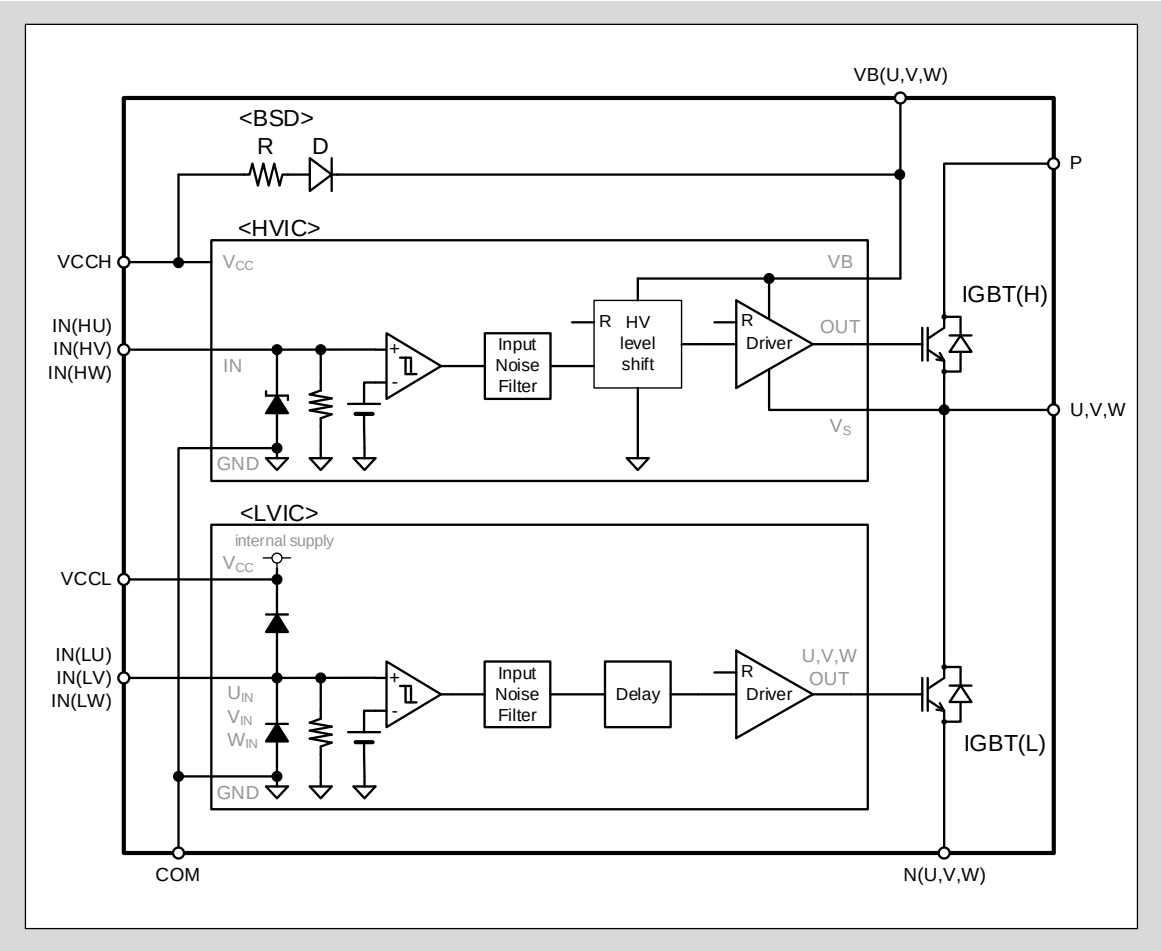


Fig.3-16 Input terminals IN(HU, HV, HW), IN(LU, LV, LW) circuit

<IGBT drive state versus Control signal pulse width>

$t_{IN(ON)}$ is a recommended minimum turn-on pulse width for changing the IGBT state from OFF to ON, and $t_{IN(OFF)}$ is a recommended minimum turn-off pulse width for changing the IGBT state from ON to OFF. Fig.3-17 and Fig.3-18 show IGBT drive state for various control signal pulse width.

A: IGBT may turn on occasionally, even when the ON pulse width of control signal is less than minimum tIN(ON). Also if the ON pulse width of control signal is less than minimum tIN(ON) and voltage below -5V is applied between U-COM,V-COM,W-COM , it may not turn off due to smalfunction of the control circuit.
B: IGBT can turn on and is saturated under normal condition.
C: IGBT may turn off occasionally, even when the OFF pulse width of control signal is less than minimum $t_{IN(OFF)}$. Also if the OFF pulse width of control signal is less than minimum $t_{IN(OFF)}$ and voltage below -5V is applied between U-COM, V-COM, W-COM , it may not turn on due to malfunction of the control circuit.
D: IGBT can turn fully off under normal condition.

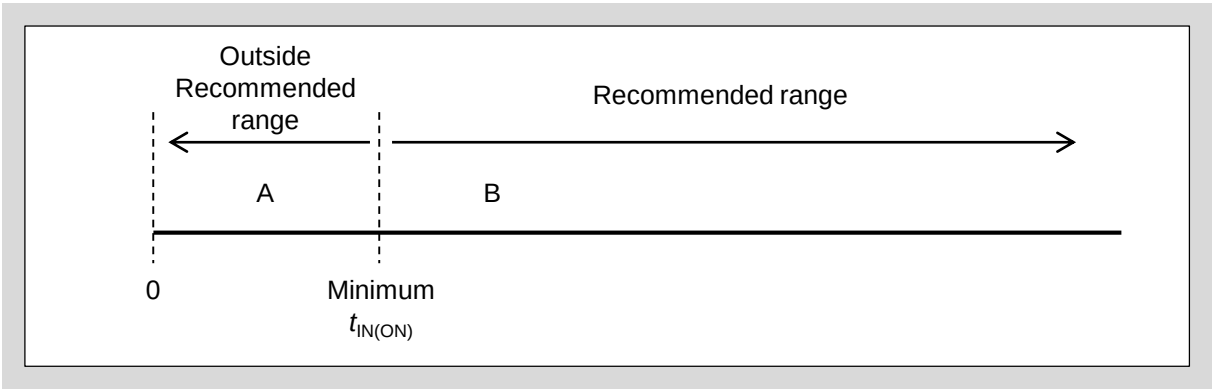


Fig.3-17 IGBT drive state versus ON pulse width of input signal

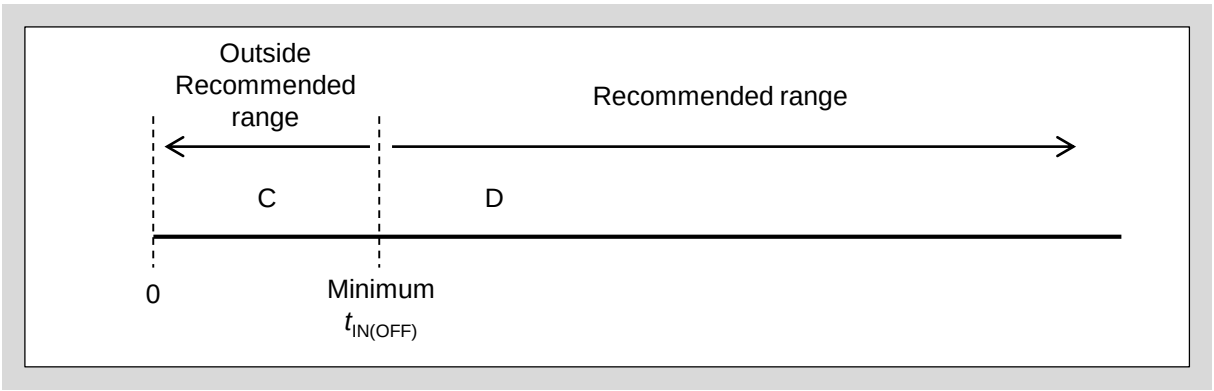


Fig.3-18 IGBT drive state versus OFF pulse width of input signal

5. Over Current Protection Input Terminal IS

- Over current (OC) protection function works by detecting the voltage generated by the external shunt resistor connected between N(U, V, W) and COM at the IS terminal, turn off the IGBTs and output an alarm signal.
- Fig.3-19 shows the over current sensing voltage input IS circuit block, and Fig.3-20 shows the OC operation sequence.
- To prevent the product from unnecessary operations due to normal switching noise or recovery current, it is necessary to apply an external R-C filter (time constant is approximately 1.5μs) to the IS terminal. The shunt resistor should be connected to the product as close as possible.
- Fig.3-19 shows that the diodes in the product are connected to the VCCL-IS and IS-COM terminals. Do not use these diodes for voltage clamp purpose otherwise the product might be damaged.

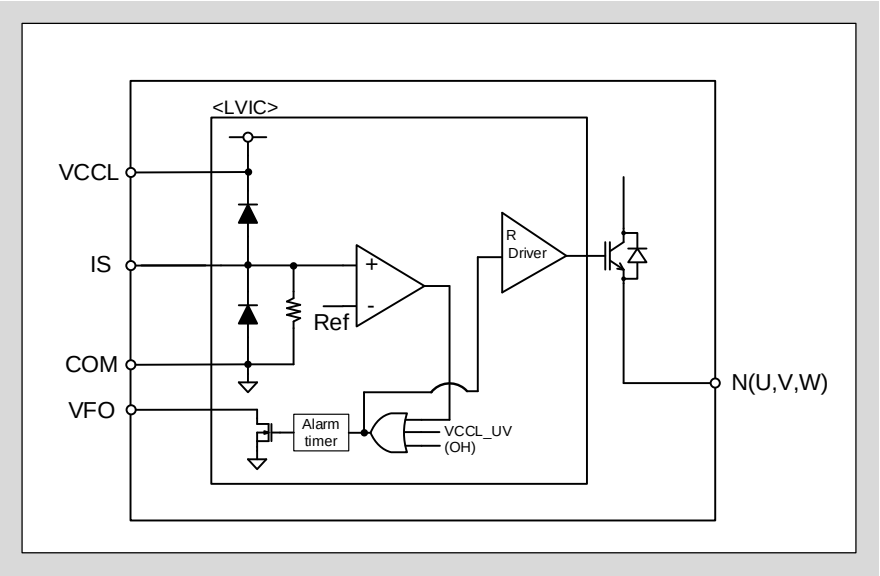


Fig.3-19 Over current sensing voltage input IS circuit

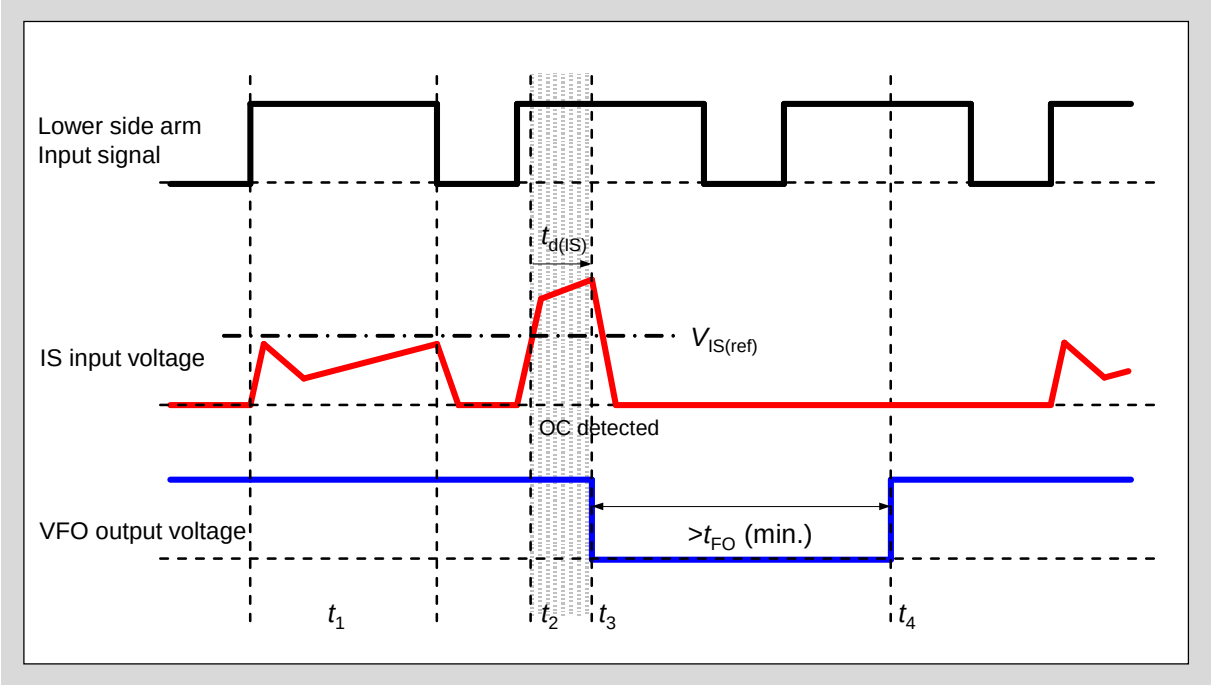


Fig.3-20 Operation sequence of Over Current protection

t1 : IS input voltage does not exceed $V_{IS(ref)}$, while the collector current of the lower side IGBT is under the normal operation.

t2 : When IS input voltage exceeds $V_{IS(ref)}$, the OC is detected.

t3 : The fault output V_{FO} is activated and all lower side IGBT shut down simultaneously after the over current protection delay time $t_{d(IS)}$. Inherently there is dead time of LVIC in $t_{d(IS)}$.

t4 : After the fault output pulse width t_{FO}, the OC is reset. Then next input signal is activated.

6. Fault Status Output Terminal VFO

- As shown in Fig.3-21, it is possible to connect the fault status output VFO terminal directly to the MPU. VFO terminal is open drain configured, thus this terminal should be pulled up by a resistor of approximate 10kΩ to the positive side of the 5V or 3.3V external logic power supply, which is the same as the input signals. It is also recommended that the by-pass capacitor C1 should be connected at the MPU, and the inrush current limitation resistance R1, which is more than 5kΩ, should be connected between the MPU and the VFO terminal. These signal lines should be wired as short as possible.
- Fault status output VFO function is activated by the UV of V_{CCL}, OC and OH. (OH protection function is applied to “6MBP**XSF060-50”.)
- Fig.3-21 shows that the diodes in the IPM are electrically connected to the VCCL-VFO and VCCL-COM terminals. Do not use these diodes for voltage clamp purpose otherwise the product might be damaged.
- Fig.3-22 shows the Voltage-current characteristics of VFO terminal at fault state condition. The I_{FO} is the sink current of the VFO terminal as shown in Fig.3-21.

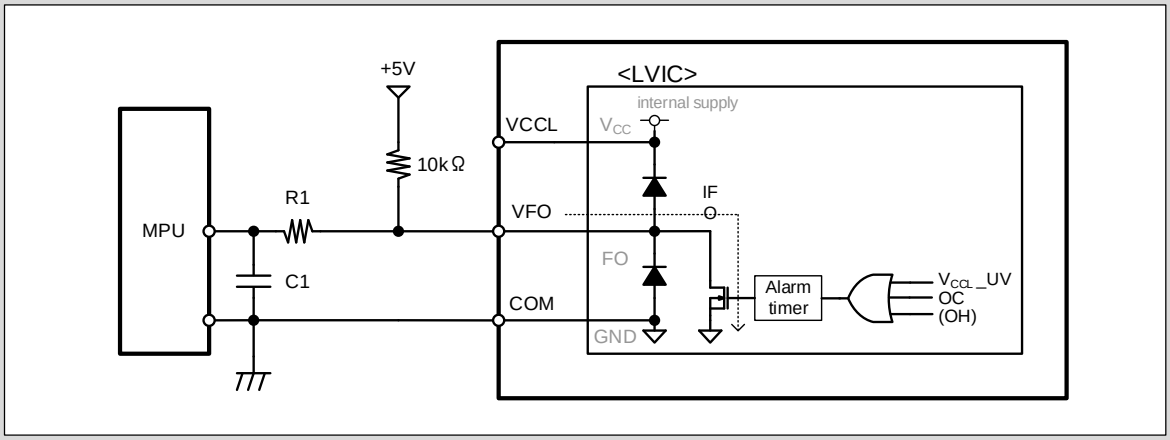


Fig.3-21 Recommended MPU I/O Interface Circuit of VFO terminal

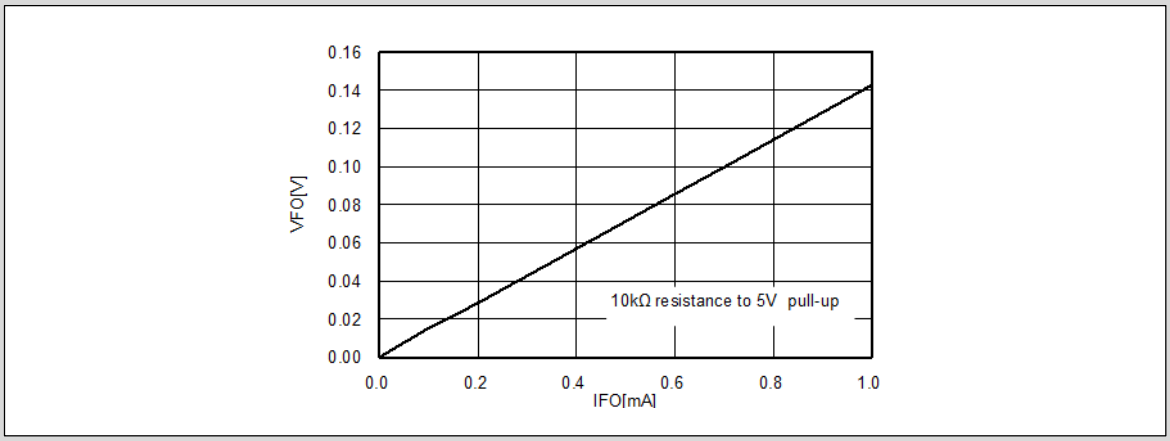


Fig.3-22 Voltage-current Characteristics of VFO terminal at the fault state condition

7. Temperature Sensor Output Terminal TEMP

- As shown in Fig. 3-23, the temperature sensor output TEMP can be connected to MPU directly.
- It is recommended that a by-pass capacitor C_{TEMP} and >10kΩ of inrush current limiting resistor R_{TEMP} are connected between the TEMP terminal and the MPU. These signal lines should be wired as short as possible to each device.
- The product has a built-in temperature sensor, and it can output an analog voltage according to the LVIC temperature. This function doesn't protect the product, and there is no fault signal output.
- "6MBP**XSF060-50" has built-in overheating protection. If the temperature exceeds T_{OH}, fault signal will output due to the overheating protection function.
- Since the position of the IGBT chip and the position of the temperature sensor are different, it is not possible to respond to sudden rise in Tvj such as during motor lock and short circuit (see Fig. 2-2).
- A diode is electrically connected between TEMP-COM terminal as shown in Fig. 3-12. The diode protect the product from input surge voltage. Do not use the diode for voltage clamp purpose otherwise the product might be damaged.
- Fig.3-24 shows the LVIC temperature versus TEMP output voltage characteristics. A Zener diode should be connected to the TEMP terminal when the power supply of MPU is 3.3V. Fig. 3-25 shows the LVIC temperature versus TEMP output voltage characteristics with 22kΩ pull-down resistor $R_{pulldown}$.
- Fig.3-26 shows the operation sequence of TEMP terminal at during the LVIC startup and shut down conditions.

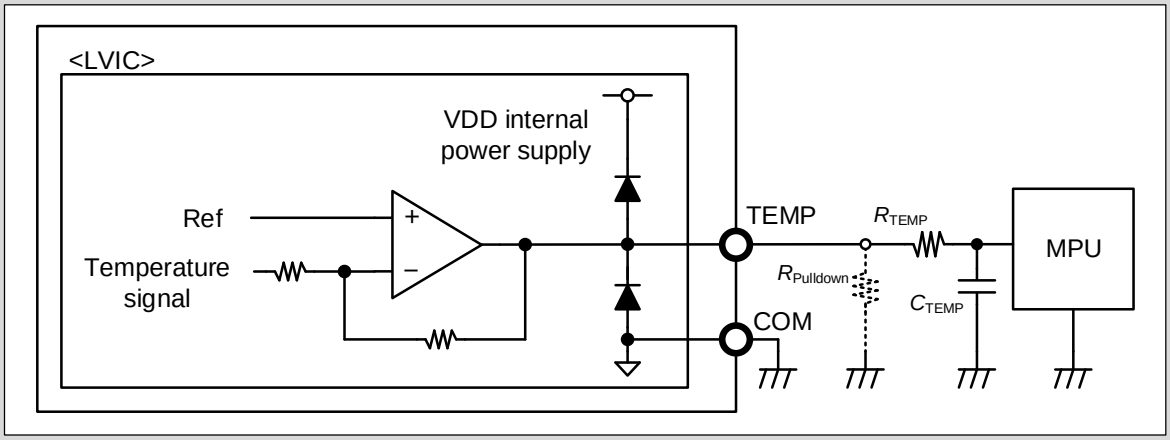


Fig.3-23 Recommended MPU I/O Interface Circuit of TEMP terminal

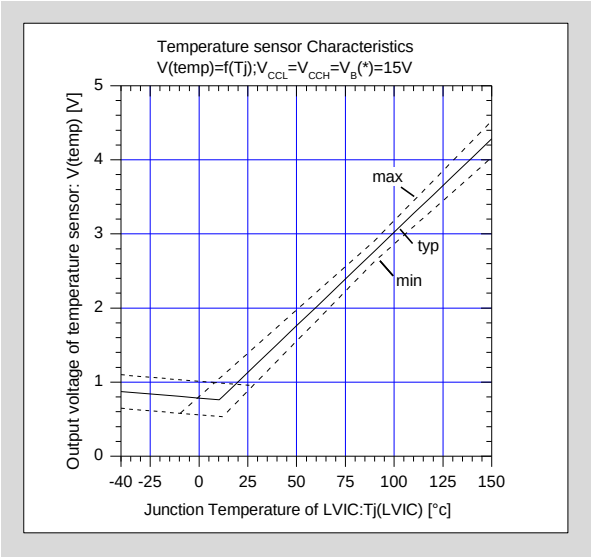


Fig.3-24 LVIC temperature vs. TEMP output voltage characteristics without pull-down resistor

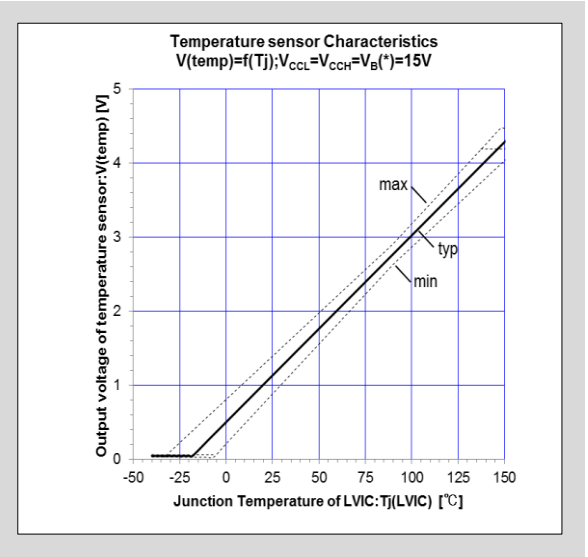


Fig.3-25 LVIC temperature vs. TEMP output voltage characteristics with 22kΩ pull-down resistor

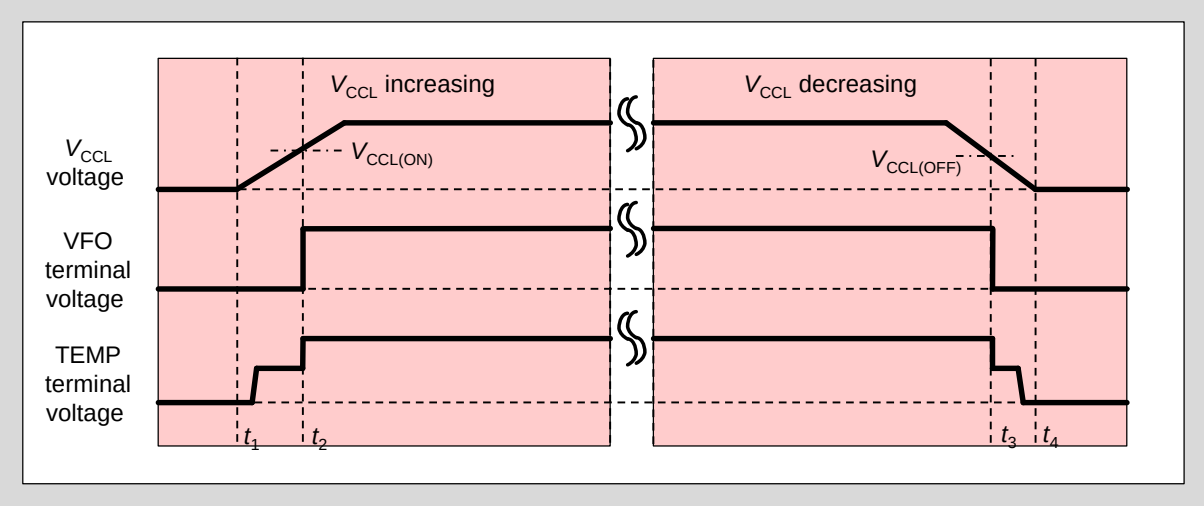


Fig.3-26 Operation sequence of TEMP terminal during LVIC startup and shut down conditions

t_1-t_2 : TEMP function is activated when V_{CCL} exceeds $V_{CCL(ON)}$. If V_{CCL} is lower than $V_{CCL(ON)}$, the TEMP terminal voltage is the same as the clamp voltage.

t_2-t_3 : TEMP terminal voltage rises to the voltage determined by LVIC temperature. In the case that the temperature is under clamping condition, the TEMP terminal voltage is the clamp voltage even though V_{CCL} is above $V_{CCL(ON)}$.

t_3-t_4 : TEMP function is reset when V_{CCL} falls below $V_{CCL(OFF)}$. TEMP terminal voltage is the same as the clamp voltage.

8. Over Heating Protection

- The over heating (OH) protection functions is integrated into "6MBP**XSF060-50".
- The OH function monitors the LVIC junction temperature. Since the position of the IGBT chip and the position of the temperature sensor are different, it is not possible to respond to sudden rise in Tvj such as during motor lock and short circuit (see Fig. 2-2).
- The T_{OH} sensor position is shown in Fig.2-2.
- As shown in Fig.3-27, the product shuts down all low side IGBTs when the LVIC temperature exceeds T_{OH}. The fault status is reset when the LVIC temperature drops below $T_{OH} - T_{OH(hys)}$.

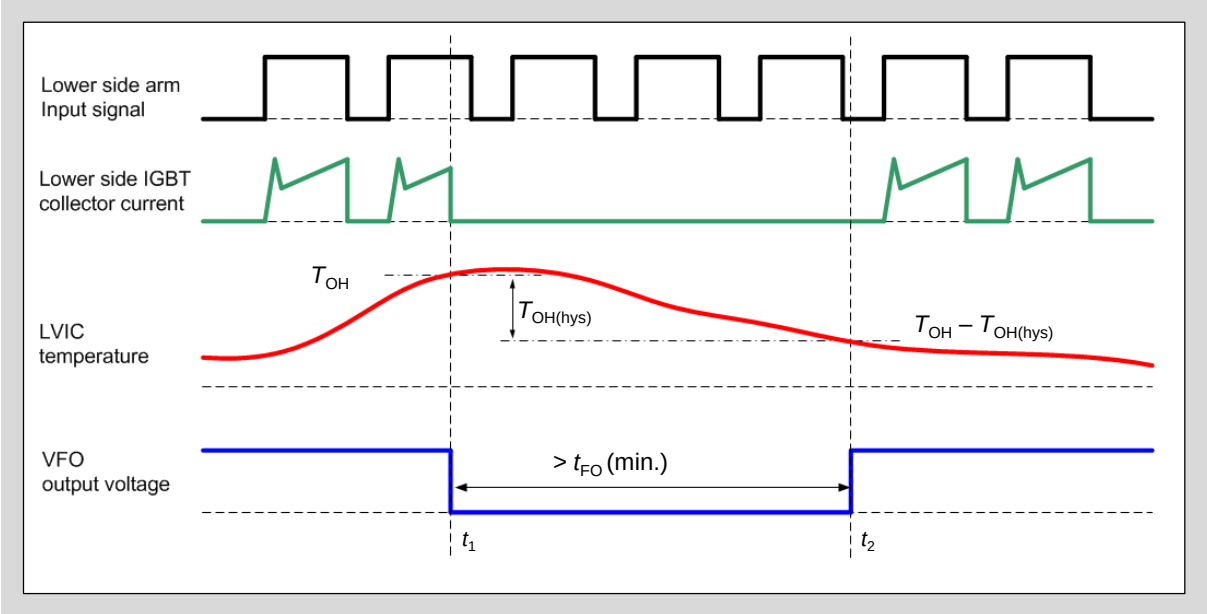


Fig.3-27 Operation sequence of the over heating operation

t_1 : The fault status is activated and all IGBTs of the lower side arm shut down, when LVIC temperature exceeds T_{OH}.

t_2 : When LVIC temperature falls below $T_{OH} - T_{OH(hys)}$, the fault status is reset after t_{FO} and next input signal is activated. $T_{OH(hys)}$ is the over heating protection hysteresis

Chapter 4 Power Terminals

In this chapter, the guideline and precautions in circuit design on the power terminals, such as how to determine the resistance of shunt resistor are explained.

1. Connection of Bus Input terminal and Low Side Emitters

<Description of the power terminals>

Table 4-1 shows the details about the power terminals.

Table 4-1 Detailed description of power terminals

Terminal Name	Description
P	Positive bus voltage input terminal It is internally connected to the collector of the high side IGBTs. In order to suppress the surge voltage caused by the wiring or PCB pattern inductance of the bus voltage, connect a snubber capacitor close to this pin. (Typically metal film capacitors are used)
U,V,W	Motor output terminal Inverter output terminals for connecting to motor load.
N(U),N(V),N(W)	Negative bus voltage input terminals These terminals are connected to the low side IGBT emitter of the each phase. In order to monitor the current on each phase, shunt resistors are connected between these terminals and the negative bus voltage input (power ground).

<Recommended wiring of shunt resistor and snubber capacitor>

- Connect external shunt resistors to detect over current (OC) condition and phase currents.
- Long wiring patterns between the shunt resistor and the product will cause excessive surge voltage that might damage the internal control IC and current detection components. To reduce the pattern inductance, the wiring between the shunt resistors and the product should be as short as possible.
- As shown in the Fig.4-1, snubber capacitors should be connected at the right location to suppress surge voltage effectively.
- Connecting the snubber capacitor at location "C" is recommended. If the snubber capacitor is connected at location "A" as shown in the Fig.4-1, the snubber capacitor cannot suppress the surge voltage effectively because the wiring inductance is not negligible. If the capacitor is connected at the location "B", the charging and discharging current of snubber capacitor will flow through the shunt resistor. This will impact the current detection signal and the OC protection level will be lower than the design value. Although the surge voltage suppression effect when the snubber capacitor is connected at location "B" is greater than that at location "A" or "C", location "C" is recommended considering the impact to the current detection accuracy.
- Snubber capacity of 0.1 ~ 0.22 μF is recommended.

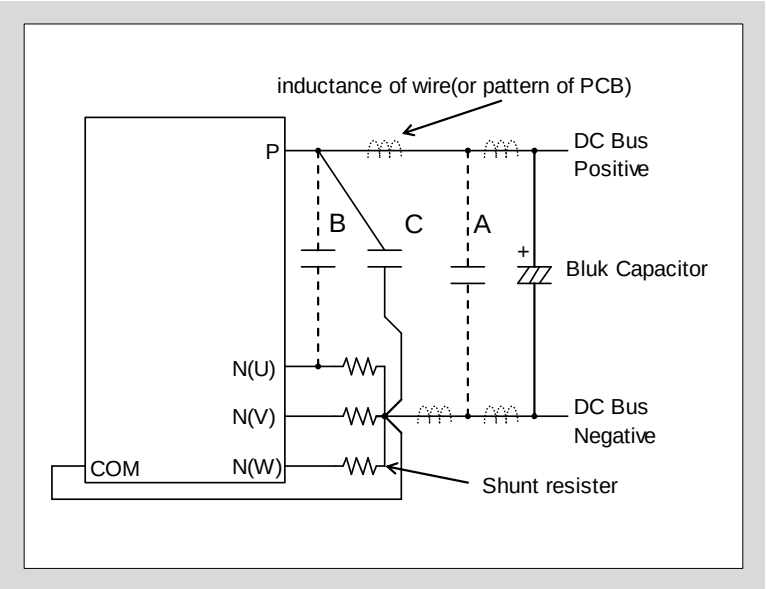


Fig.4-1 Recommended wiring of shunt resistor and snubber capacitor

2. Setting of Shunt Resistor for Over Current Protection

<Selecting current sensing shunt resistor>

The value of current sensing resistor is calculated by the following equation :

$$R_{\mathrm{Sh}} = \frac{V_{\mathrm{IS(ref)}}}{I_{\mathrm{OC}}} \qquad (4.1)$$

- Where $V_{\mathrm{IS(ref)}}$ is the over current (OC) protection reference voltage level of the product and I_{OC} is the current of OC detection level. $V_{\mathrm{IS(ref)}}$ is 0.455V(min.), 0.48V(typ.) and 0.505V(max.). And R_{Sh} is the Resistance of the shunt resistor.
- The maximum value of OC level should be set lower than the repetitive peak collector current in the specification datasheet of this product, taking into consideration the variation in shunt resistance.
- For example, if OC level is set at 45A, the recommended value of the shunt resistor is calculated as:

$$R_{\mathrm{Sh(min)}} = \frac{V_{\mathrm{IS(ref)(max)}}}{I_{\mathrm{OC}}} = \frac{0.505}{45} = 11.2[\mathrm{m\Omega}] \qquad (4.2)$$

- Where $R_{\mathrm{Sh(min)}}$ is the minimum resistance of the shunt resistor. It should be noted that a proper resistance should be chosen considering OC level required in practical application.

<Filter delay time setting of over current protection>

- An external RC filter is necessary in the over current sensing circuit to prevent unnecessary over current protection caused by noise. The RC time constant is determined by the applying time of noise and the short circuit withstand capability of IGBTs. It is recommended to be set approximately 1.5μs.
- When the voltage across the shunt resistor exceeds the OC level, the filter delay time t_{delay} that delays the rises of input voltage of IS terminal to the OC level is caused by the RC filter delay time constant and is given by:

$$t_{\mathrm{delay}} = -\tau \cdot \ln\left(1 - \frac{V_{\mathrm{IS(ref)(max)}}}{R_{\mathrm{Sh}} \cdot I_{\mathrm{p}}}\right) \quad (4.3)$$

- Where τ is the RC time constant, I_P is the peak current flowing through the shunt resistor. In addition, there is a shut down propagation delay $t_{d(IS)}$ of OC.
- Therefore, the total time t_{total} from OC triggered to shut down of the IGBT is given by:

$$t_{\mathrm{total}} = t_{\mathrm{delay}} + t_{\mathrm{d(IS)}} \quad (4.4)$$

- The total delay time t_{total} should be shorter than the short circuit withstands capability of IGBT. Please confirm the proper delay time in actual equipment.

Chapter 5 Recommended wiring and layout

In this chapter, recommended wiring and layout are explained. In this section, tips and precautions in PCB design are described with example of application circuit.

1. Examples of Application Circuits

Fig. 5-1 and Fig.5-2 show examples of application circuits and their notes. In these figures, although two types of current detection method are shown, the notes are common.

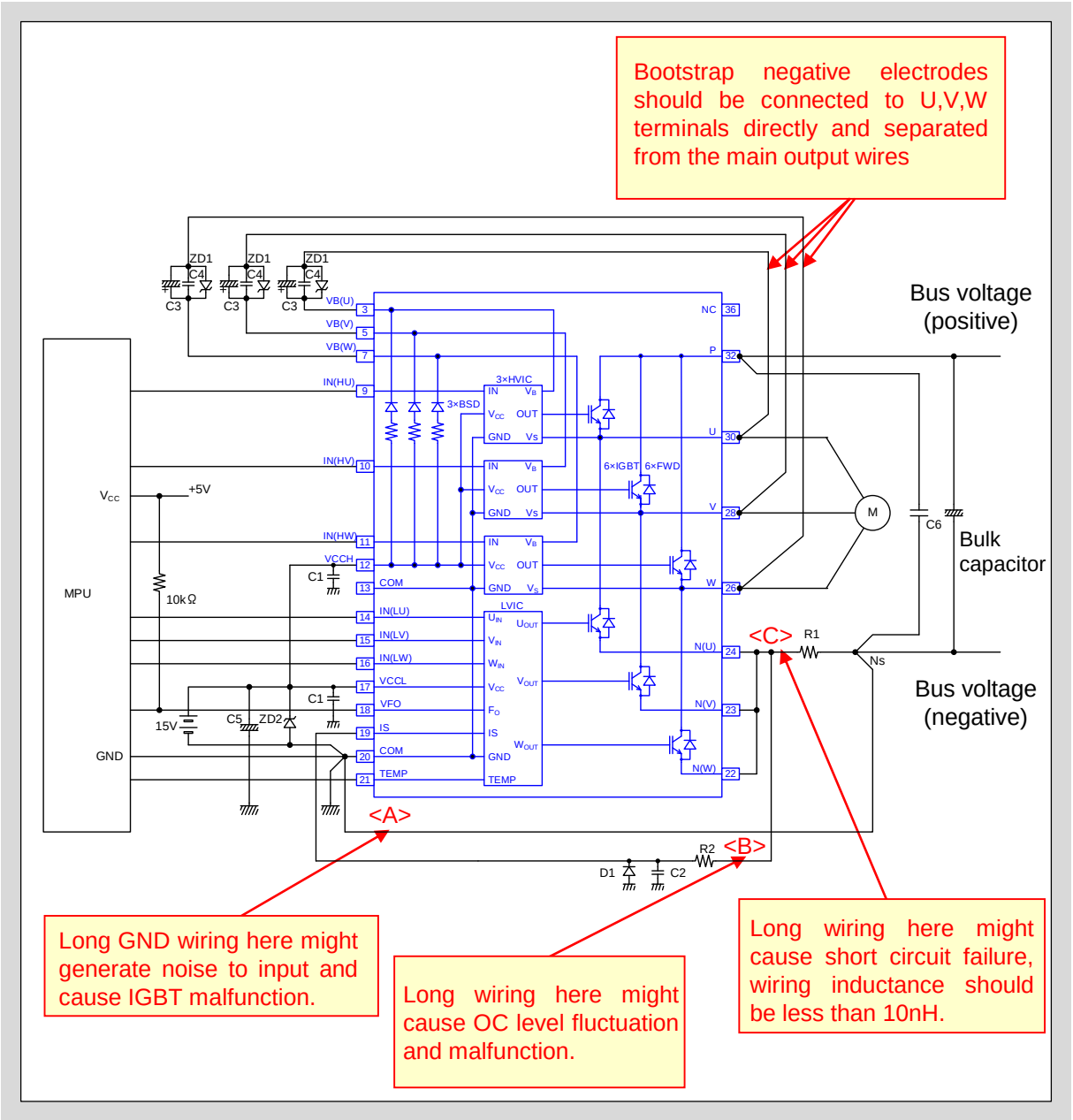


Fig. 5-1 Example of application circuit 1
(In case of sensing all 3 phase currents at once with a single shunt resistor)

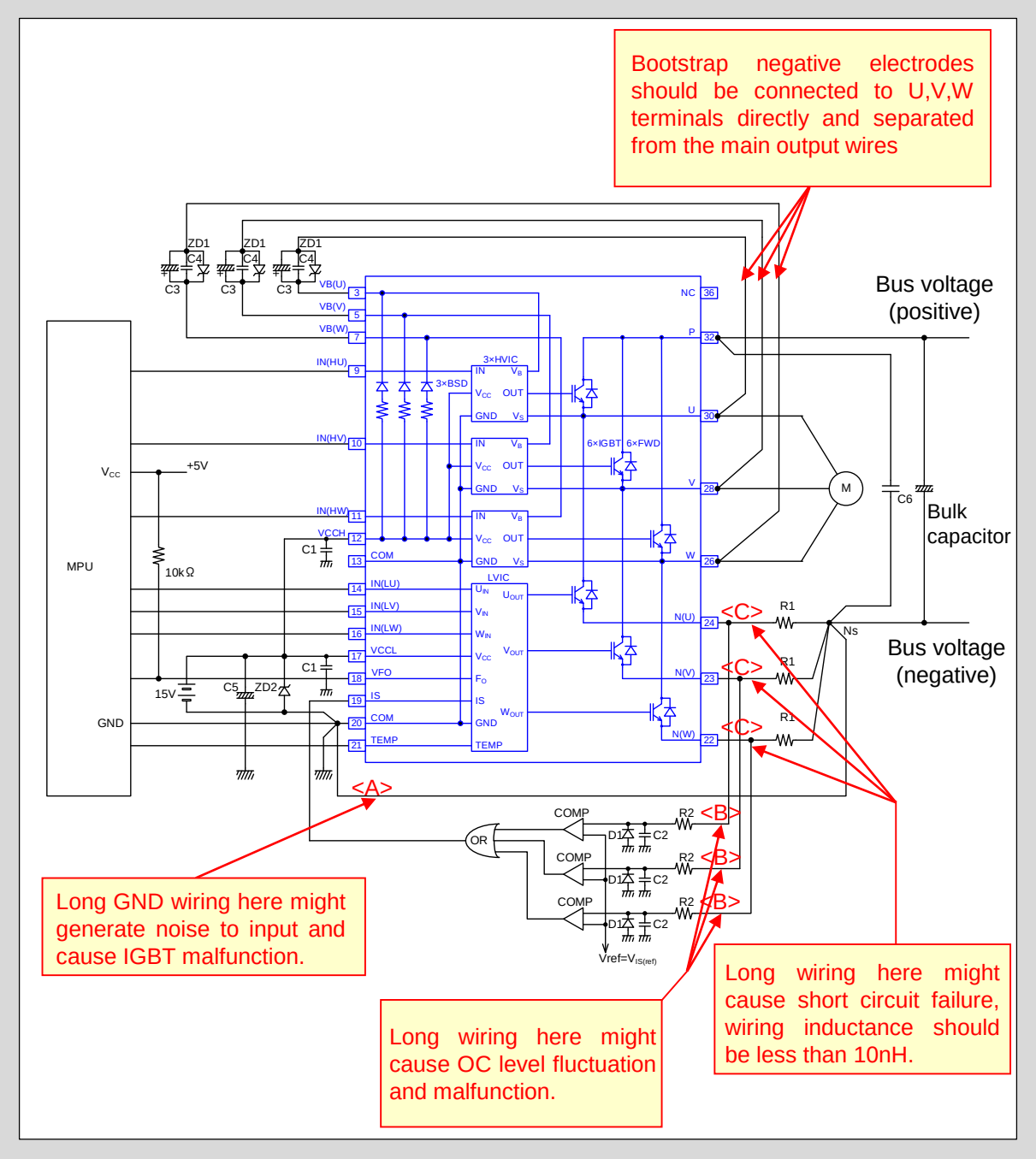


Fig. 5-2 Example of application circuit 2
(In case of sensing each phase current individually)

<Note>

1. Input signal for IGBT driving is High-Active. The input circuit of the IC has a built-in pull-down resistor. To prevent malfunction, the wiring of each input should be as short as possible. When using RC filter, please make sure that the input signal level meets the turn-on and turn-off threshold voltage.
2. The product has built-in HVICs and thus it is possible to be connected to MPU directly without any photocoupler or pulse transformer.
3. VFO output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10kW.
4. To prevent erroneous protection, the wiring of (A), (B), (C) should be as short as possible.
5. The time constant R2-C2 of the protection circuit should be selected approximately 1.5μs. Over current (OC) shut down time might vary due to the wiring pattern. Tight tolerance, temp-compensated type is recommended for R2, C2.
6. It is recommended to set the threshold voltage of the comparator reference input to be same level as the product OC trip reference voltage VIS(ref).
7. Please use high speed type comparator and logic IC to detect OC condition quickly.
8. If negative voltage is applied to R1 during switching operation, connecting a Schottky barrier diode D1 is recommended.
9. All capacitors should be connected as close to the terminals of the product as possible. (C1, C4: ceramic capacitors with excellent temperature, frequency and DC bias characteristics are recommended; C3, C5: select an electrolytic capacitor considering the ripple current capability and lifetime.)
10. To prevent destruction caused by surge voltage, the wiring between the snubber capacitor C6 and P terminal, Ns node should be as short as possible. Generally, snubber capacity of 0.1μF~0.22μF is recommended.
11. Two COM terminals (9 & 16 pin) are connected internally. Please connect either of the terminal to the signal GND and leave the other terminal open.
12. It is recommended to connect a Zener diode (22V) between each pair of control power supply terminals to prevent destruction caused by surge voltage.
13. If signal GND is connected to power GND by board pattern, there is possibility of malfunction due to fluctuations at the power GND. It is recommended to connect signal GND and power GND at a single point.

2. Recommendations and Precautions in PCB design

In this section, the recommended pattern layout and precautions in PCB design are described.
Fig.5-3 to Fig.5-7 show the images of recommended PCB layout (referring to example application circuit in Fig.5-1 and Fig.5-2).
In these figures, the input signals from system control are represented with "IN(HU)".

The recommendations and precautions are as follows,

<Overall design around Small IPM>

- Keep a relevant creepage distance at the boundary. (Place a slit between there if needed.)
- The pattern of the power input (DC bus voltage) part and the power supply for high side drive parts should be separated in order to prevent the increase of conduction noise. In case of crossing these wirings on pattern in multi-layer PCB, please take note of stray capacitance between wires and insulation performance of the PCB.
- The pattern of the power supply for high side drive part and the input circuit of each phase part should be separated to avoid malfunction of the system. In case of using multi-layer PCB, it is strongly recommended not to cross these wirings.

Details of each part are described in next page.

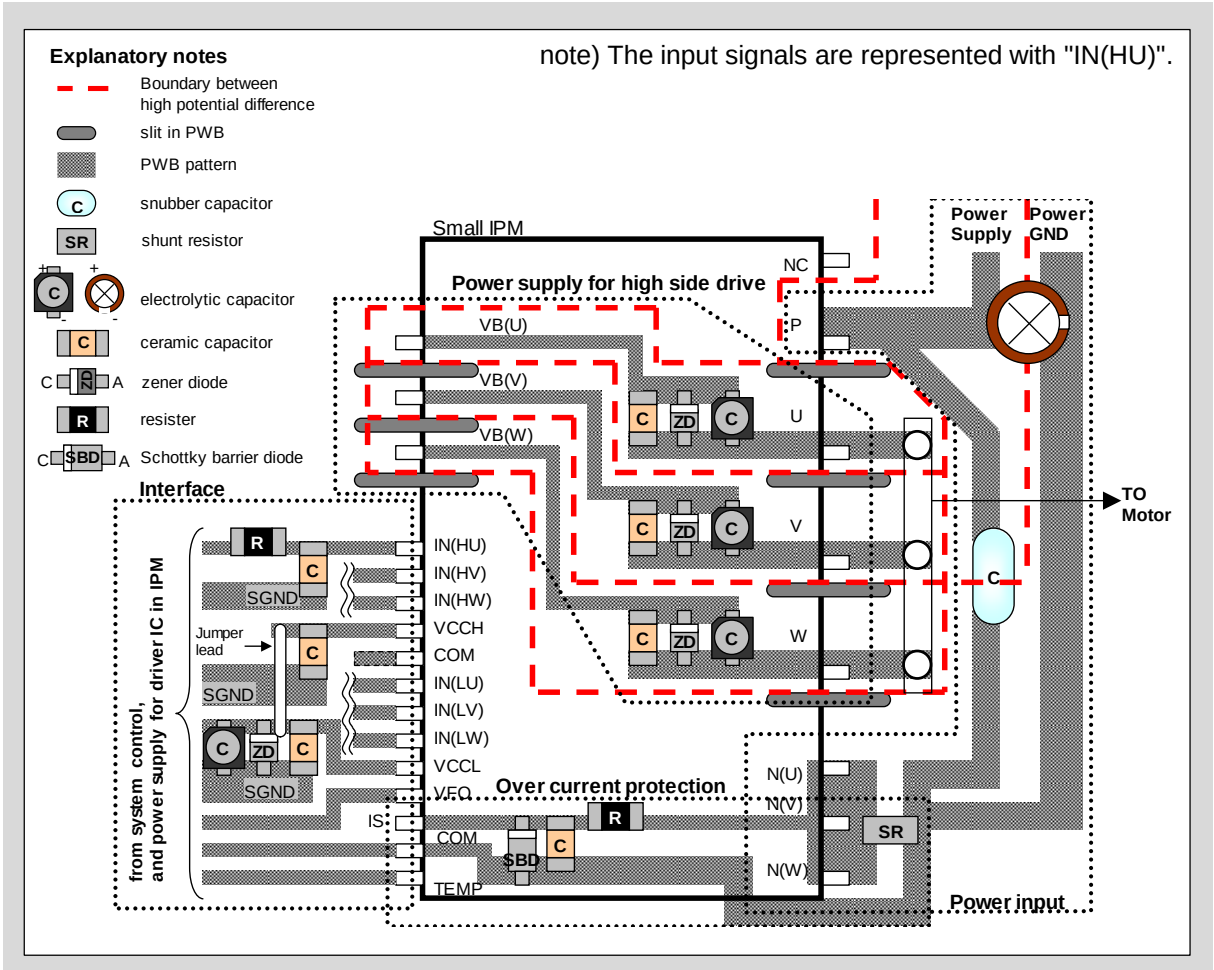


Fig.5-3 Image of recommended PCB layout (Overall design around the Small IPM)

<Power input part>

(A) Connect the snubber capacitor between P terminal and the negative node of the shunt resistor as close as possible. The pattern between the snubber capacitor and P terminal, and shunt resistor should be as short as possible to avoid the influence of pattern inductance.

(B) Pattern of the bulk capacitor and snubber capacitor should be separated near the P terminal and shunt resistor.

(C) The pattern from power GND and COM terminal should be connected as close as possible to the shunt resistor with single-point-grounding.

(D) Please use low inductance shunt resistor.

(E) The pattern between N(U),N(V),N(W) terminals and the shunt resistor should be as short as possible.

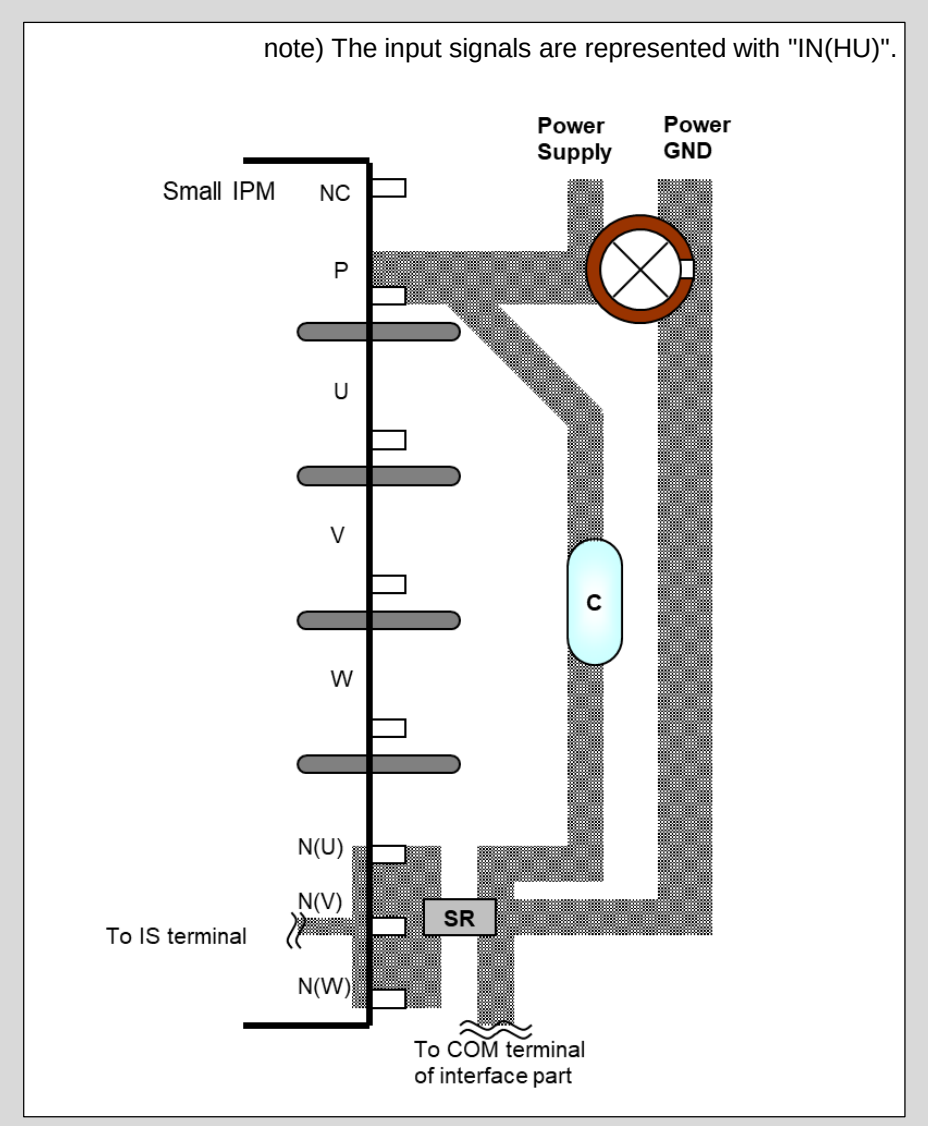


Fig.5-4 Image of recommended PCB layout(Power input part)

<Power supply for high side drive part>

A) The pattern between VB(U), VB(V), VB(W) and the electronic components (ceramic capacitor, electrolytic capacitor and Zener diode) should be as short as possible to avoid the influence of pattern inductance.

B) Please use appropriate capacitor according to applications. Especially, please use ceramic capacitor or low-ESR capacitor close to VB(U), VB(V), VB(W) terminals.

C) The pattern to Motor output and negative pole of the capacitor connected to VB(U), VB(V), VB(W) should be separated close to U,V and W terminals in order to avoid malfunction due to common impedance.

D) If the stray capacitance between VB(U) and power GND (or equal potential) is large, the voltage between VB(U) and U terminals might become overvoltage or negative voltage when IGBT turns on and off with high dV/dt. Therefore, connecting a Zener diode between VB(U) and U are recommended. It should be connected close to VB(U) terminal.
(The same applies to VB(V) and VB(W).)

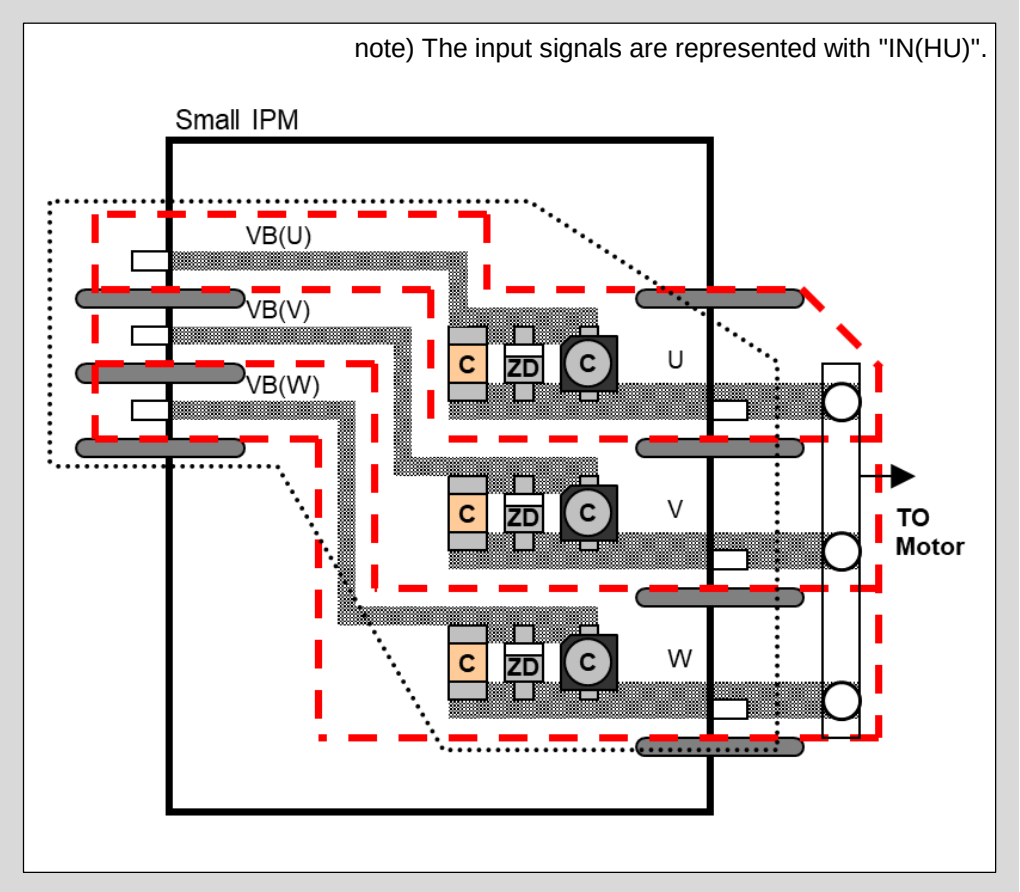


Fig.5-5 Image of recommended PCB layout(Power supply for high side drive part)

<Interface part>

(A) Please connect a capacitor between the input signal and COM terminal if the influence of noise from the power supply for high side drive part (and so forth) are not negligible. The negative pole of the capacitor should be connected as close as possible to the pattern of signal GND near the COM terminal. If filter resistor or capacitor is used, please take into account the internal pull down resistors in this IPM and confirm the signal level in the actual system.

(B) This product has two COM terminals that are connected internally. Please use either one.

(C) Electrolytic capacitor and ceramic capacitor should be connected between VCCL and COM, VCCH and COM. These capacitors should be connected as close to each terminal as possible.

(D) The output signal from TEMP terminal should be parallel with Signal GND in order to minimize the effects of noise.

(E) The pattern of Signal GND from system control and the pattern from COM terminal should be connected at single point ground. The single point ground should be as close to the COM terminal as possible.

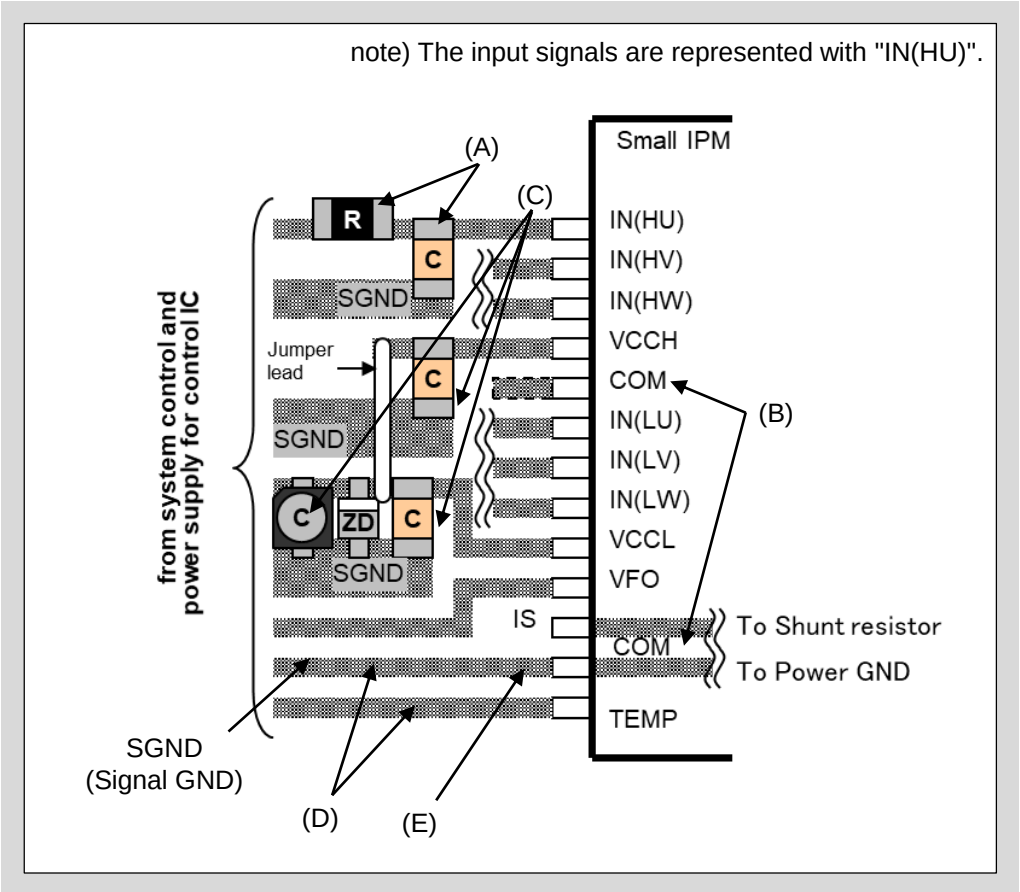


Fig.5-6 Image of recommended PCB layout
(Interface part)

<Over Current Protection part>

There are two methods to detect overcurrent (OC). Fig.5-7(a) shows the 'one-shunt type', and Fig.5-7(b) shows the '3-shunt type'.

Fig.5-7 (a)

(A) The pattern between the negative pole of the shunt resistor and the COM terminal is very important. It is not only the reference zero level of the control IC, but also the current path of bootstrap capacitor charging current and gate driving current of low side IGBTs.Therefore, in order to minimize the impact of common impedance, this pattern should be as short as possible.

(B) The pattern of IS signal should be as short as possible to avoid OC level fluctuation and malfunction.

(C) In order to prevent false detection during switching operation, it is recommended to connect a RC filter to the IS terminal. The negative pole of this capacitor should be connected to the pattern of signal GND near the COM terminal.

(D) If negative voltage is applied to IS terminal during switching operation, please connect a Schottky barrier diode between the IS and COM terminals or in parallel with the shunt resistor .

Fig.5-7 (b)

(A) Please use high speed type comparator and logic IC to detect OC condition quickly.

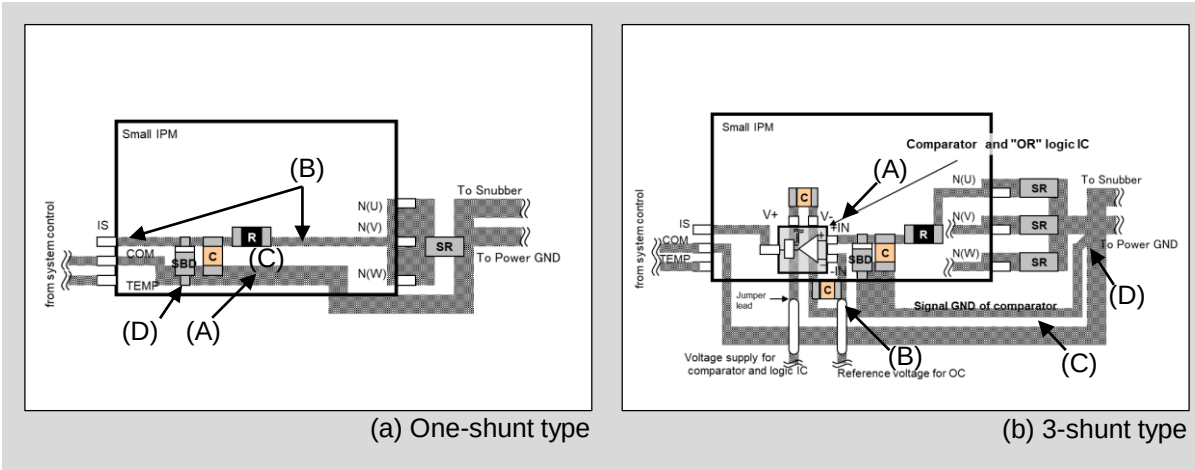
(B) The reference voltage level of OC which is inputted to the comparator should be coupled by a capacitor to signal GND. The capacitor should be as close to the comparator as possible.

(C) The pattern of signal GND for COM terminal and the pattern of signal GND for the comparator should be separated.

(D) The pattern of signal GND from COM and the pattern of signal GND of the comparator should be connected at single point ground. The single point ground should be as close to the shunt resistors as possible.

(E) The other precautions and recommendations are same as Fig.5-7 (a).

Please refer to Chapter 4, Section 2 for more information on determining the circuit constant.



(a) One-shunt type (b) 3-shunt type

Fig.5-7 Image of recommended PCB layout (Over Current Protection part)

note) The input signals are represented with "IN(HU)".

Chapter 6 Mounting Guideline and Thermal Design

1. Soldering to PCB

- The product's temperature during soldering might exceed the maximum storage temperature. To prevent damage to the product and to ensure reliability, please use the following soldering temperature.

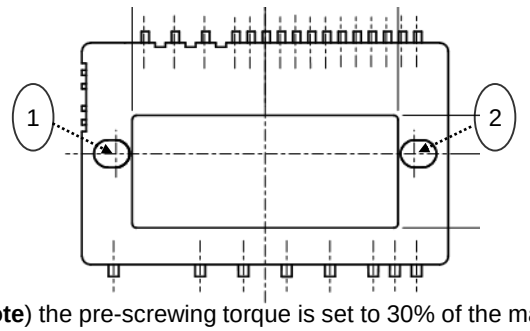
Table 6.1 Soldering temperature and duration

Methods	Soldering Temp. & Time
Dip soldering	260±5°C, 10±1sec

- A stopper is provided on the terminal to prevent the immersion depth of the terminal from coming too close to the product body. Use this stopper to secure the required distance from the printed circuit board and prevent the product body from being immersed in the solder bath during flow soldering.
- It is not recommended to reuse the product after it is removed from the printed circuit board because there is a possibility that the removed product was subjected to thermal or mechanical damage during the removal process.

2. Mounting to Heat Sink

- When mounting the product to a heat sink, please refer to the following recommended fastening order. Uneven fastening due to excessive torque might lead to destruction or degradation of the chip.



Note) the pre-screwing torque is set to 30% of the maximum torque rating.

Fig.6-1 Recommended screw fastening procedure

- Fig.6-2 shows the measurement position of heat sink flatness.
- The heat sink flatness should be 0μm/100mm to +100μm/100mm, and the surface roughness (Rz) should be less than 10μm.
- If the heat sink surface is concave, a gap occurs between the heat sink and the product, leading to deterioration of cooling efficiency.
- If the flatness is +100μm/100 mm or more, the aluminum base of the product is deformed and cracks could occur in the internal isolating substrates.

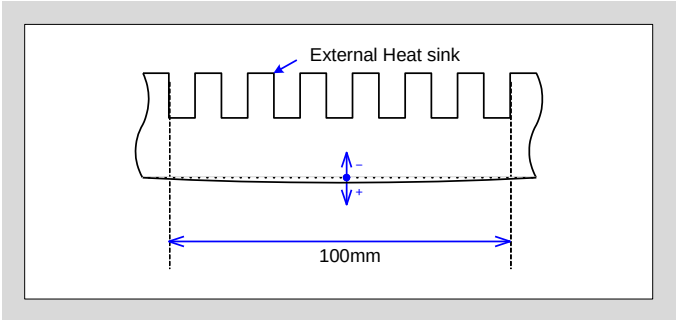


Fig.6-2 The measurement point of heat sink flatness

In order to achieve good heat dissipation, thermal grease with high thermal conductivity should be applied evenly to the contact surface between the product and the heat sink. The stencil mask method (Fig. 6-3) is recommended to control the appropriate thermal grease thickness. Please refer to mounting instruction for the recommended characteristics, amount, stencil mask pattern, etc. of thermal grease.

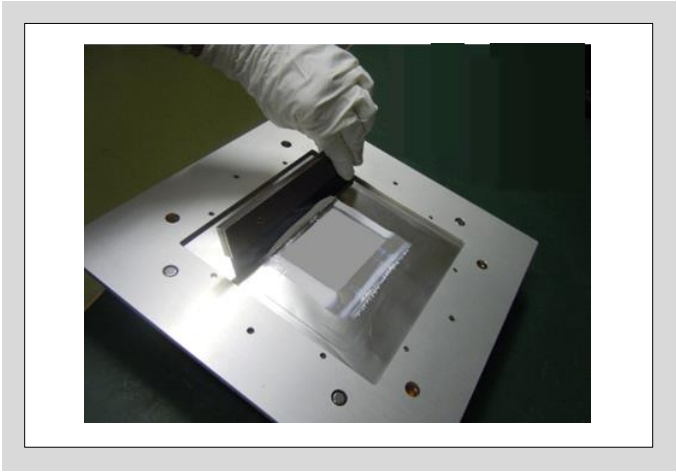


Fig. 6-3 Thermal grease application

3. Heat Sink Selection

- Please make sure that the junction temperature T_{vj} should not exceed the maximum junction temperature rating for safe operation. Heat sink should be designed to ensures that T_{vj} is always below the maximum junction temperature rating even during abnormal conditions such as overload operation as well as during rated load.
- Operating the IGBT above the maximum junction temperature rating can cause damage to the chips. The over heating (OH) protection function works when the IGBT junction temperature exceeds the maximum junction temperature rating. However, if the temperature rises too quickly, the OH protection might not work.
- Please note that the junction temperature of FWD should not exceed the maximum junction temperature rating too.
- When selecting a heat sink, please verify the chip temperature by measuring at the position shown in Fig.2-2.

For more detail about thermal design, please refer to Chapter 6 Section 2 of this note and “IGBT MODULE APPLICATION MANUAL (REH984e)”

Contents:

- Power dissipation loss calculation
- Selecting heat sinks
- Heat sink mounting precautions
- Troubleshooting

Chapter 7 Cautions

1. Precautions for use

- This product should be used within the absolute maximum rating (voltage, current, temperature, etc.). This product may be broken if used beyond the rating.
- Do not design and use the product in excess of the absolute maximum ratings (voltage, current and temperature). The product might be damaged if it is used in excess of the absolute maximum ratings.
- The equipment containing this product should have adequate fuses or circuit breakers to prevent the equipment from causing secondary destruction (ex. fire, explosion etc.).
- Please confirm the turn-off current and voltage are within the RBSOA.
- Consider the possible temperature rise not only for the junction and case, but also the terminals. Please confirm these temperatures are within the absolute maximum ratings.
- The product is made of incombustible material. However, if the product fails, it may emit smoke or flame. The product may become hot during operation, therefore when operating the product near flammable places or materials. please take measures to prevent the spread of fire.
- Do not touch the terminals or package of the product directly while power is supplied or during operation in order to avoid electric shock and burns.

- To prevent high-frequency noise such as switching noise from being directly applied to VCCH and VCCL terminals, connect a ceramic capacitor of appropriate capacity near to VCCH terminal between VCCH and ground terminals, and near to VCCL terminal between VCCL and ground terminals.
- The product might malfunction if noise is applied to the control terminals. Please use the product after checking that unstable operation or malfunction due to noise does not occur.
- The high side IGBTs might turn off if VB voltage drops below $V_{B(off)}$ due to noise, etc. Please connect ceramic capacitors of appropriate capacity between VB(U) - U terminals, VB(V) - V terminals, and VB(W) - W terminals respectively. The input signal voltage should be higher than the threshold voltage.

- Use this product within the reliability and lifetime under certain environments or conditions. The product may fail before the target lifetime of your system if used beyond the reliable lifetime of the product.
- The lifetime of the semiconductor products is not permanent. Please consider the thermal fatigue caused by temperature cycle due to self-generated heat. Please use the product within the ΔT_{vj} power cycle lifetime and ΔT_c power cycle lifetime.
- The ΔT_c power cycle depends on the case temperature (T_c) rise and fall, and T_c is affected by the cooling conditions of the system. Please consider the heat generation of the product and design the cooling condition to achieve target lifetime.
- The product should not used in an environment in the presence of acid, organic matter, or corrosive gas (hydrogen sulfide, sulfurous acid gas etc.)
- The product is not designed to be radiation-proof. Please avoid using it in an environment where it is exposed to radiation.
- It is recommended that any handling of the IPM is done on grounded electrically conductive floor and tablemats.

- Be careful of static electricity when handling the product.
- When handling the product, hold them by the case (package) and do not touch the terminals.
- Before touching the product, discharge any static electricity from your body and clothes by grounding out through a high impedance resistor (about 1MΩ)
- When soldering, insulate and ground the soldering iron and solder bus to prevent the leakage voltage from the soldering iron or solder bus from being applied to the product and damaging it.
- Do not apply mechanical stress that deform the terminals.
- During open short test, the internal of the product might explode instantaneously and the resin mold package might be blown off when high voltage is applied to the low voltage terminals. Make sure in your design that during open short test, high voltage will not be applied to the low voltage terminals. To avoid accidents and explosion damage if high voltage is applied, use fuses in your design.
- Please check electrical characteristic, thermal characteristic, and mechanical characteristic when considering replacement with another company's product.
- Do not use the product in parallel connection.

2. Precautions during transportation and storage

- The product should be stored at a normal temperature of 5 to 35°C and relative humidity of 45 to 75%, otherwise the product might be corroded or destructed, or it's lifetime might be shorter. If the storage area is very dry, a humidifier may be required. In such a case, use only deionized water or boiled water, since the chlorine in tap water may corrode the leads.
- In case of storage environment with rapid temperature changes, condensation will be occurred on the surface of the product. In order to avoid the condensation, the product shall be stored in steady temperature environment if possible.
- The product should not stored or used in an environment where it is exposed to acids, organic substances, or corrosive gas (hydrogen sulfide, sulfurous acid gas etc.) or in a dusty place.
- When stored, it is necessary to prevent external pressure to the product. Stacking that may deform the outer box shall be avoided even when it is packed in the outer box.
- Transport the cardboard box with the appropriate side facing up. This is to prevent unexpected stress being applied to the product, which may cause bending of the terminals or distortion in the resin package of the product. Throwing or dropping the product can cause significant damage to the product. Also, it is necessary to pay attention to rain and freezing to avoid wetting, as it may cause damage or destruction. The environmental conditions such as temperature and humidity during transportation described in the specifications shall be strictly observed.
- The product should be stored with the lead terminals remaining unprocessed. It is necessary to avoid rusting etc. due to scratches during processing, resulting in poor soldering.
- The containers and bags for storing the product should be non-static or conductive.
- Under the above storage condition, use the product within one year.