
Chapter 3

Detail of Signal Input/Output Terminals

Contents	Page
1. Control Power Supply Terminals V_{CCH}, V_{CCL}, COM	3-2
2. Power Supply Terminals of High Side $VB(U, V, W)$	3-6
3. Function of Internal BSDs (Boot Strap Diodes)	3-9
4. Input Terminals $IN(HU, HV, HW), IN(LU, LV, LW)$	3-13
5. Over Current Protection Input Terminal IS	3-16
6. Fault Status Output Terminal VFO	3-17
7. Temperature Sensor Output Terminal TEMP	3-18
8. Over Heat Protection	3-20

1. Control Power Supply Terminals V_{CCH}, V_{CCL}, COM

1. Voltage Range of control power supply terminals V_{CCH}, V_{CCL}

Control and gate drive power for this IPM is normally provided by a single 15Vdc supply that is connected to the V_{CCH}, V_{CCL} and COM terminals. For proper operation this voltage should be regulated to $15V \pm 10\%$. Table 3-1 describes the behavior of this IPM for various control supply voltages. The control supply should be well filtered with a low impedance electrolytic capacitor and a high frequency decoupling capacitor connected right at terminals.

High frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than $\pm 1V/\mu s$.

The voltage at the COM terminal is different from that at the $N(*)^{*1}$ power terminal by the sensing resistor. It is very important that all control circuits and power supplies are referred to the COM terminal and not to the $N(*)^{*1}$ terminals. If circuits are improperly connected, the additional current flowing through the sense resistor might cause improper operation of the short-circuit protection function. In general, it is best practice to make the COM a ground plane in the PCB layout.

The main control power supply is also connected to the bootstrap circuits that are used to establish the floating supplies for the high side gate drives.

When high side control supply voltage (V_{CCH} and COM) falls down under V_{CCH} UV (Under Voltage protection) level, the upper side IGBT, which is only triggered phase, is off state in spite of the input signal condition.

When low side control supply voltage (V_{CCL} and COM) falls down under V_{CCL} UV level, all lower side IGBTs are off state in spite of the input signal condition.

Table 3-1 Functions versus supply voltage V_{CCH}, V_{CCL}

Control Voltage Range [V]	Function Operations
0 ~ 4	HVICs and LVIC are not activated. UV and fault output do not operate. dV/dt noise on the main P-N supply might trigger the IGBTs.
4 ~ 13	HVICs and LVIC start to operate. As UV is activated, control input signals are blocked and a fault output VFO is generated.
13 ~ 13.5	UV is reset. IGBTs are operated in accordance with the control gate input. Driving voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition and high side IGBTs can't operate after $VB(*)^{*2}$ initial charging because $VB(*)$ can't reach to $V_{B(ON)}$.
13.5 ~ 16.5	Normal operation. This is the recommended operating condition.
16.5 ~ 20	The lower side IGBTs are still operated. Because driving voltage is above the recommended range, IGBT's switching is faster. It causes increasing system noise. And peak short circuit current might be too large for proper operation of the short circuit protection.
Over 20	Control circuit in this IPM might be damaged. If necessary, it is recommended to insert a zener-diode between each pair of control supply terminals.

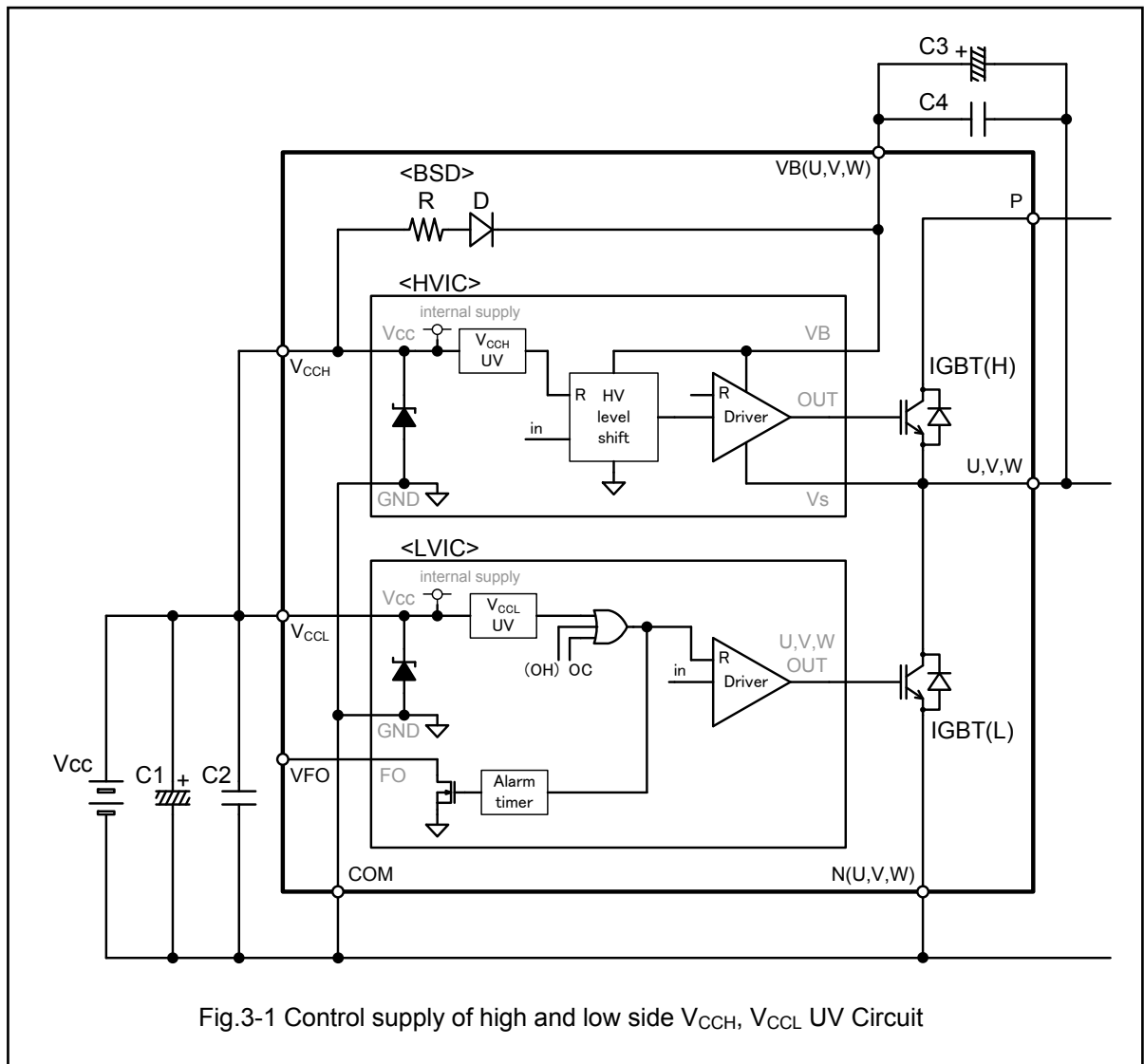
1 $N()$: $N(U), N(V), N(W)$

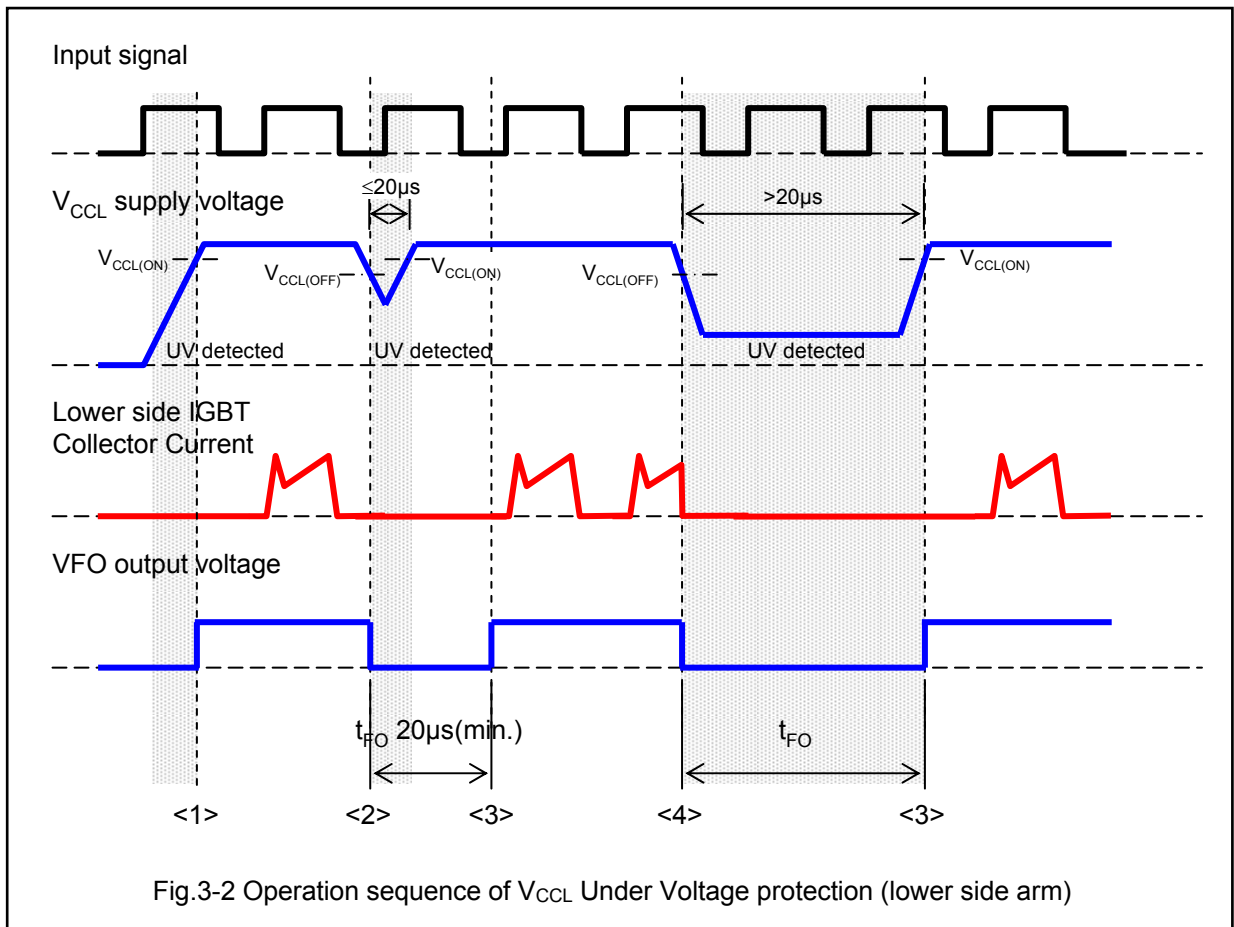
2 $VB()$: $VB(U)-U, VB(V)-V, VB(W)-W$

2. Under Voltage protection of control power supply terminals V_{CCH} , V_{CCL}

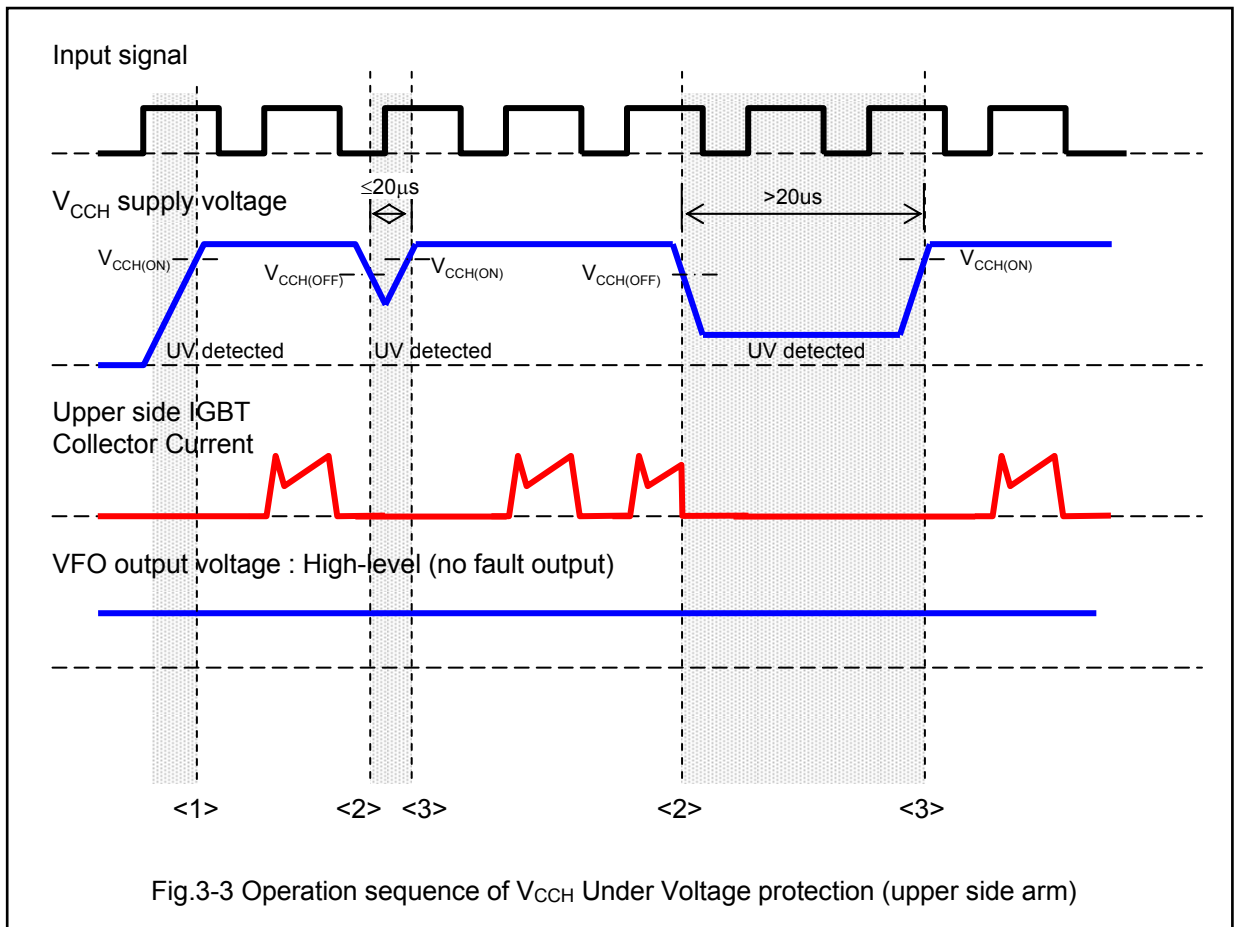
Fig.3-1 shows control supply of high and low side (V_{CCH} , V_{CCL} and COM) UV circuit block, and Fig.3-2 and Fig.3-3 shows UV operation sequence of V_{CCH} and V_{CCL} .

Fig.3-1 shows that the diodes are electrically connected to the V_{CCH} , V_{CCL} and COM terminals. They should not be used for the voltage clamp intentionally to prevent from major problems and destroy.





- <1> When V_{CCL} is under $V_{CCL(ON)}$, all lower side IGBTs are OFF state.
After V_{CCL} rises $V_{CCL(ON)}$, the fault output VFO is released (high level).
And the LVIC starts to operate, then next input is activated.
- <2> The fault output VFO is activated when V_{CCL} falls below $V_{CCL(OFF)}$, and all lower side IGBT remains OFF state.
When the voltage drop time is less than $20\mu s$, the fault output pulse width is generated minimum $20\mu s$ and all lower side IGBTs are OFF state in spite of input signal condition during that time.
- <3> UV is reset after t_{FO} when V_{CCL} exceeds $V_{CCL(ON)}$ and the fault output VFO is reset simultaneously.
And the LVIC starts to operate, then next input is activated.
- <4> When the voltage drop time is more than t_{FO} , the fault output pulse width is generated and all lower side IGBTs are OFF state in spite of input signal condition during the same time.



- $\langle 1 \rangle$ When V_{CCH} is under $V_{CCH(ON)}$, the upper side IGBT is OFF state.
After V_{CCH} exceeds $V_{CCH(ON)}$, the HVIC starts to operate. Then next input is activated.
The fault output VFO is constant (high level) not to depend on V_{CCH} .
- $\langle 2 \rangle$ After V_{CCH} falls below $V_{CCH(OFF)}$, the upper side IGBT remains OFF state.
But the fault output VFO keeps high level.
- $\langle 3 \rangle$ The HVIC starts to operate after UV is reset, then next input is activated.

2. Power Supply Terminals of High Side VB(U,V,W)

1. Voltage Range of high side bias voltage for IGBT driving terminals VB(U,V,W)

The VB(*) voltage, which is the voltage difference between VB(U,V,W) and U,V,W, provides the supply to the HVICs within the IPM. This supply must be in the range of 13.0~18.5V to ensure that the HVICs can fully drive the upper side IGBTs. The IPM includes UV function for the VB(*) to ensure that the HVICs do not drive the upper side IGBTs, if the VB(*) voltage drops below a specified voltage (refer to the datasheet). This function prevents the IGBT from operating in a high dissipation mode. Please note here, that the UV (under voltage protection) function of any high side section acts only on the triggered channel without any feedback to the control level.

In case of using bootstrap circuit, the IGBT drive power supply of an upper side arm can be composed of one common power supply with a lower side arm. In the conventional IGBT drive circuit for upper side arm was necessary for the three independent power supply.

The power supply of an upper side arm is charged by the turned on the lower side IGBT or freewheel current flows the lower side IGBT. Table 3-2 describes the behavior of the IPM for various control supply voltages. The control supply should be well filtered with a low impedance electrolytic capacitor and a high frequency decoupling capacitor connected right at the terminals, because the high frequency noise on the supply might cause the internal control IC to malfunction.

When control supply voltage (VB(U)-U,VB(V)-V and VB(W)-W) falls down under UV (Under Voltage protection) level, only triggered phase IGBT is off state in spite of the input signal condition.

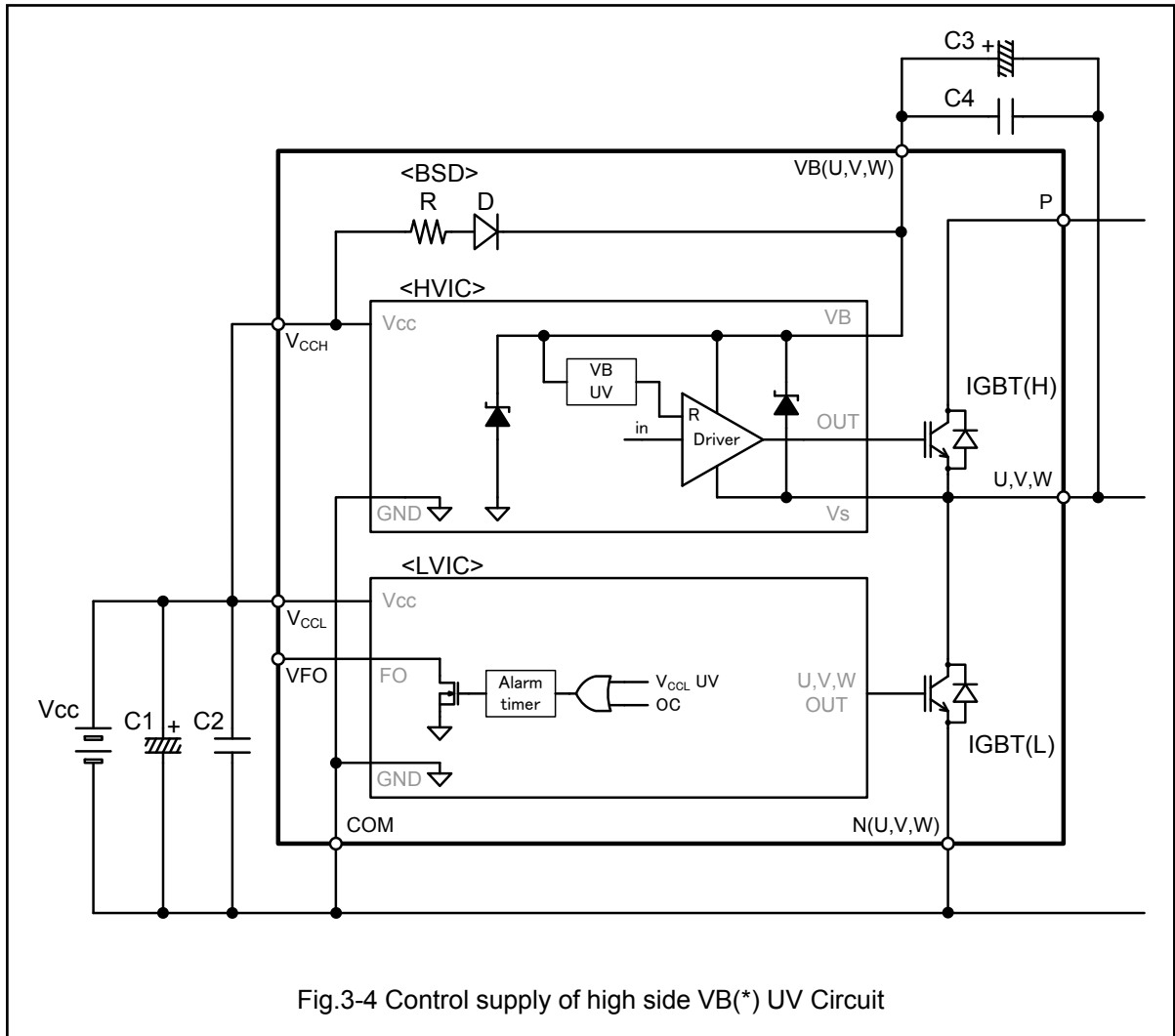
Table 3-2 Functions versus high side bias voltage for IGBT driving VB(*)

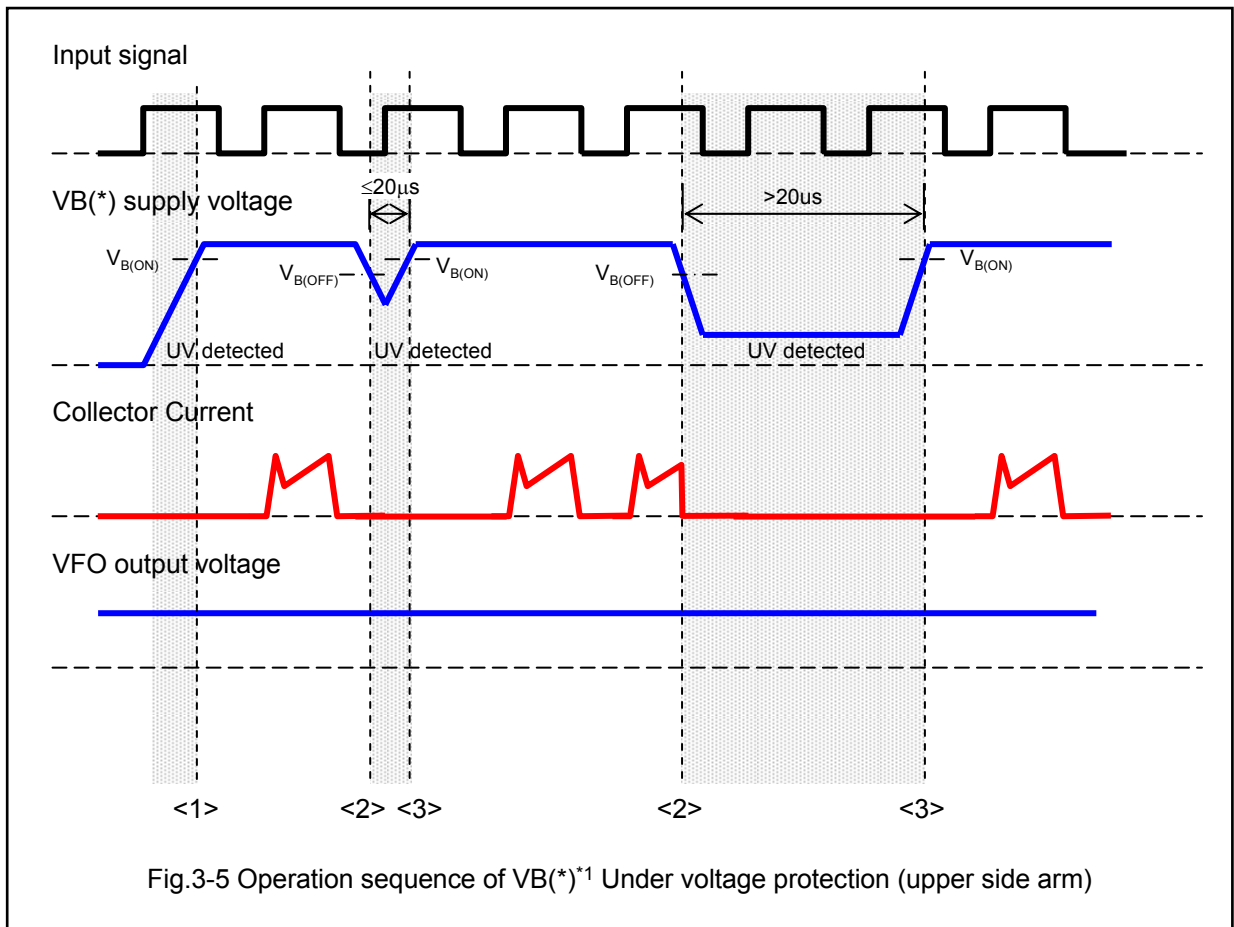
Control Voltage Range [V]	The IPM function operations
0 ~ 4	HVICs are not activated. UV does not operate. dV/dt noise on the main P-N supply might trigger the IGBTs.
4 ~ 12.5	HVICs start to operate. As the UV is activated, control input signals are blocked.
12.5 ~ 13	UV is reset. The upper side IGBTs are operated in accordance with the control gate input. Driving voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition.
13 ~ 18.5	Normal operation. This is the recommended operating condition.
18.5 ~ 20	The upper side IGBTs are still operated. Because driving voltage is above the recommended range, IGBT's switching is faster. It causes increasing system noise. And peak short circuit current might be too large for proper operation of the short circuit protection.
Over 20	Control circuit in the IPM might be damaged.

2. Under Voltage protection of high side power supply terminals VB(U,V,W)

Fig.3-4 shows control supply of high side (VB(U)-U,VB(V)-V and VB(W)-W) UV (Under Voltage protection) circuit block, and Fig.3-5 shows operation sequence of V_{CCL}, V_{CCH} Under Voltage operation.

Fig.3-4 shows that the diodes are electrically connected to the VB(U,V,W), U,V,W and COM terminals. They should not be used for the voltage clamp intentionally to prevent major problems and destroy the IPM.





- <1> When VB(*) is under $V_{B(ON)}$, the upper side IGBT is OFF state.
After VB(*) exceeds $V_{B(ON)}$, the HVIC starts to operate. Then next input is activated.
The fault output VFO is constant (high level) not to depend on VB(*).
- <2> After VB(*) falls below $V_{B(OFF)}$, the upper side IGBT remains OFF state.
But the fault output VFO keeps high level.
- <3> The HVIC starts to operate after UV is reset, then next input is activated.

1 VB() : VB(U)-U,VB(V)-V,VB(W)-W

3. Function of Internal BSDs (bootstrap Diodes)

There are a number of ways in which the $V_{B(*)}^{*1}$ floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and cheap. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of an internal diode with resistor and an external capacitor as shown in Fig.3-6, Fig.3-8 and Fig.3-11. The current flow path of the bootstrap circuit is shown in the same Fig.3-6, Fig.3-8 and Fig.3-11.

1. Charging and Discharging of the Bootstrap Capacitor During Inverter Operation

a) Charging operation Timing Chart of Bootstrap Capacitor (C)

<Sequence (Fig.3-7) : lower side IGBT is turn-on in Fig.3-6>

When lower side IGBT is in ON state, charging voltage on bootstrap capacitance $V_c(t_1)$ is calculated by

$$V_c(t_1) = V_{CC} - V_F - V_{CE(sat)} - I_b \cdot R \quad \dots \dots \text{Transient state}$$

$$V_c(t_1) \approx V_{CC} \quad \dots \dots \text{Steady state}$$

- V_F : Forward voltage of Boost strap diode (D)
- $V_{CE(sat)}$: Saturation voltage of lower side IGBT
- R : inrush current limitation of bootstrap resistance (R)
- I_b : Charge current of bootstrap

Then, lower side IGBT is turn off. Motor current will flow through the free-wheel path of the upper side FWD. Once the electric potential of VS rises near to that of P terminal, the charging to C is stopped.

When the upper side IGBT is in ON state, the voltage of C gradually declines from the potential VC due to the current consumed by the drive circuit.

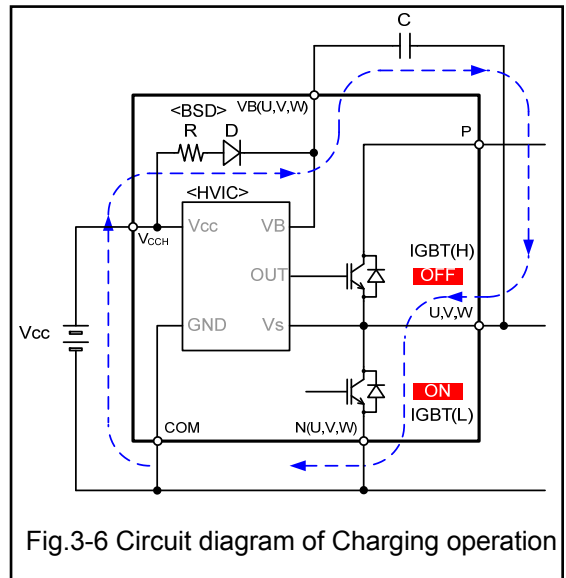


Fig.3-6 Circuit diagram of Charging operation

1 $V_{B()}$: $V_B(U)-U, V_B(V)-V, V_B(W)-W$

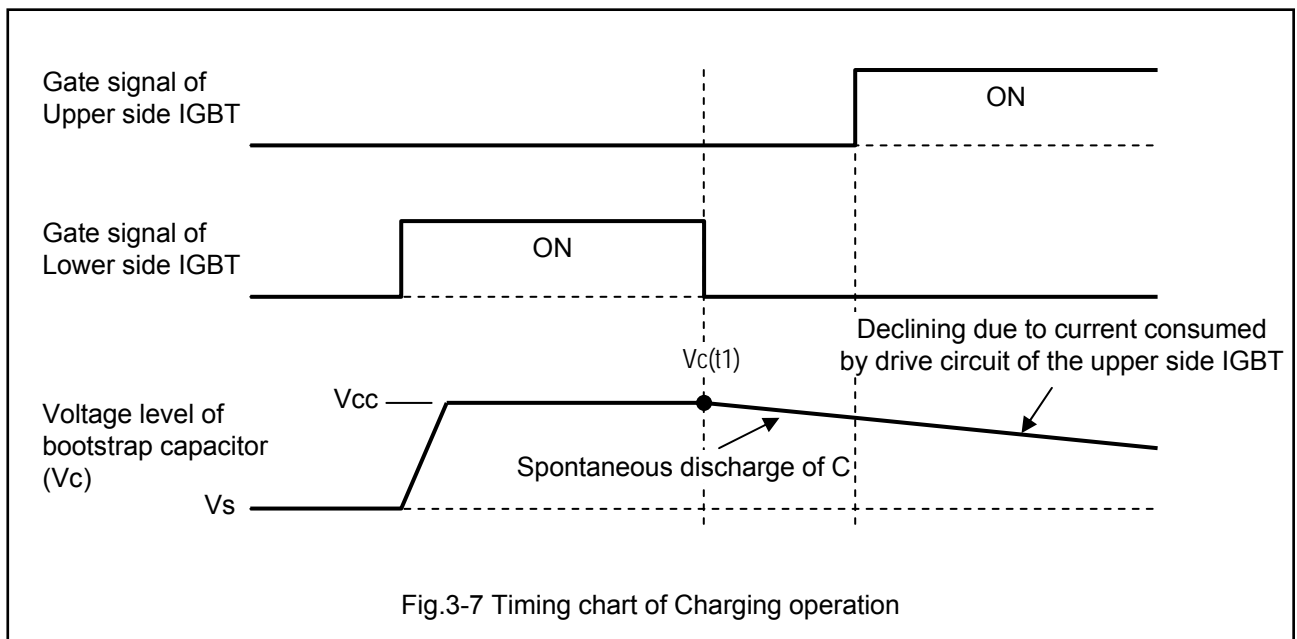


Fig.3-7 Timing chart of Charging operation

<Sequence (Fig.3-9): Lower side IGBT is OFF and Lower side FWD is ON (Freewheel current flows) in Fig.3-8 >

When the lower side IGBT is OFF and the lower side FWD is ON, means free wheel current flows the lower side FWD, the voltage on bootstrap capacitance $V_c(t_2)$ is calculated by:

$$V_c(t_2) = V_{CC} - V_F + V_{F(FWD)} - I_b \cdot R \dots\dots \text{Transient state}$$

$$V_c(t_2) \approx V_{CC} \dots\dots \text{Steady state}$$

V_F : Forward voltage of Boost strap diode (D)
 $V_{F(FWD)}$: Forward voltage of lower side FWD

R : inrush current limitation of bootstrap resistance (R)
 I_b : Charge current of bootstrap

When both the lower side IGBT and the upper side IGBT are OFF, the regenerative current flows continuously through the freewheel path of the lower side FWD. Therefore the potential of V_s drops to $-V_F(FWD)$, then bootstrap capacitance is recharged to restore the declined potential. When the upper side IGBT is turned ON, the potential of V_s rises to that of the terminal P, the charge to the bootstrap capacitance stops and the voltage on the bootstrap capacitance gradually declines from the potential $V_c(t_2)$ due to the current consumed by the drive circuit.

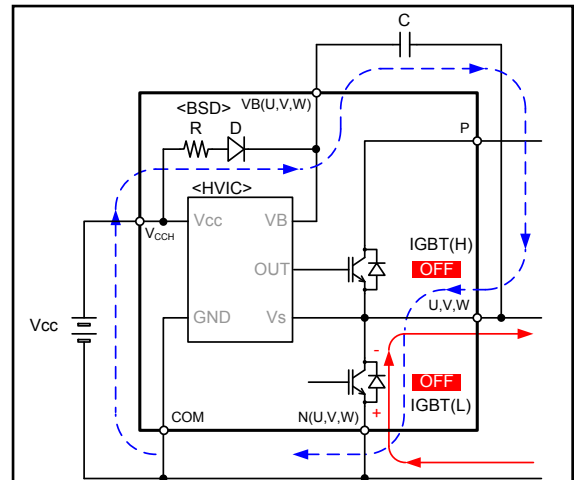


Fig.3-8 Circuit diagram of Charging operation under the lower side arm FWD is ON

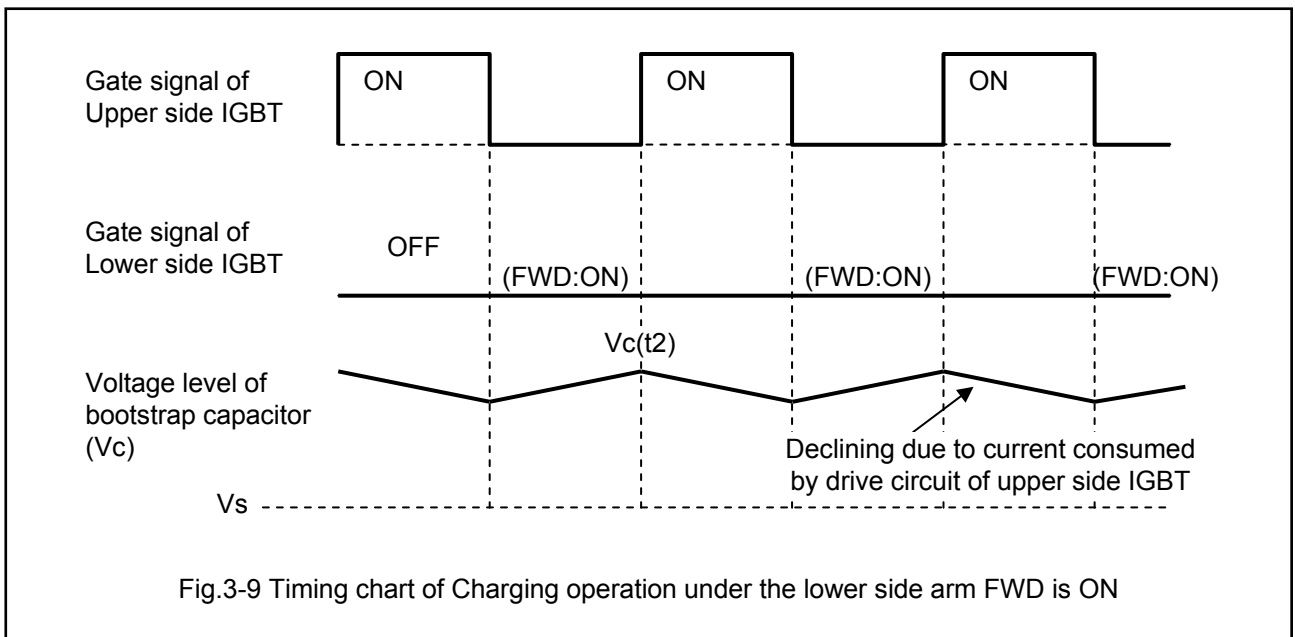


Fig.3-9 Timing chart of Charging operation under the lower side arm FWD is ON

2) Setting the bootstrap Capacitance and minimum ON/OFF pulse width

The parameter of bootstrap capacitor can be calculated by:

$$C = I_b \cdot \frac{t_1}{dV}$$

- * t1 : the maximum ON pulse width of the upper side IGBT
- * I_b : the drive current of the HVIC (depends on temperature and frequency characteristics)
- * dV: the allowable discharge voltage. (see Fig.3-10)

A certain margin should be added to the calculated capacitance.

The bootstrap capacitance is generally selected as large as 2~3 times of the calculated one.

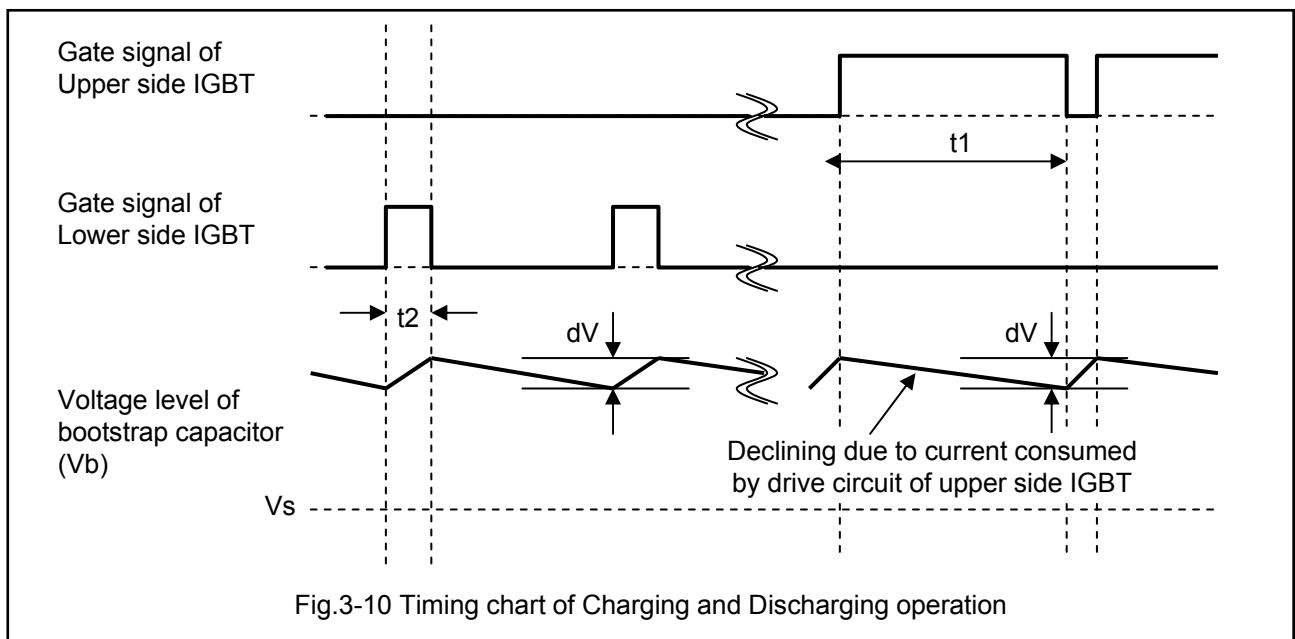
The recommended minimum ON pulse width (t₂) of the lower side IGBT should be basically determined such that the time constant C·R will enable the discharged voltage (V) to be fully charged again during the ON period.

However, if only upper side IGBT has an ON-OFF-ON control mode (Sequence Fig.3-10), the time constant should be set so that the consumed energy during the ON period can be charged during the OFF period.

The minimum pulse choice the minimum ON pulse width of the lower side IGBT or the minimum OFF pulse width of the upper side IGBT.

$$t_2 \geq \frac{R \cdot C \cdot dV}{V_{CC} - V_{b(\min)}}$$

- * R : Series resistance of Bootstrap diode ΔRF(BSD)
- * C : Bootstrap capacitance
- * dV: the allowable discharge voltage.
- *V_{CC} : Voltage of HVICs and LVIC power supply (ex.15V)
- *V_{b(min)} : the minimum voltage of the upper side IGBT drive (Added margin to UV. ex. 14V)



3) Setting the bootstrap capacitance for Initial charging

The initial charge of the bootstrap capacitance is necessary to start-up the inverter.
The pulse width or pulse number should be large enough to make a full charge of the bootstrap capacitance.
For reference, the charging time for the bootstrap circuit with a 10 μ F capacitor and internal bootstrap diode is about 2ms.

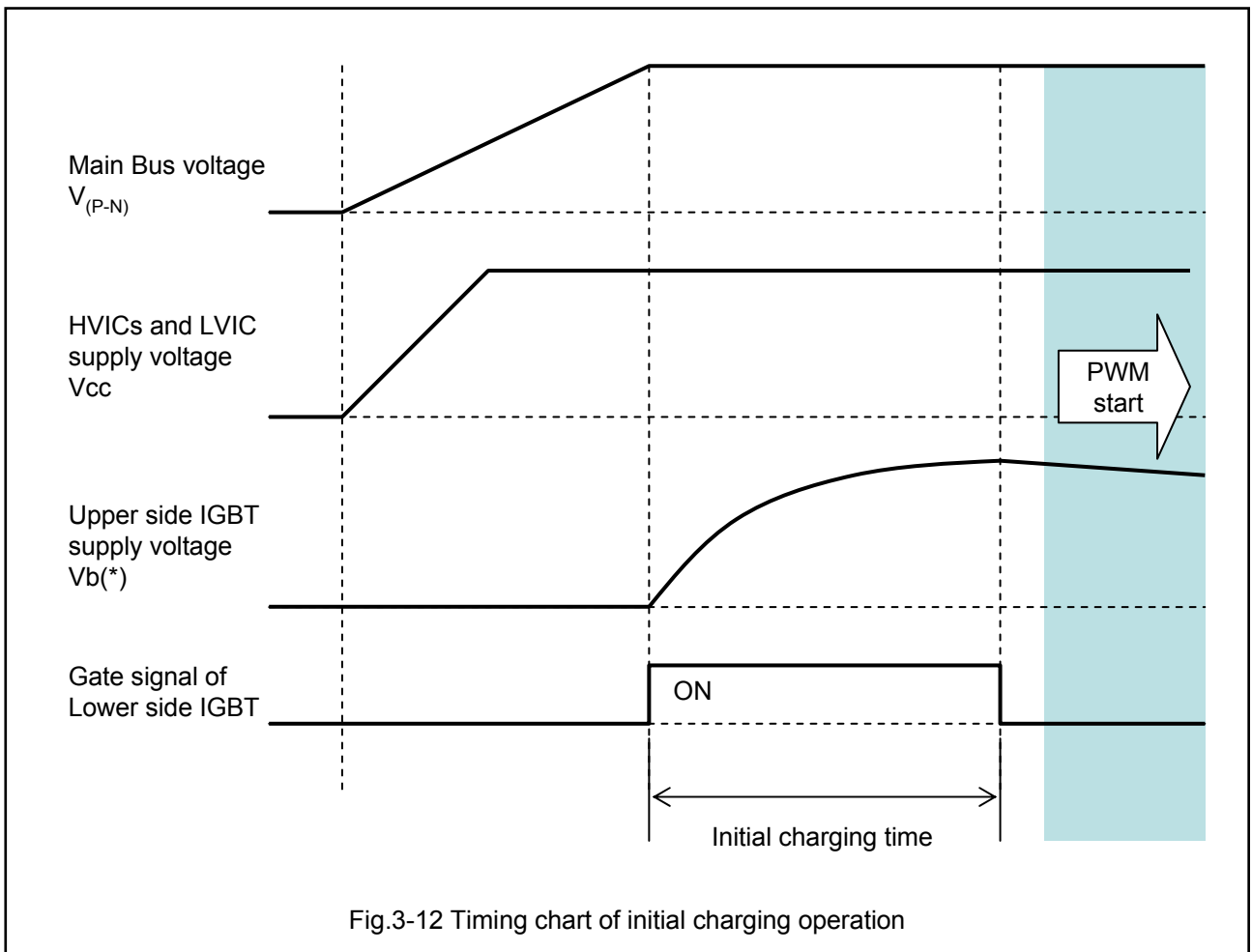
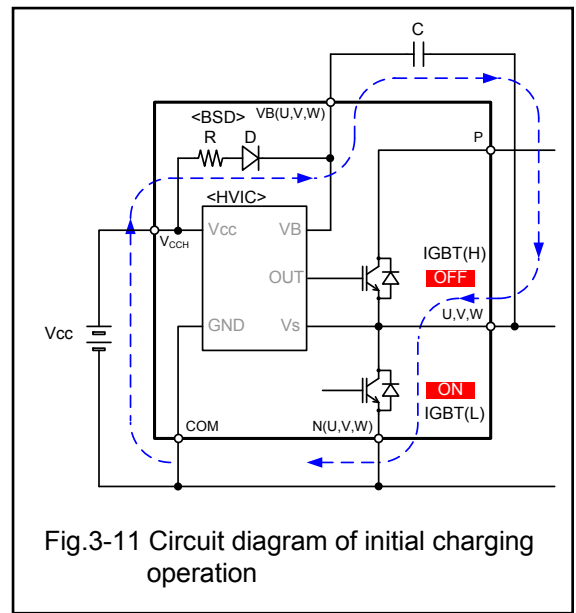


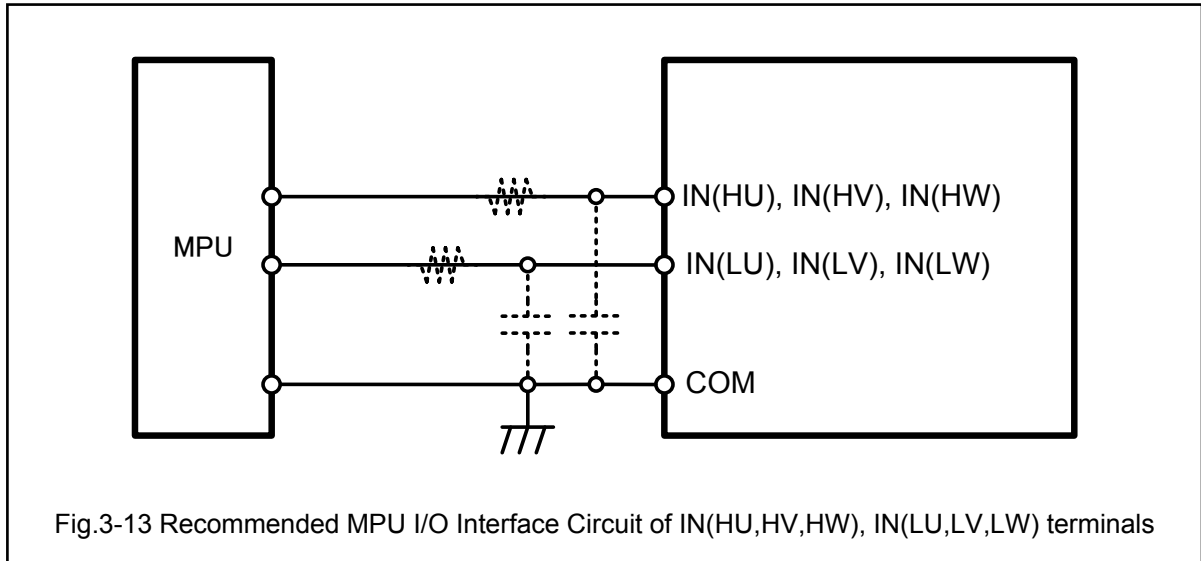
Fig.3-12 Timing chart of initial charging operation

4. Input Terminals IN(HU,HV,HW), IN(LU,LV,LW)

1. Input terminals Connection

Fig.3-13 shows the input interface circuit between the MPU and the IPM. It is possible that the input terminals connect directly to the MPU. It should not need the external pull up and down resistors connected to the input terminals, input logic is active high and the pull down resistors are built in.

The RC coupling at each input (parts shown dotted in Fig.3-13) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's PCB layout.

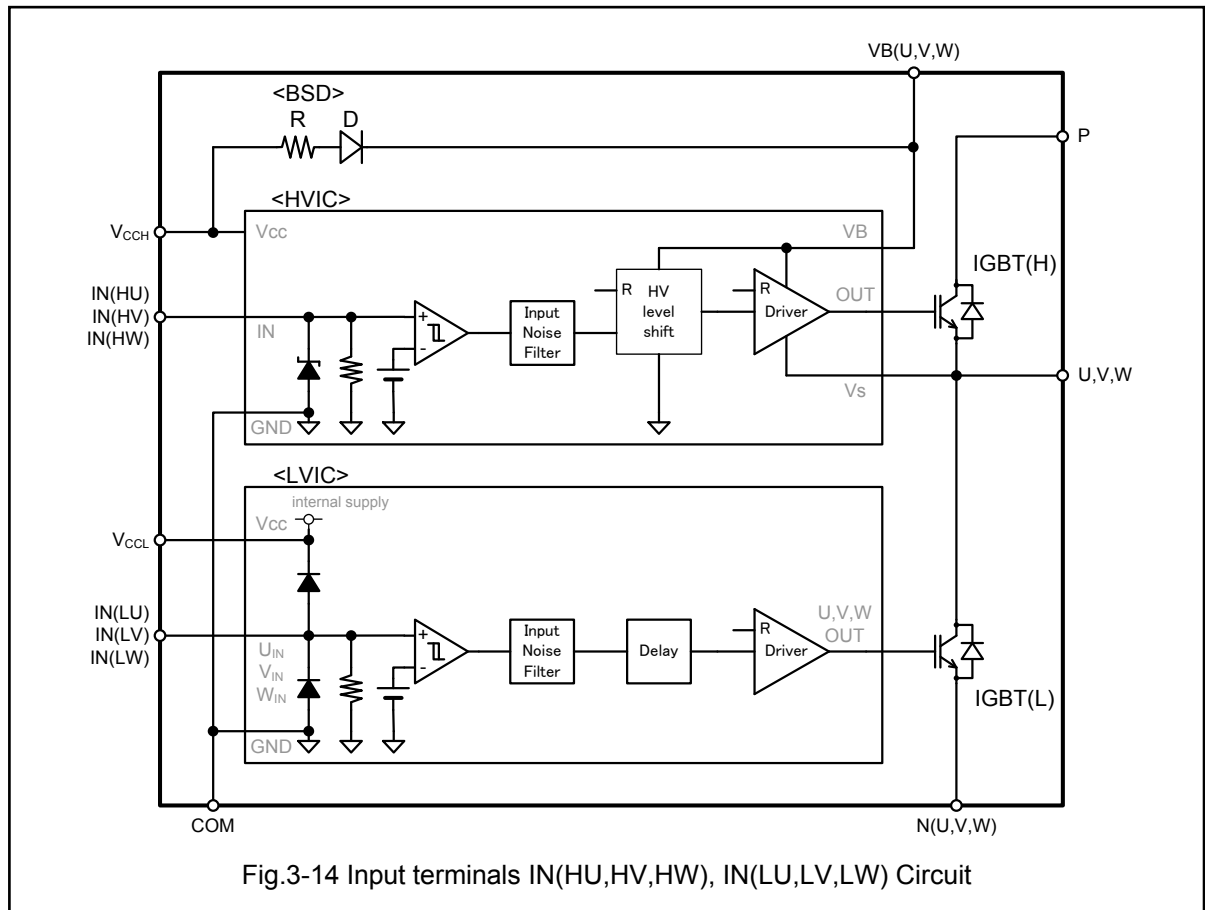


2. Input terminal circuit

The input logic of this IPM is active high. This logic has removed the sequence restriction between the control supply and the input signal during startup or shutdown operation. Therefore it makes the system failsafe. In addition, the pull down resistors are built in to each input terminals in Fig.3-14. Thus, external pull-down resistors are not needed reducing the required external component. Furthermore, a direct connection to 3.3V-class MPU by the low input signal threshold voltage.

As shown in Fig.3-14, the input circuit integrates a pull-down resistor. Therefore, when using an external filtering resistor between the MPU output and input of the IPM, please care to the signal voltage drop at the input terminals to satisfy the turn-on threshold voltage requirement. For instance, $R=100\Omega$ and $C=1000pF$ for the parts shown dotted in Fig.3-13.

Fig.3-14 shows that the internal diodes are electrically connected to the V_{CC} , IN(HU, HV, HW, LU, LV, LW) and COM terminals. They should not be used for the voltage clamp intentionally to prevent major problems and destroy the IPM.



3. IGBT drive state versus Control signal pulse width

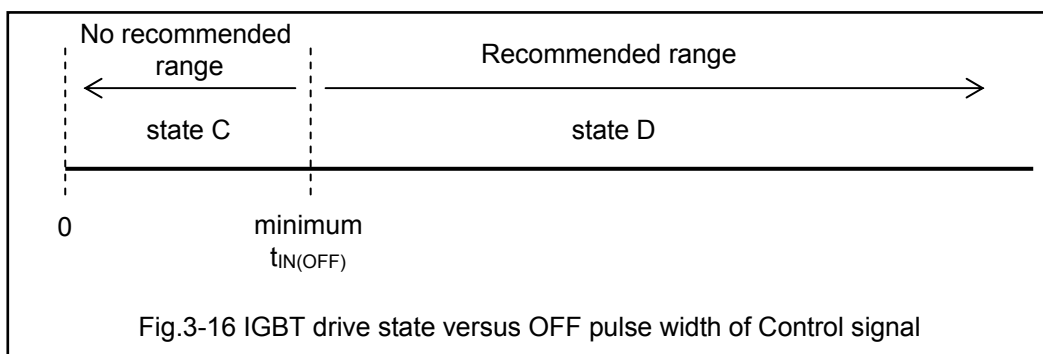
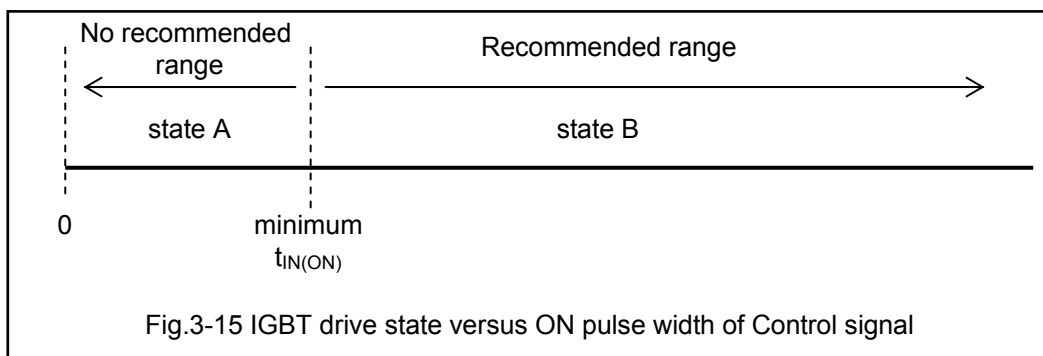
It is provided that $t_{IN(ON)}$ is the control signal pulse width necessary to change from OFF to ON and $t_{IN(OFF)}$ is from ON to OFF. Fig.3-15 and Fig.3-16 show IGBT drive state for various control signal pulse width.

state A : IGBT may turn on occasionally, even when the ON pulse width of control signal is less than minimum $t_{IN(ON)}$. Also if the ON pulse width of control signal is less than minimum $t_{IN(ON)}$ and voltage is applied below -5V between U-COM,V-COM,W-COM , it may not turn off by the malfunction of the control circuit.

state B : IGBT can turn on and is saturated under normal condition.

state C : IGBT may turn on occasionally, even when the ON pulse width of control signal is less than minimum $t_{IN(OFF)}$. Also if the OFF pulse width of control signal is less than minimum $t_{IN(OFF)}$ and voltage is applied below -5V between U-COM, V-COM, W-COM , it may not turn on by the malfunction of the control circuit.

state D : IGBT can turn fully off under normal condition.



5. Over Current Protection Input Terminal IS

Over current protection (OC) is a function of detecting the IS voltage determined with the external shunt resistor, connected to N(*)^{*1} and COM.

Fig.3-17 shows over current sensing voltage input IS circuit block, and Fig.3-18 shows OC operation sequence.

To prevent the IPM erroneous from the normal switching noise or recovery current, it is necessary to set an external R-C filter (time constant is approximately 1.5μs) to the IS terminal. Also the IPM and the shunt resistor should be wired as short as possible.

Fig.3-17 shows that the diodes in the IPM are electrically connected to the V_{CCL}, IS and COM terminals. They should not be used for the voltage clamp intentionally to prevent major problems and destroy the IPM.

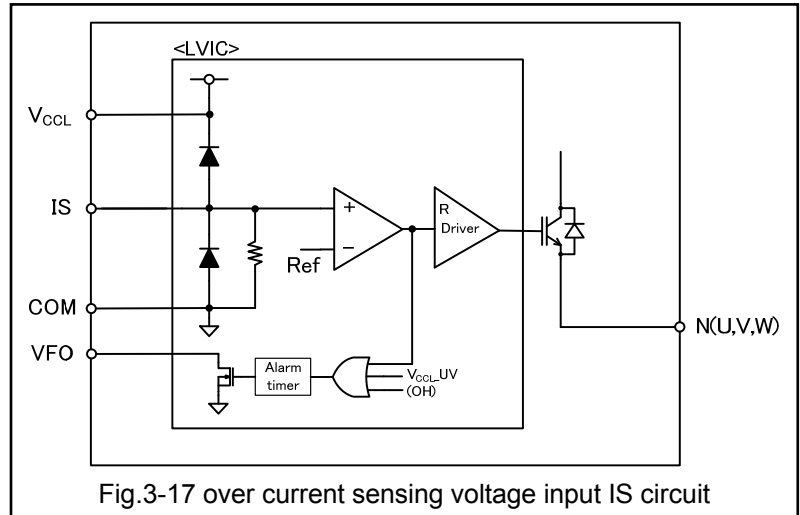


Fig.3-17 over current sensing voltage input IS circuit

1 N() : N(U), N(V), N(W)

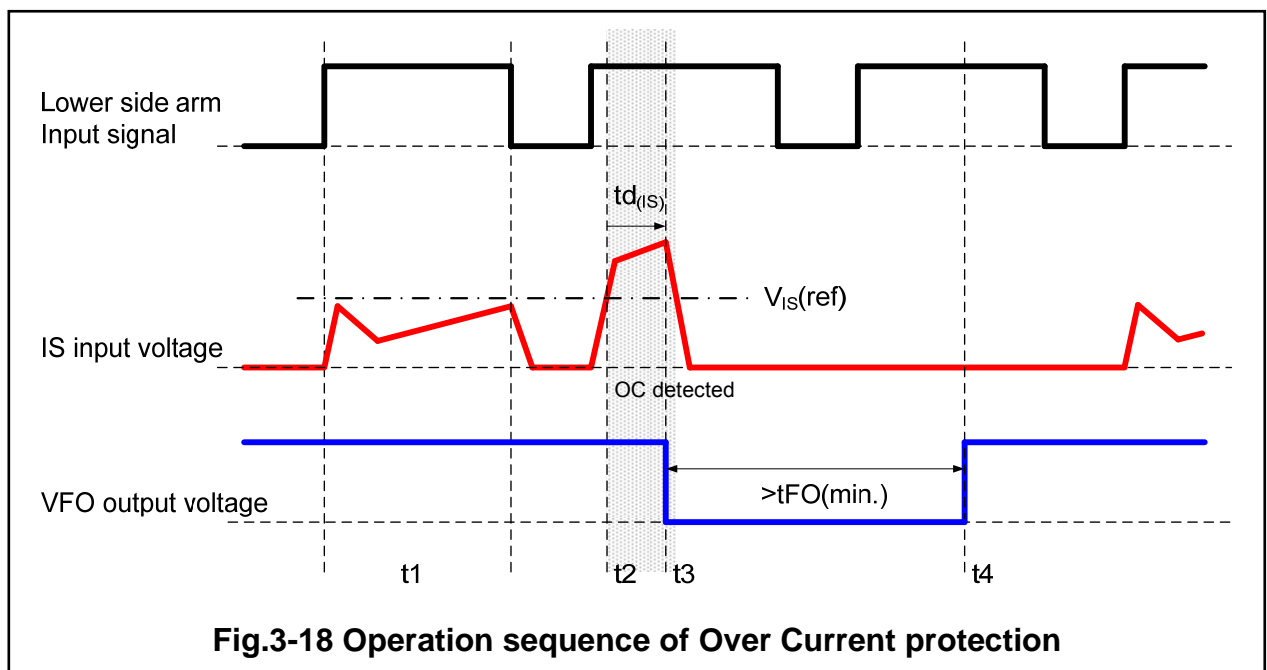


Fig.3-18 Operation sequence of Over Current protection

t1 : IS input voltage does not exceed $V_{IS(ref)}$, while the collector current of the lower side IGBT is under the normal operation.

t2 : When IS input voltage exceeds $V_{IS(ref)}$, the OC is detected.

t3 : The fault output VFO is activated and all lower side IGBT shut down simultaneously after the over current protection delay time $t_{d(IS)}$. Inherently there is dead time of LVIC in $t_{d(IS)}$.

t4 : After the fault output pulse width tFO , the OC is reset. Then next input signal is activated.

6. Fault Status Output Terminal VFO

As shown in Fig.3-19, it is possible that the fault status output VFO terminal connects directly to the MPU. VFO terminal is open drain configured, thus this terminal should be pulled up by a resistor of approximate 10kΩ to the positive side of the 5V or 3.3V external logic power supply, which is the same as the input signals. It is also recommended that the by-pass capacitors C1 should be connected at the MPU, and the inrush current limitation resistance R1, which is more than 5kΩ, should be connected between the MPU and the VFO terminal. These signal lines should be wired as short as possible to each device.

Fault status output VFO function is activated by the UV of V_{CCL}, OC and OH. (OH is applied to "6MBP15VRB060-50" and "6MBP15VRC060-50".)

Fig.3-19 shows that the diodes in the IPM are electrically connected to the V_{CCL}, VFO and COM terminals. They should not be used for the voltage clamp intentionally to prevent major problems and destroy the IPM.

Fig.3-20 shows Voltage-current characteristics of VFO terminal at fault state condition. The IFO is the sink current of the VFO terminal as shown in Fig.3-19.

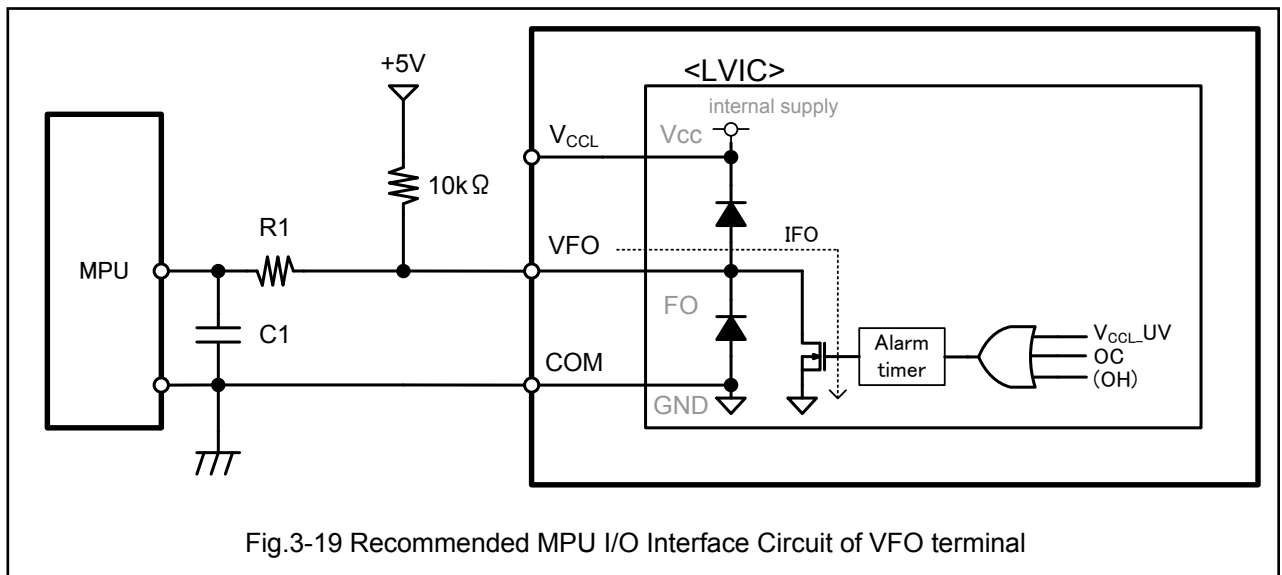


Fig.3-19 Recommended MPU I/O Interface Circuit of VFO terminal

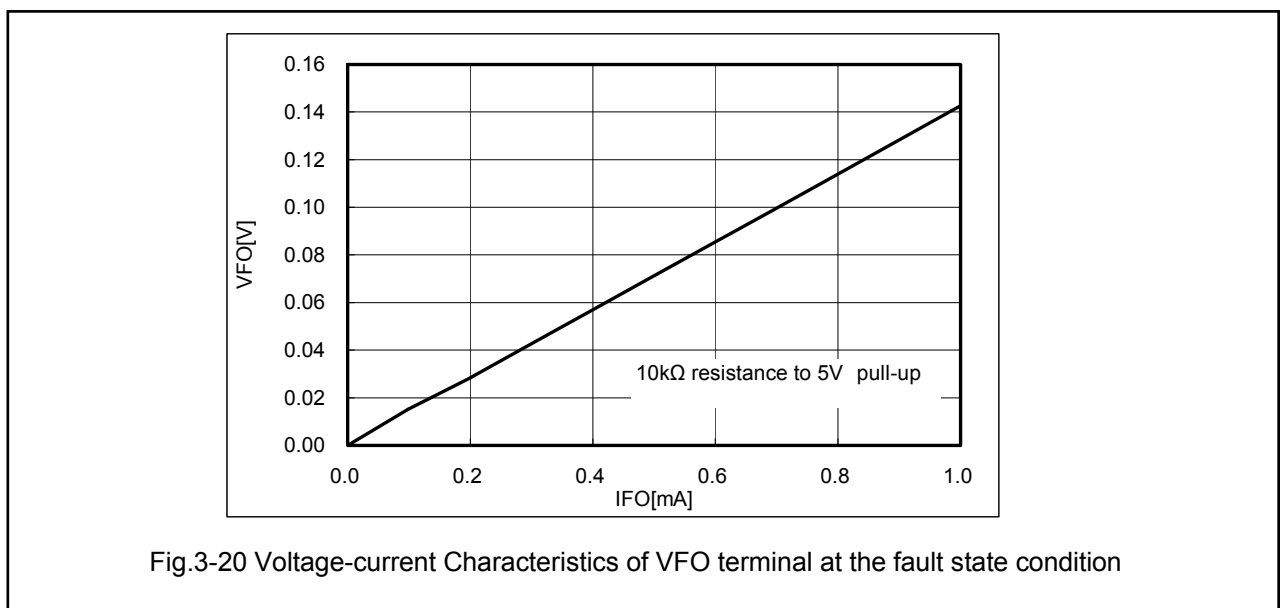


Fig.3-20 Voltage-current Characteristics of VFO terminal at the fault state condition

7. Temperature Sensor Output Terminal TEMP

This function is applied to "6MBP15VRA060-50", "6MBP15VRC060-50" and "6MBP15VRD060-50".

Fig.3-21 shows that the temperature sensor output TEMP terminal connects directly to the MPU. It is recommended that the by-pass capacitors should be connected at the MPU, and the inrush current limitation resistance, which is more than 10kΩ, should be connected between the MPU and the TEMP terminal. These signal lines should be wired as short as possible to each device.

The IPM builds in the temperature sensor, and outputs the analog voltage according to the LVIC temperature. In this function, the IPM does not protect by itself and no fault status is outputted.

The diodes in the IPM are electrically connected to the TEMP and COM terminals. They should not be used for the voltage clamp intentionally to prevent major problems and destroy the IPM.

Fig.3-22 shows the LVIC temperature versus TEMP output voltage characteristics. It should be connected the TEMP terminal to a zener diode for the voltage clamp when the power supply of MPU is 3.3V.

Fig.3-23 shows the operation sequence of TEMP terminal at the LVIC startup and shutdown conditions.

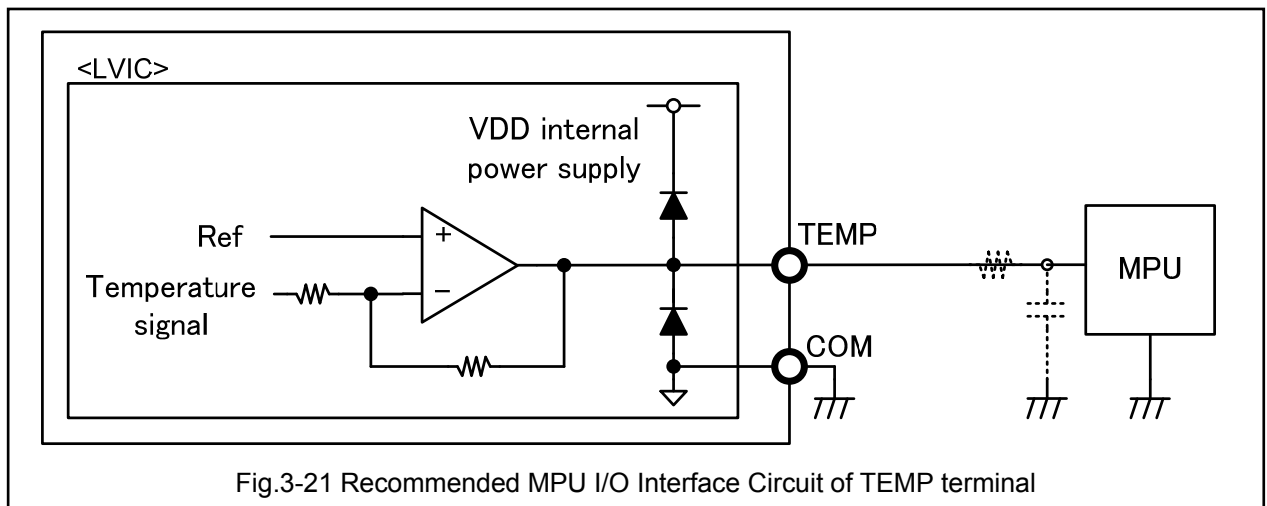
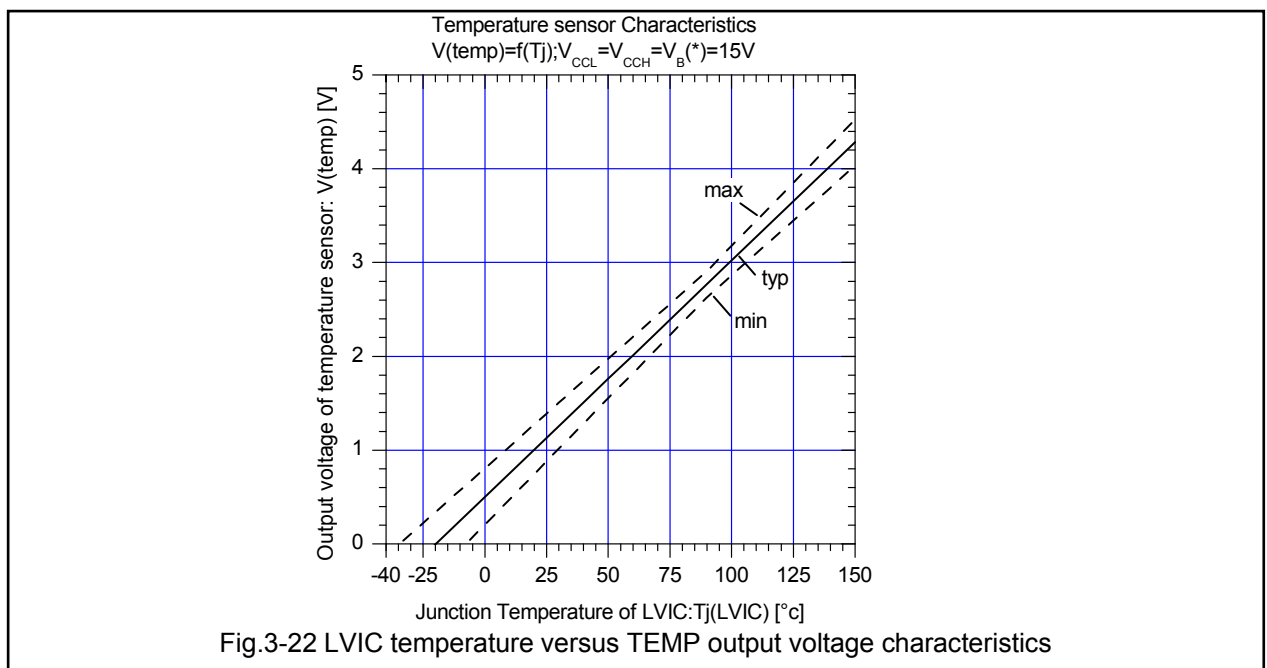
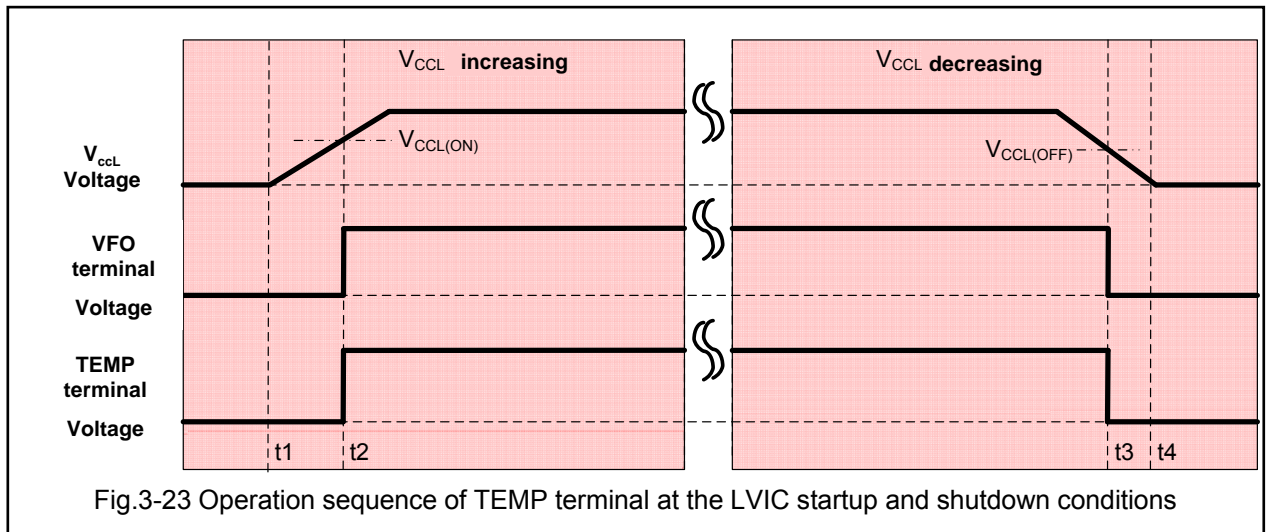


Fig.3-21 Recommended MPU I/O Interface Circuit of TEMP terminal





t1-t2 : TEMP function is activated when V_{CCL} exceeds $V_{CCL(ON)}$. TEMP terminal voltage has nearly 0V when V_{CCL} is less than $V_{CCL(ON)}$.

t2-t3 : TEMP terminal voltage rises to the voltage determined with LVIC temperature.

t3-t4 : TEMP function is reset when V_{CCL} falls below $V_{CCL(OFF)}$. TEMP terminal voltage becomes shutdown and output 0V.

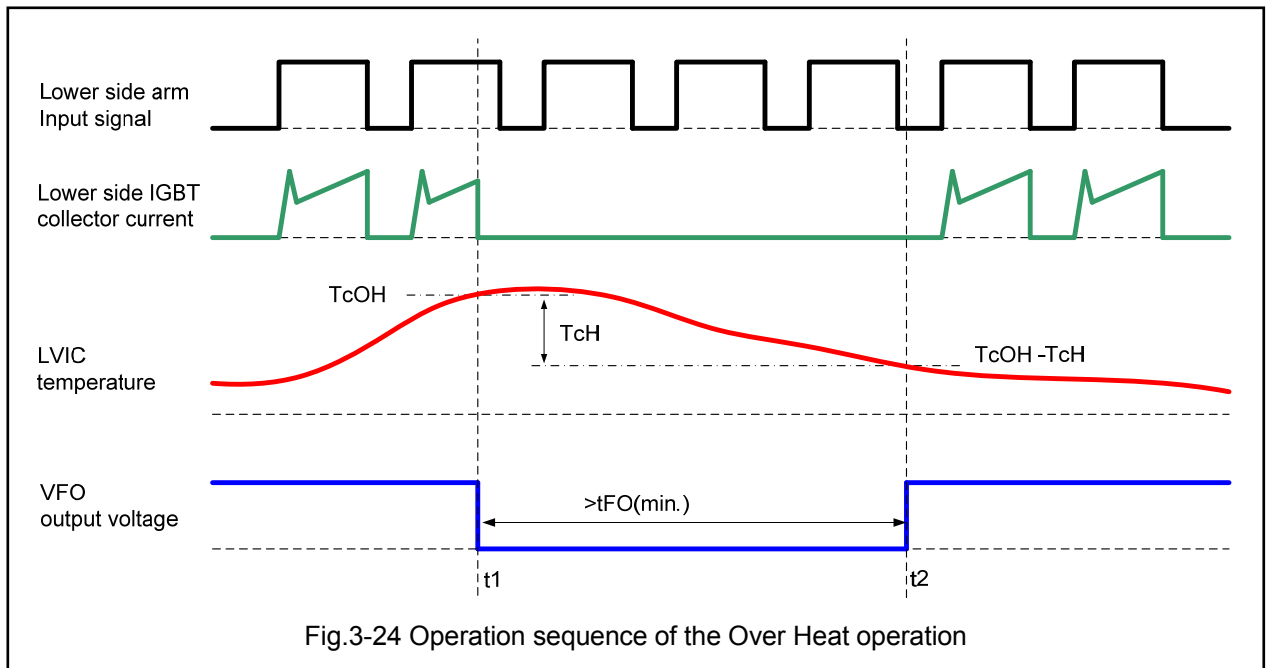
8. Over Heat Protection

This function is applied to "6MBP15VRB060-50" and "6MBP15VRC060-50".

The IPM has the over-heating protection (OH) function by monitoring the LVIC temperature.

The TcOH sensor position is shown in Fig.2-2.

As shown in Fig.3-24, the IPM shutdown all lower side IGBTs while the LVIC temperature exceeds TcOH. The fault status is reset when the LVIC temperature drops below (TcOH-TcH).



- t1 : The fault status is activated and all IGBTs of the lower side arm shutdown, when LVIC temperature exceeds case overheating protection (OH) temperature TcOH.
- t2 : The fault status, which outputs over tFO, is reset and next input signal is activated, when LVIC temperature falls below TcOH - TcH which is the case overheating protection hysteresis.