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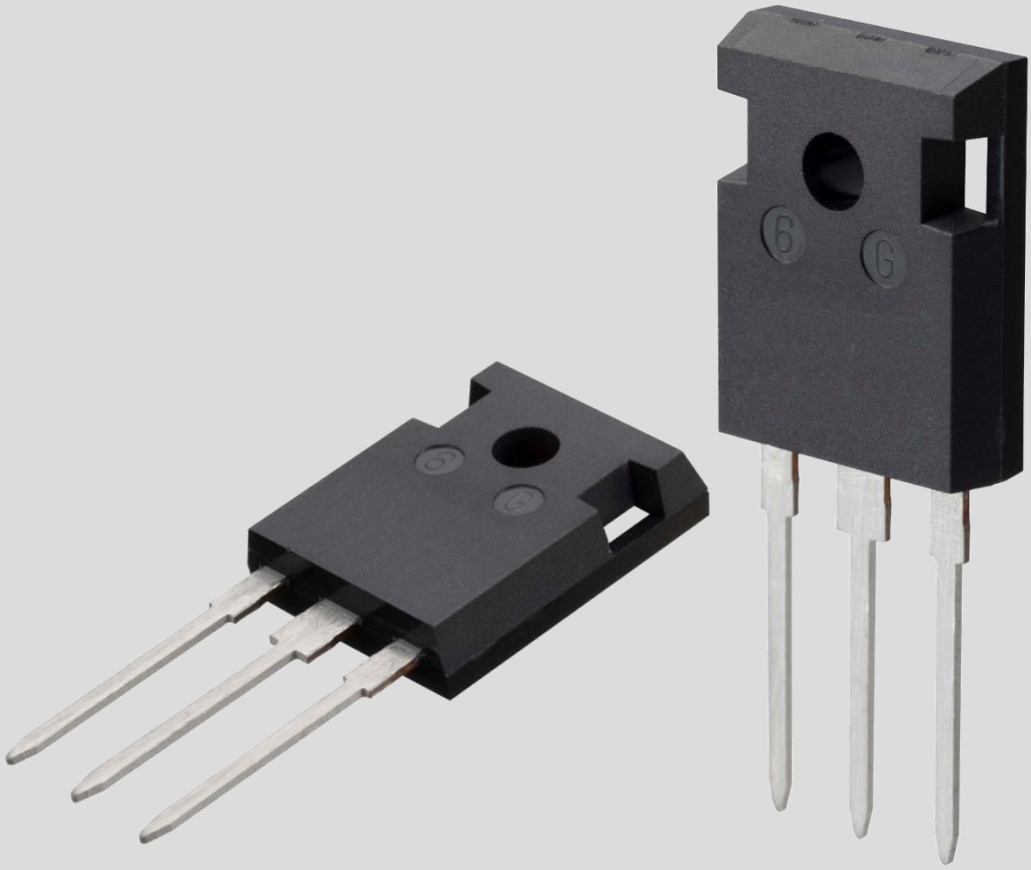

Fuji Discrete IGBT
TO-247-P

Application Manual

Feb. 1st, 2021 Rev1.0

Fuji Electric Co., Ltd.

MT5F43750

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Chapter 7 Typical Troubles and Troubleshooting

Chapter 8 Precautions for Storage and Transportation

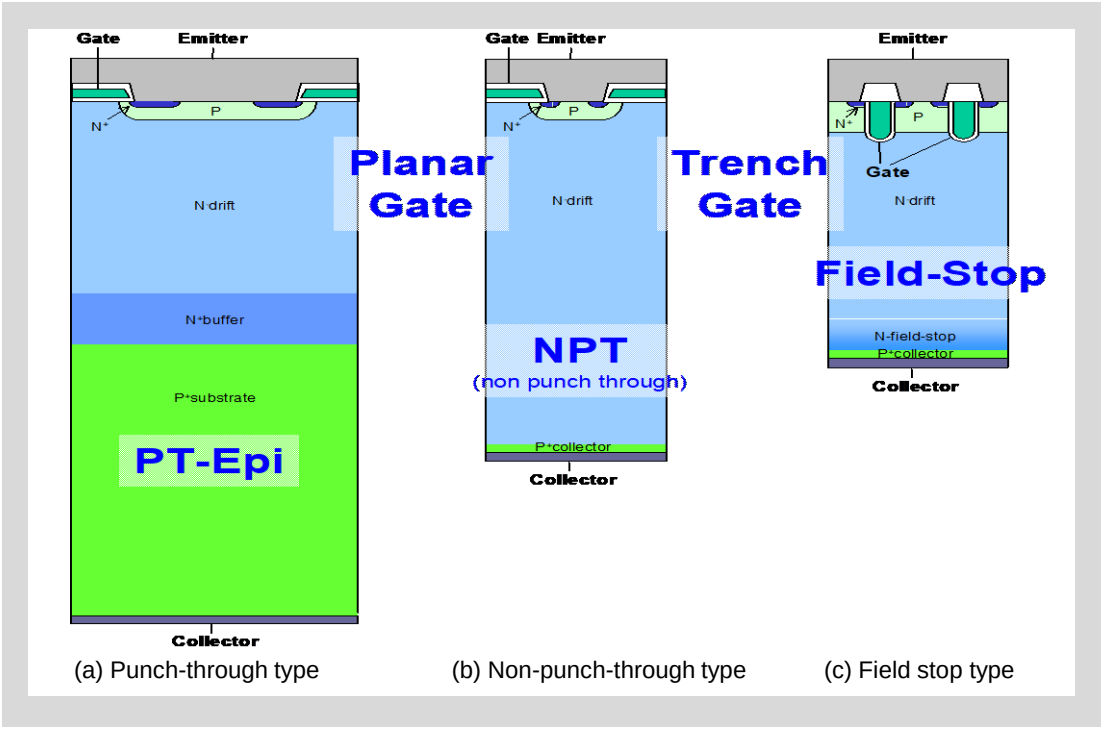
Chapter 1 Product Overview of Fuji Discrete IGBT

This chapter describes the product overview of Fuji discrete IGBT.

1. Transformation and Features of Fuji Discrete IGBT

The IGBT has a structure in which p+ layer is added to the drain side of the MOSFET, and is a device that realizes low resistance at high current by using conductivity modulation of the base layer. In particular, IGBT in which n-type channel is formed when positive voltage is applied to the gate is called n-channel type.

The IGBT structure can be divided roughly into the surface gate structure and the bulk structure that constitutes the base layer. There are two types of surface gate structures. One is the planar gate structure, in which the gates are formed on the wafer surface, namely the chip surface. The other is the trench gate structure, in which the trenches are made to form the gates in the wafer. On the other hand, the bulk structure can be divided roughly into the punch-through type, in which the depletion layer contacts the collector side at turn-off, and the non-punch-through type, in which it does not contact the collector side. Fig.1-1 shows the structural comparison of IGBT.



(a) Punch-through type (b) Non-punch-through type (c) Field stop type

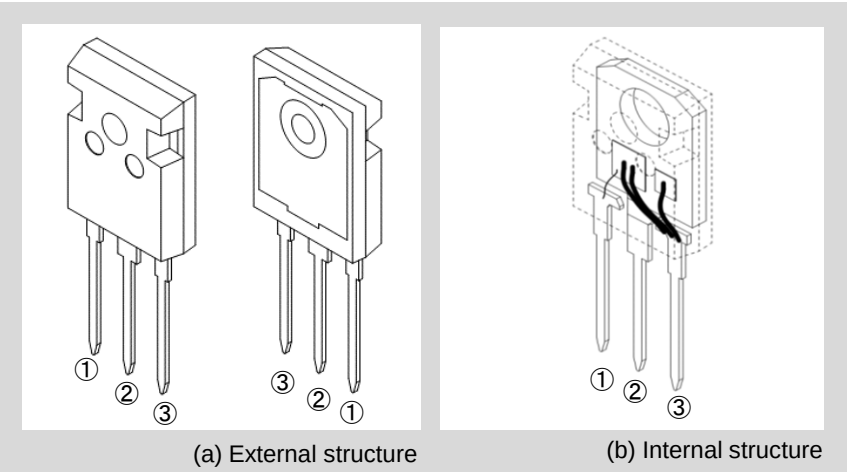
Fig.1-1 Structure comparison of IGBT

Fuji Electric has supplied IGBT to the market since it commercialized them in 1988. The planar-gate punch-through IGBT was the mainstream IGBT at that time. Punch-through type IGBTs at that time used epitaxial wafers, and achieved low on-voltage by injecting carriers from the collector side. At the same time, the lifetime control technology was used because the carriers, which were high-injected into the n-base layer, had to be removed quickly at turn-off. The low on-state voltage and the low turn-off switching loss (E_{off}) were materialized in this way. However, when the lifetime control technology was used, the improvement of characteristics was limited because the high-injected carriers were suppressed by this technology. In addition, the on-state voltage characteristics varied and so the IGBT at that time could not meet the increasing demand for large capacity by using them in parallel.

The non-punch-through IGBT was developed to solve these problems. In this IGBT, the injection efficiency of carriers was suppressed by controlling the impurity concentration in the collector (p+ layer) and the transport efficiency was increased by making the n-base layer thinner. The non-punch-through IGBT used the floating zone (FZ) wafer instead of the epitaxial wafer and so had the advantage that it was less affected by crystal defect. On the other hand, in order to achieve low on-state voltage, it was necessary to improve the transport efficiency and reduce the thickness of the n-base layer. Fuji Electric has developed new technologies for production of thinner wafers and improved the characteristics. In order to further improve the characteristics, IGBT with a thinner chip thickness is required. However, the thickness of the n-base layer constitutes most of the chip thickness. Reducing the thickness will make it impossible to maintain the breakdown voltage. The field stop (FS) structure solved this problem that prevented the improvement of the characteristics. In the FS structure, the high concentration FS layer is provided in the n-base layer, enabling improvement of the characteristics. Fuji Electric has also advanced the miniaturization of surface structure that is imperative to improve the characteristics of IGBT. The IGBT device consists of many arranged structures called cells. The more the IGBT cells are provided, the lower the on-state voltage will be. Therefore, the surface structure has changed from the planar structure, in which the IGBT cells are made planarly on the wafer surface, to the trench structure, in which the trenches are formed on the silicon surface and the gate structure is formed three-dimensionally.

2. Structure of Discrete IGBT

Fig.1-2 shows the discrete product structure of the TO-247-P with built-in IGBT and FWD. Fig.1-2 (a) shows the external structure, and Fig.1-2 (b) shows the internal structure. Terminal ①, ②, and ③ indicates the gate, collector, and emitter terminal, respectively. Unlike IGBT modules, discrete IGBT do not use insulating substrate.

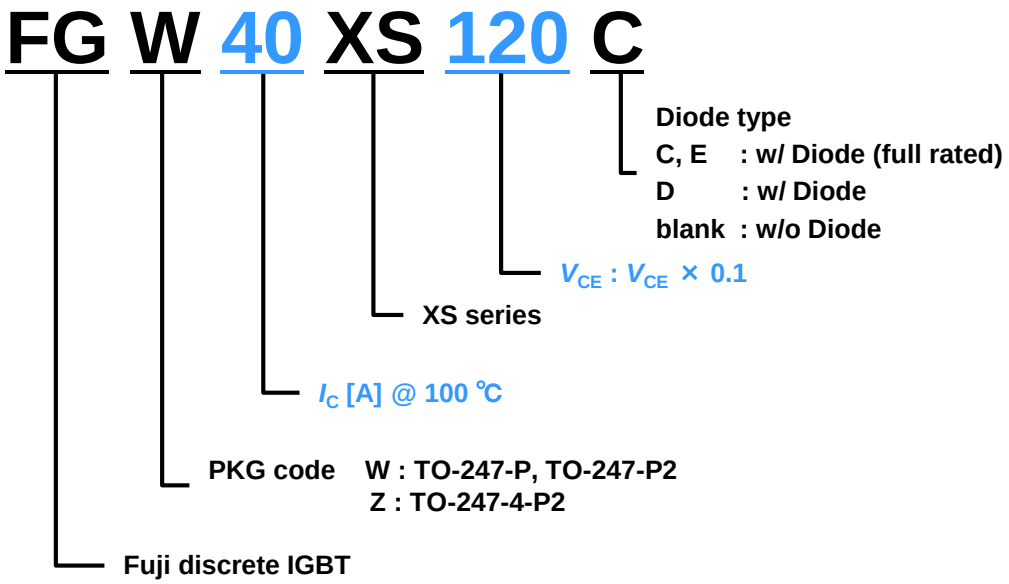


(a) External structure (b) Internal structure

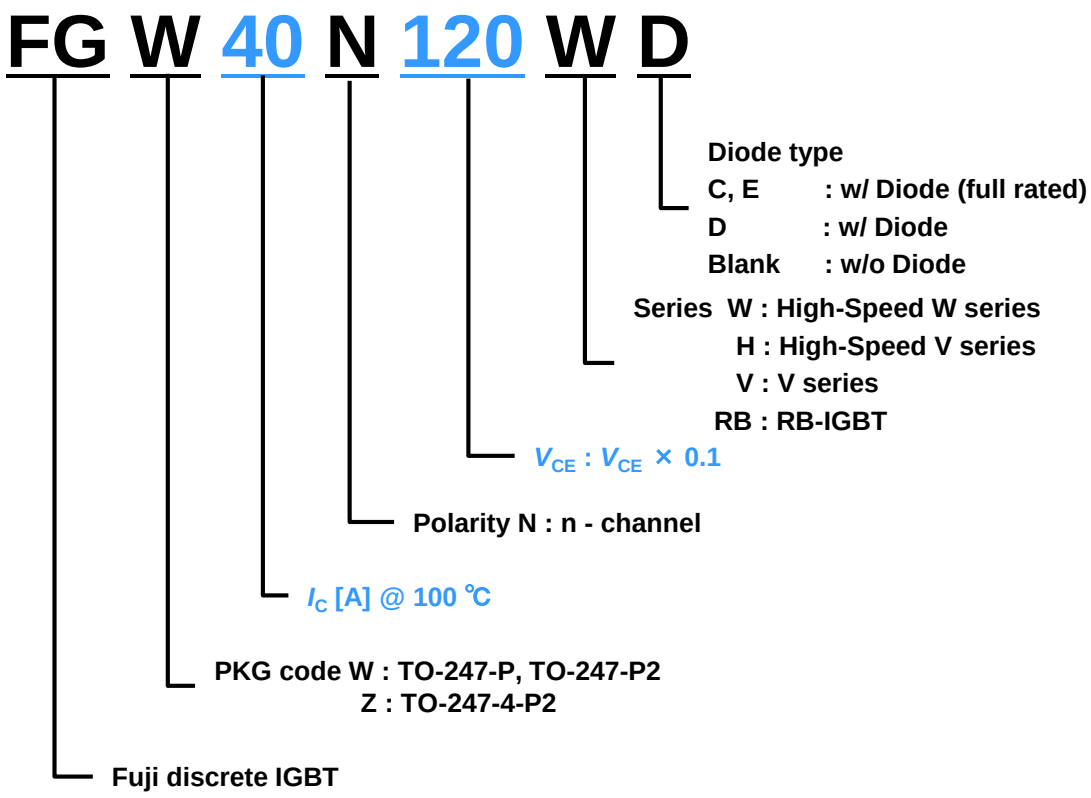
Fig.1-2 Structural diagram of discrete IGBT

3. Code Symbols

FGW40XS120C(example) : XS series



FGW40N120WD (example) : except XS series



4. RoHS Compliance

The Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) was enacted by the EU on July 1, 2006 to restrict the use of certain hazardous substances in electrical and electronic equipment.

The use of the following ten substances are restricted: Pb(lead), Cd(cadmium), Cr6+(hexavalent chromium), Hg(mercury), PBB(polybrominated biphenyl), PBDE(polybrominated diphenyl ether), DEHP(bis(2-ethylhexyl)phthalate), BBP(benzyl butyl phthalate), DBP(dibutyl phthalate) and DIBP(diisobutyl phthalate).

Products containing these 10 substances above the threshold (0.01% for Cd, 0.1% for others) cannot be sold in the EU, but exemptions are granted for applications that are technically difficult to replace.

Our discrete IGBT products are RoHS compliant. Lead-free solder (Pb less than 0.1%) is used for the dip solder of the terminal part.

Chapter 2 Terms and Characteristics

This chapter describes the terms and characteristics.

1. Explanation of Terms

This section describes the terms used in specifications.

Table.2-1 Absolute maximum rating

Term	Symbol	Definition explanation (See specifications for test conditions)
Collector-Emitter Voltage	V_{CES}	Max. Collector-Emitter (hereinafter referred to as C-E) voltage with Gate-Emitter (G-E) shorted
Gate-Emitter Voltage	V_{GES}	Max. G-E voltage with C-E shorted (Normally ±20V max.)
Collector Current	I_C	Max. DC collector current
	I_{CP}	Max. pulse collector current
Diode Forward Current	I_F	Max. DC FWD current
	I_{FP}	Max. pulse FWD current
Short Circuit Withstand Time	t_{SC}	The time interval which the device can withstand in short circuit condition without failing
Collector Power Dissipation	P_{D_IGBT}	Max. power dissipation of IGBT
FWD Power Dissipation	P_{D_FWD}	Max. power dissipation of FWD
Operating Junction Temperature	T_{vj}	Junction temperature range during continuous operation
Storage Temperature	T_{stg}	Temperature range allowing storage or transportation without being subjected to electrical load

Table.2-2 Electrical characteristics

Term	Symbol	Definition explanation (See specifications for test conditions)
Zero Gate Voltage Collector Current	I_{CES}	Leakage current when a specified voltage is applied to C-E with G-E shorted
Gate-Emitter Leakage Current	I_{GES}	Leakage current when a specified voltage is applied to G-E with C-E shorted
Gate-Emitter Threshold Voltage	$V_{GE(th)}$	G-E voltage (hereinafter, V_{GE}) at specified C-E (hereinafter, I_C) current and C-E voltage (hereinafter, V_{CE}). (It is used as a measure of V_{GE} value at which I_C begins to flow, and V_{GE} at which the IGBT begins to turn-on.)
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	V_{CE} at a specified I_C and V_{GE}
Input Capacitance	C_{ies}	G-E capacitance, when a specified V_{GE} and V_{CE} are applied with C-E shorted in AC
Output Capacitance	C_{oes}	C-E capacitance, when a specified V_{GE} and V_{CE} are applied with G-E shorted in AC
Reverse Transfer Capacitance	C_{res}	C-G capacitance, when a specified V_{GE} and V_{CE} are applied with G-E and C-E shorted in AC
Gate Charge	Q_G	Amount of G-E charge to turn-on IGBT
Turn-On Delay Time	$t_{d(on)}$	Time from when V_{GE} reaches 10% of the max. value until I_C reaches 10% of the max. value at IGBT turn-on (See Fig.2-4)
Rise Time	t_r	Time from when I_C rises to 10% of the max. value to 90% of the max. value at IGBT turn-on (See Fig.2-4)
Turn-Off Delay Time	$t_{d(off)}$	Time from when V_{GE} reaches 90% of its max. value until I_C reaches 90% of the max. value at IGBT turn-off (See Fig.2-4)
Fall Time	t_f	Time from when I_C falls from 90% of its max. value to 10% of the max. value at IGBT turn-off (See Fig.2-4)
Turn-on Energy	E_{on}	Loss that occurs during IGBT turn-on (See Fig.2-4)
Turn-off Energy	E_{off}	Loss that occurs during IGBT turn-off (See Fig.2-4)
Reverse Recovery Energy	E_{rr}	Loss that occurs during FWD reverse recovery (See Fig.2-4)
Forward Voltage Drop	V_F	Forward voltage when a specified forward current is applied to FWD
Diode Reverse Recovery Time	t_{rr}	Time from when the current crosses 0A to 10% of the reverse recovery peak current at FWD turn-off (See Fig.2-4)
Diode Reverse Recovery Charge	Q_{rr}	Amount of charge required for reverse recovery current in FWD to disappear
Reverse Biased Safe Operating Area	RBSOA	Region of current and voltage where the IGBT can be safely turned-off under specified conditions
Thermal Resistance, Junction-Ambient	$R_{th(j-a)}$	Thermal resistance between chip and surroundings without heat sink and without wind
Thermal Resistance, IGBT Junction to Case	$R_{th(j-c)\_IGBT}$	Thermal resistance between the IGBT chip and case
Thermal Resistance, FWD Junction to Case	$R_{th(j-c)\_FWD}$	Thermal resistance between the FWD chip and case

2. Characteristics of IGBT and FWD

Discrete IGBT products include products in which a FWD is connected in anti-parallel to the IGBT, and products with only IGBT. Taking FGW40XS120C (1200V / 40A device) as an example, the explanation of various characteristics of IGBT and FWD described in the specifications etc. are shown below.

＜Output Characteristics＞

This characteristic shows the relationship between the drop voltage (V_{CE}) and the current (I_C) when the IGBT is in on-state, which is the loss that occurs in the IGBT. The lower the V_{CE}, the smaller the loss. Please note that these characteristics change depending on T_{vj} and V_{GE}. Generally, the output characteristic of V_{GE} = 15V is used.

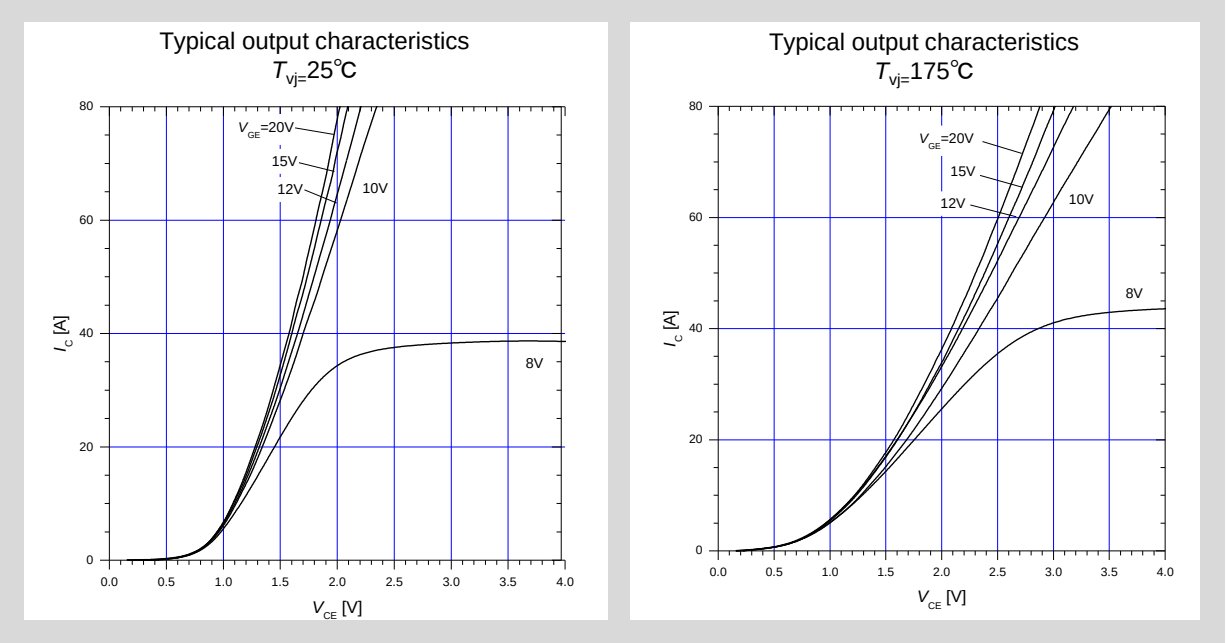


Fig.2-1 Characteristics of $V_{CE(sat)}$ - I_C

Fig.2-2 shows V_F-I_F characteristics of FWD. This characteristic changes depending on T_{vj}.

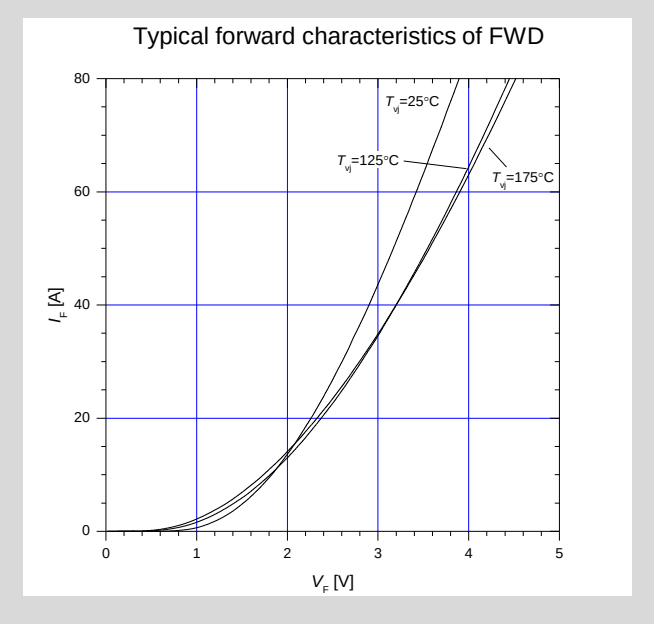


Fig.2-2 Characteristics of V_F-I_F

＜Switching Characteristics＞

Switching characteristics can be broadly divided into switching time and switching loss. The switching characteristics can be measured with the chopper circuit shown in Fig.2-3.

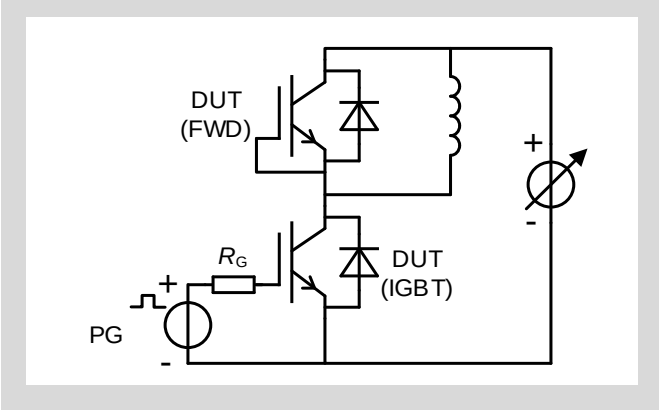
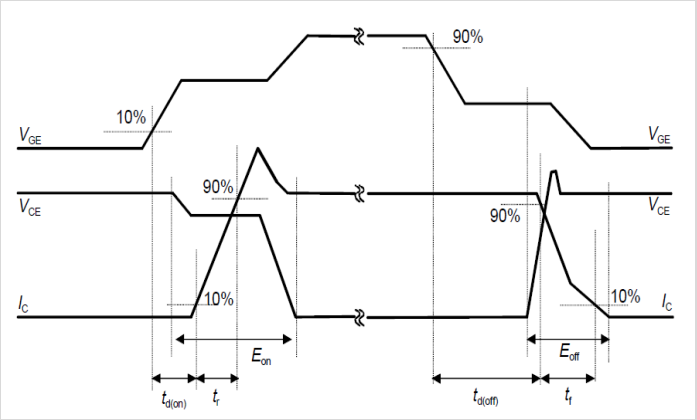
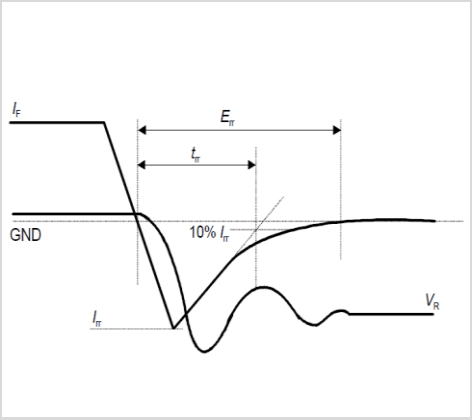


Fig.2-3 Switching characteristic measurement circuit

Fig.2-4 shows the definitions of switching time ($t_{d(on)}$, t_r, $t_{d(off)}$, t_f, t_{rr}) and switching loss (E_{on}, E_{off}, E_{rr}) shown in Table 2-2.



(a) Waveforms of turn-on and turn-off



(b) Reverse recovery waveforms

Fig.2-4 Definition of switching time

The relationship between switching time and I_C is shown in Fig.2-5, and the relationship between switching time and R_G is shown in Fig.2-6. Please note that the switching time varies depending on I_C, T_{vj} and R_G.

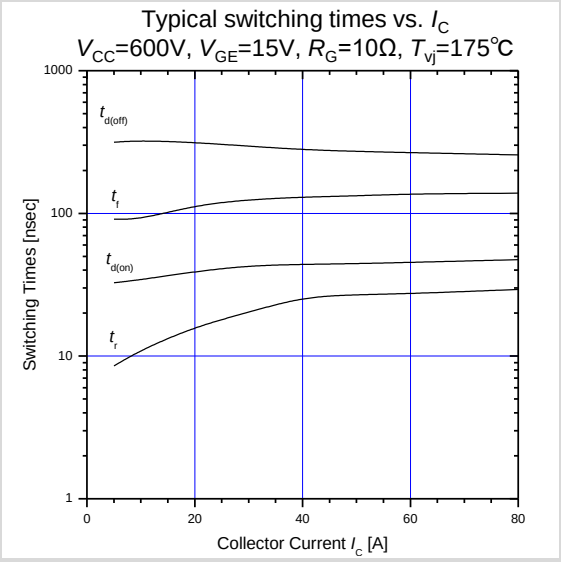


Fig.2-5 Characteristics of switching time-I_C

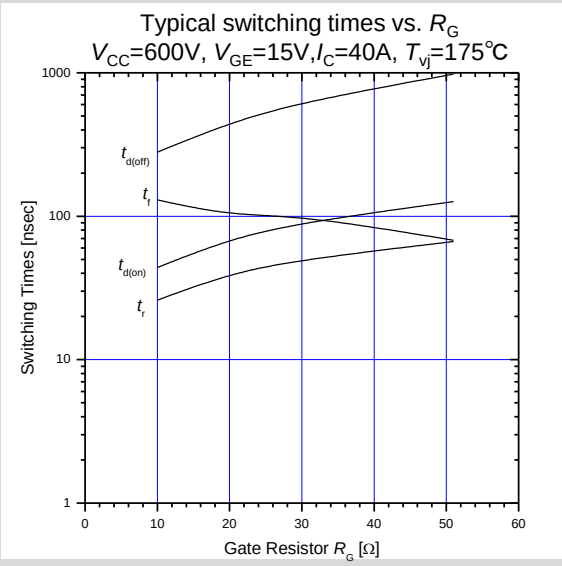


Fig.2-6 Characteristics of switching time-R_G

Fig.2-7 shows the relationship between the reverse recovery time of FWD and I_F. The reverse recovery time varies depending on I_F, T_{vj}, and R_G.

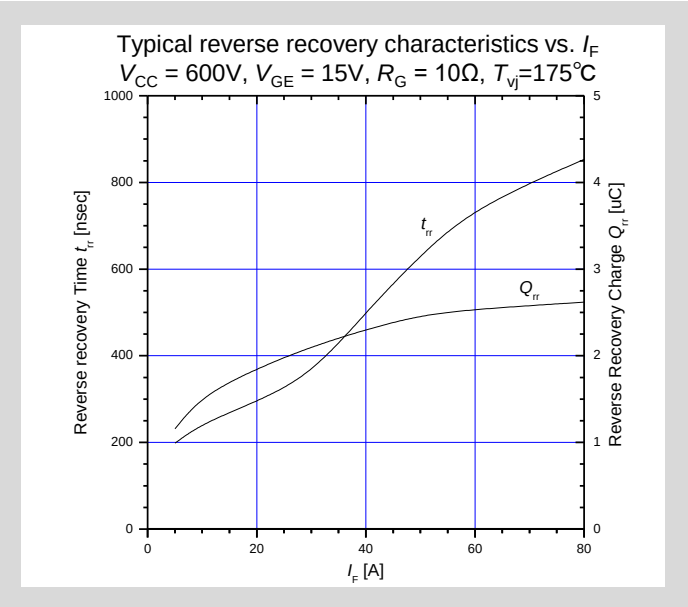


Fig.2-7 Characteristics of t_{rr}-I_F

Switching loss (E_{on}, E_{off}, E_{rr}) occurs when the IGBT switches (turn-on, turn-off). Fig.2-8 shows the relationship between E_{on}, E_{off} and I_C, and Fig.2-9 shows the relationship between E_{on}, E_{off} and R_G. The relationship between E_{rr} and I_F is shown in Fig.2-10. Please note that this characteristic varies depending on T_{vj}, V_{GE}, I_C, I_F, and R_G.

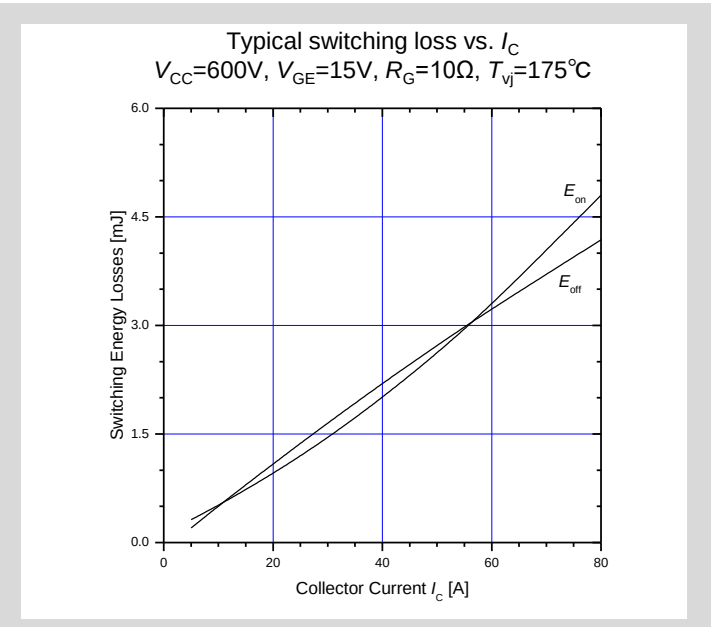


Fig.2-8 Characteristics of E_{on}, E_{off}-I_C

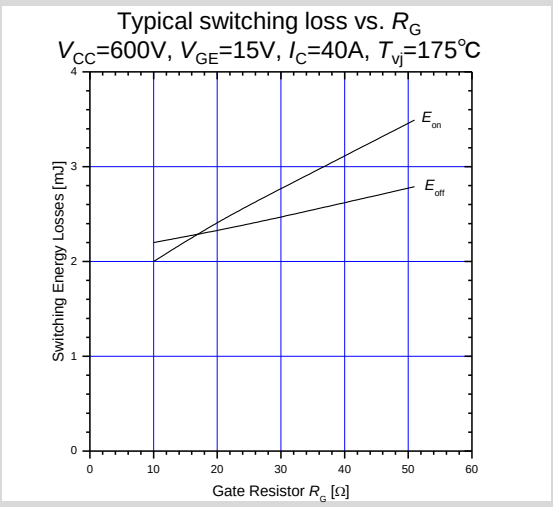


Fig.2-9 Characteristics of E_{on}, E_{off}-R_G

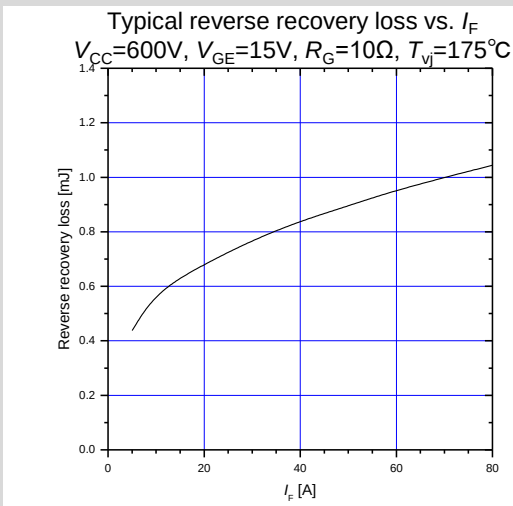


Fig.2-10 Characteristics of E_{rr}-I_F

＜Capacitance characteristics＞

The IGBT has parasitic capacitance due to its structure. The Parasitic capacitance includes C_{ies}, C_{oes}, and C_{res}. The relationship between V_{GE} and Q_G is shown in Fig.2-11, and the relationship between C_{ies}, C_{oes}, C_{res} and V_{CE} is shown in Fig.2-12.

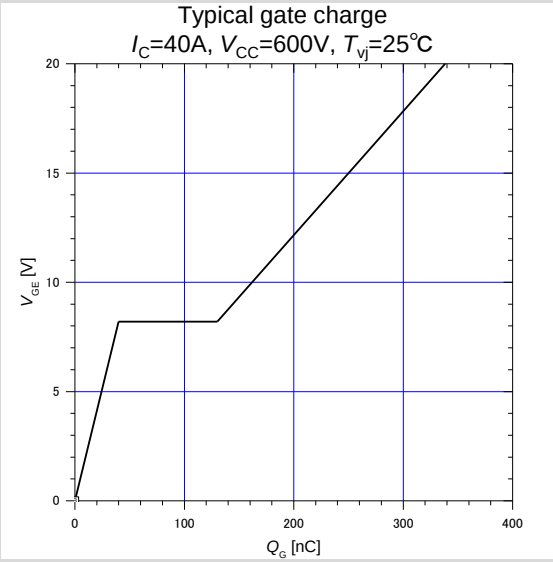


Fig.2-11 Characteristics of V_{GE}-Q_G

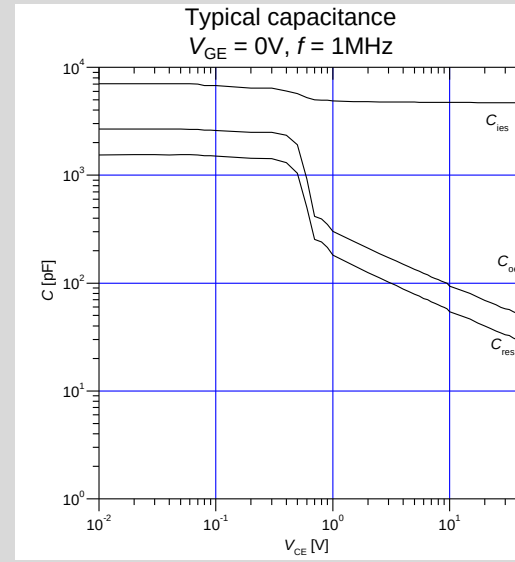


Fig.2-12 Characteristics of C_{ies}, C_{oes}, C_{res}-V_{CE}

＜Reverse Biased Safe Operating Area (RBSOA)＞

Fig.2-13 shows the region of V_{CE}-I_C (RBSOA) where the IGBT can safely turn-off under specified conditions.

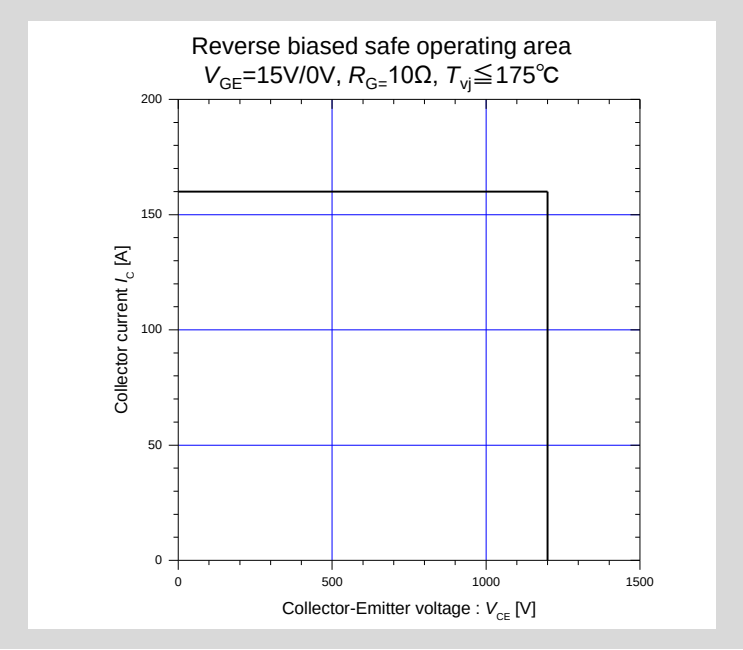
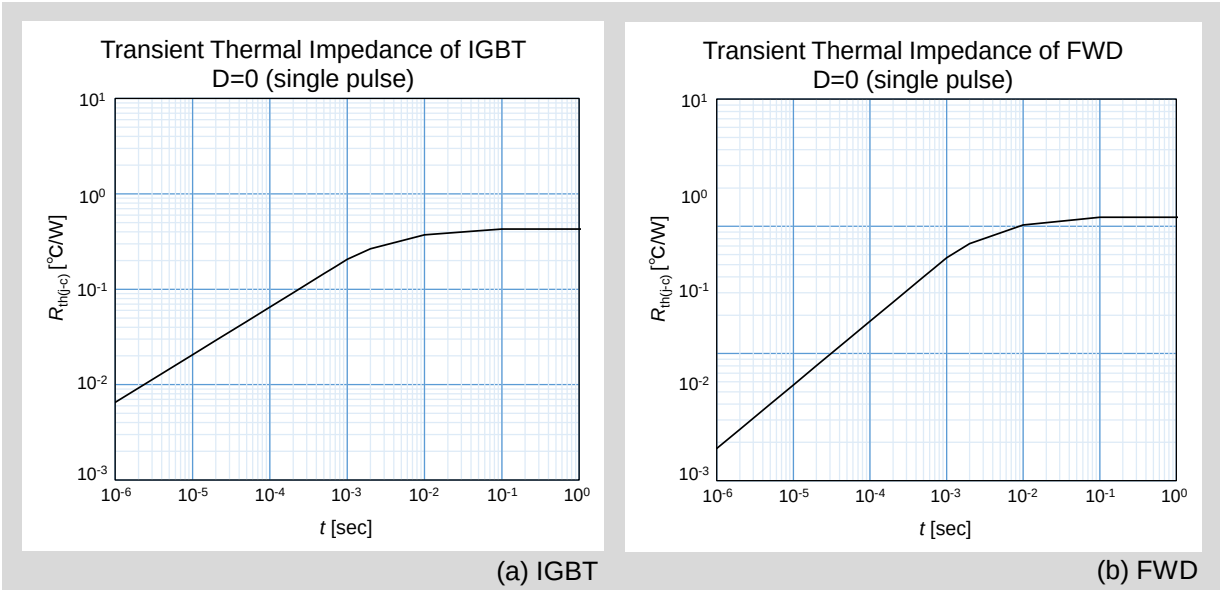


Fig.2-13 Reverse Biased Safe Operating Area (RBSOA)

＜Transient thermal resistance characteristics＞

Fig.2-14 show the transient thermal resistance characteristics. The thermal resistance value is the value obtained by dividing the temperature change that occurs by the applied power when a single constant power pulse is applied to the product. The value of thermal resistance expressed in pulse time is the transient thermal resistance characteristic.



(a) IGBT (b) FWD

Fig.2-14 Characteristics of transient thermal resistance characteristics

Chapter 3 Overvoltage Protection (Main Circuit)

Overvoltage is applied to IGBT and FWD when the current is cut off, and the overvoltage may destroy the device. This chapter describes the overvoltage protection (main circuit).

1. Overvoltage Causes and Suppression Method

Fig.3-1 shows the inverter circuit for one phase. The overvoltage is generated at the wiring inductance L_S of the main circuit due to a sudden change in the main circuit current when the IGBT is turned-off. Fig.3-2 shows a typical IGBT1 turn-off waveform and FWD2 reverse recovery waveform. If this overvoltage exceeds V_{CES}, the IGBT and FWD might be destroyed.

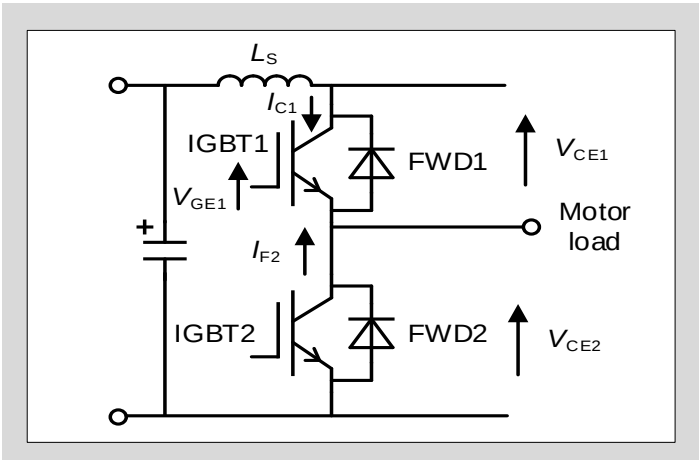
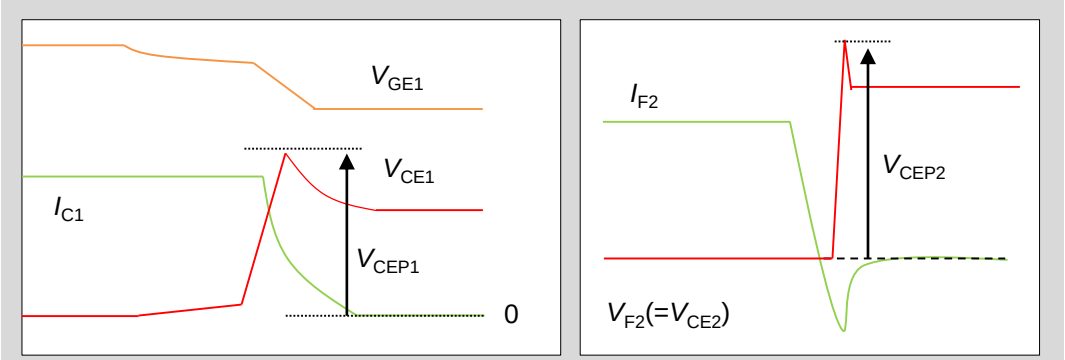


Fig.3-1 Inverter circuit for one phase



(a) IGBT1 turn-off waveform (b) FWD reverse recovery waveform

Fig. 3-2 Switching waveforms

＜Overvoltage suppression methods＞

The methods for suppressing the overvoltage are shown below.

(a) Snubber circuit placement

Place the snubber circuit close to the terminals to reduce the effect of wiring inductance.

(b) Adjustment of reverse biased voltage ($-V_{GE}$) and gate resistance (R_G) of IGBT drive circuit

By reducing $-V_{GE}$ and increasing R_G, di/dt at the time of turn-off can be reduced and overvoltage can be suppressed. (See Chapter 4, Drive Circuit Design for details)

(c) Shortening the distance between the electrolytic capacitor and the IGBT

Place the electrolytic capacitor as close as possible to the IGBT in order to reduce the wiring inductance. It is even more effective to use a capacitor with low impedance.

(d) Adjustment of main circuit

To reduce the inductance, use thicker and shorter wires. It is also very effective to use laminated copper bars .

(e) Application of active clamp circuit

By applying an active clamp circuit to the gate drive circuit, it is possible to suppress the overvoltage to approximately equal to the Zener Voltage of the Zener diode.

2. Types of Snubber Circuits and Their Features

Individual snubber circuits are connected to each IGBT, while lump snubber circuits are connected between the DC power-supply bus and the ground for centralized protection.

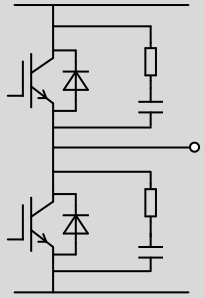
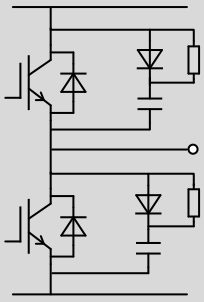
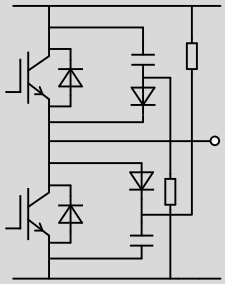
＜Individual snubber circuits＞

Examples of typical individual snubber circuits are listed below.

(a) RC snubber circuit (b) Charge and discharge RCD snubber circuit

(c) Discharge-suppressing RCD snubber circuit

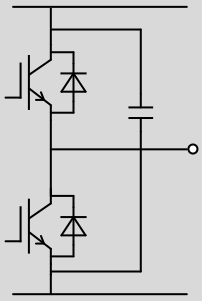
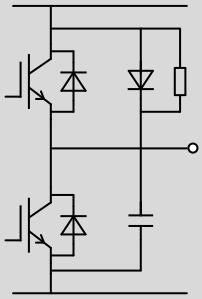
Table.3-1 Individual snubber circuits

Snubber circuit schematic	Circuit features (comments)
(a) RC snubber circuit 	・This circuit has greater overvoltage suppression effect than the lump snubber circuit. ・When applied to large capacity IGBT, the snubber resistance must be low. Consequently however, the above condition causes the load conditions at turn-on to become more severe.
(b) Charge and discharge RCD snubber circuit 	・This circuit has overvoltage suppression effect. ・As opposed to the RC snubber circuit, a snubber diode has been added. This allows the snubber resistance to increase and consequently avoids the IGBT load conditions at turn-on problem. ・The power dissipation loss caused by the snubber resistance can be calculated as follows: $P = \frac{L \cdot I_o^2 \cdot f}{2} + \frac{C_s \cdot E_d^2 \cdot f}{2}$ L : Wiring inductance of main circuit I_o : I_C at IGBT turn-off C_s : Capacitance of snubber capacitor E_d : DC supply voltage f : Switching frequency
(c) Discharge suppressing RCD snubber circuit 	・This circuit has overvoltage suppression effect. ・Snubber circuit power dissipation is small. ・The power dissipation loss caused by the snubber resistance can be calculated as follows: $P = \frac{L \cdot I_o^2 \cdot f}{2}$ L : Wiring inductance of main circuit I_o : I_C at IGBT turn-off f : Switching frequency

＜Lump snubber circuits＞

Examples of typical snubber circuits are listed below.
(a) C snubber circuit (b) RCD snubber circuit

Fig.3-2 Lump snubber circuits

Snubber circuit schematic	Circuit features (comments)
(a) C snubber circuit 	・This is the simplest circuit. ・The LC resonance circuit, which consists of main circuit inductance and snubber capacitance, may cause the voltage to oscillate.
(b) RCD snubber circuit 	・ If the wrong snubber diode is used, high overvoltage will be generated and the output voltage will oscillate during reverse recovery.

3. Discharge-suppressing RCD Snubber Circuit Design

This section describes the basic design method of the discharge-suppressing RCD snubber circuit.

＜Study of applicability＞

Fig.3-3 shows the turn-off locus waveform of IGBT in a discharge-suppressing RCD snubber circuit. Fig.3-4 shows the I_C and V_{GE} waveforms at turn-off. This circuit is activated when V_{CE} starts to exceed the DC supply voltage. The dotted line in Fig. 3-3 shows the ideal operating locus of the IGBT. In an actual application, the wiring inductance of the snubber circuit or a transient forward voltage drop in the snubber diode can cause overvoltage at IGBT turn-off. This overvoltage causes the sharp-cornered locus indicated by the solid line in Fig.3-3. This snubber circuit applicability is decided by whether or not the IGBT operating locus is within the RBSOA at turn-off.

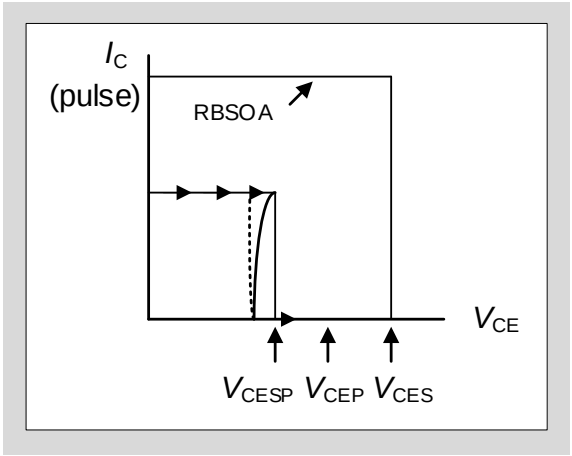


Fig.3-3 Turn-off locus waveform of IGBT

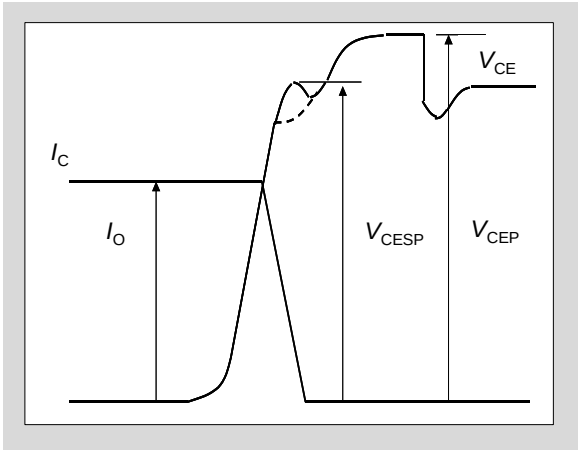


Fig.3-4 Voltage and current waveforms at turn-off

The overvoltage at IGBT turn-off is calculated as follows:

$$V_{CESP} = E_d + V_{FM} + \left(-L_S \frac{di_c}{dt}\right) \quad \cdots\cdots\cdots\cdots\cdots\cdots ①$$

E_d : DC supply voltage
V_{FM} : Transient forward voltage drop in snubber diode
L_S : Snubber circuit wiring inductance
di_c/dt : Max. I_C change rate IGBT turn-off

The reference values for the transient forward voltage drop in snubber diodes is as follows:
600V class: 20 to 30V, 1200V class: 40 to 60V

＜Calculating the capacitance of the snubber capacitor (*Cs*)＞

The necessary capacitance of a snubber capacitor is calculated as follows:

$$C_S = \frac{L \cdot I_O^2}{(V_{CEP} - E_d)^2} \quad \cdots\cdots\cdots\cdots\cdots\cdots ②$$

L : Main circuit wiring inductance
I_O : I_C at IGBT turn-off
V_{CEP} : Snubber capacitor peak voltage
E_d : DC supply voltage

V_{CEP} must be limited to less than or equal to the IGBT C-E withstand voltage. Also, select a snubber capacitor with good high-frequency characteristics (film capacitor, etc.).

＜Calculating snubber resistance (R_s)＞

The snubber resistance is required to discharge the electric charge accumulated in the snubber capacitor before the next IGBT turn-off. To discharge 90% of the accumulated energy by the next IGBT turn-off, the snubber resistance must be as follows:

$$R_S \leq \frac{1}{2.3 \cdot C_S \cdot f} \quad \cdots\cdots\cdots\cdots\cdots\cdots ③$$

R_S : Snubber resistance
C_S : Snubber capacitor
f : Switching frequency

If the snubber resistance is set too low, the snubber circuit current will oscillate and the peak I_C at the IGBT turn-off will increase. Therefore, set the snubber resistance in a range below the value calculated in equation ③.

Irrespective of the resistance value, the snubber resistance loss P(R_s) can be calculated as follows:

$$P\,(R_S) = \frac{L \cdot I_O^2 \cdot f}{2} \quad \cdots\cdots\cdots\cdots\cdots\cdots ④$$

$P_{(R_s)}$: Loss of snubber resistance
L : Main circuit wiring inductance
I_O : I_C at IGBT turn-off
f : Switching frequency

＜Snubber diode selection＞

Transient forward voltage drop in the snubber diode is one factor that can cause overvoltage. If the reverse recovery time of the snubber diode is too long, then the power dissipation loss will also be much greater during high frequency switching. If the snubber diode's reverse recovery is too fast, then the IGBT C-E voltage will increase drastically and oscillate. Select a snubber diode that has a low transient forward voltage, short reverse recovery time and a soft recovery.

＜Snubber circuit wiring precautions＞

The snubber circuit's wiring inductance is one of the main causes of overvoltage, therefore it is important to design the circuit with the lowest inductance possible.

4. Active Clamp Circuit

Other than the reduction of main circuit inductance and application of snubber circuit, applying an active clamp circuit to the gate drive circuit (GDU) is an effective method of suppressing overvoltage. Fig.3-5 shows the example of active clamp circuits. In the circuit, a zener diode and a diode connected in anti-series are added in between C-G. If a voltage exceeding the breakdown voltage of the zener diode is applied to C-G, the zener diode breakdown, and the IGBT will be turned-off with C-G voltage equal to the breakdown voltage of the zener diode. Fig.3-6 shows an example of the waveform when the active clamp circuit is applied. I_C rate of change di_C/dt at turn-off is slower than before the active clamp circuit was applied, thus the turn-off time is longer. Since the application of the active clamp circuit causes an increase in loss, it is recommended to perform various design verifications.

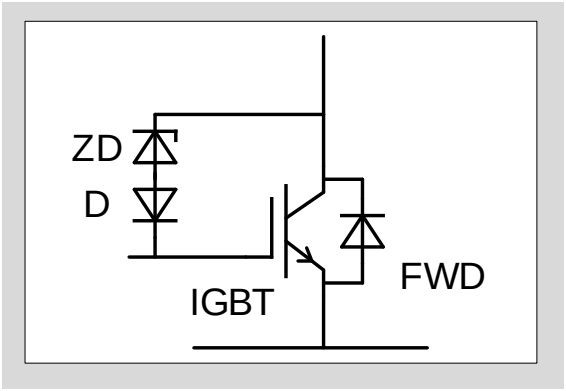


Fig.3-5 Active clamp circuit

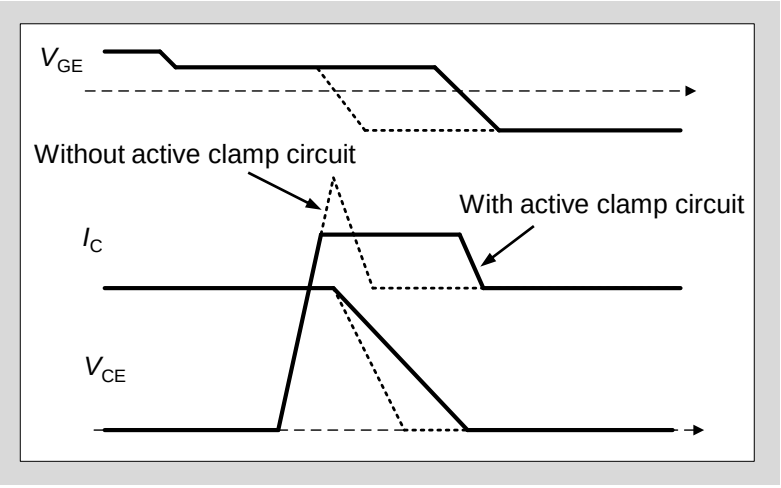


Fig.3-6 Schematic waveform for active clamp circuit

Chapter 4 Drive Circuit Design

This chapter describes the drive circuit design. The drive circuit consists of a forward bias circuit that turns on the IGBT and a reverse bias circuit that keeps the IGBT off stably. The main characteristics of the IGBT, such as switching operation, change according to the value of V_{GE} and R_G. Table.4-1 shows the general relationship between IGBT drive conditions and the main characteristics. Since the main characteristics of the IGBT change depending on V_{GE}, R_G, etc., it is necessary to set them according to the design goal of the device.

Table.4-1 IGBT drive conditions and main characteristics

Main characteristic	$+V_{GE}$ increase	$-V_{GE}$ increase	$R_{G(on)}$ increase	$R_{G(off)}$ increase
$V_{CE(sat)}$	↓	–	–	–
t_{on} E_{on}	↓	–	↑	–
t_{off} E_{off}	–	↓	–	↑
Turn-on FWD overvoltage	↑	–	↓	–
Turn-off IGBT overvoltage	–	↑	–	↓ *1
d*v*/d*t* shoot through	↑	↓	↓	↓
Saturation current value	↑	–	–	–
Short circuit withstand capability	↓	–	↑	↓
Radiation noise	↑	–	↓	↓

*1 Dependence of overvoltage on R_G is different for each series

1. Forward Bias Gate Voltage $+V_{GE}$ (On-State)

The recommended gate voltage value ($+V_{GE}$) is +15V. Notes when designing $+V_{GE}$ are shown as follows.

(1) Design the $+V_{GE}$ below the max. rated voltage of ±20V.
(2) It is recommended that supply voltage fluctuation is kept to within ±10%.
(3) The on-state $V_{CE(sat)}$ is dependent on the $+V_{GE}$, so the higher the $+V_{GE}$, the lower $V_{CE(sat)}$.
(4) The higher the $+V_{GE}$, the smaller the turn-on switching time and switching loss.
(5) At turn-on (at FWD reverse recovery), the higher the $+V_{GE}$, the greater the likelihood of overvoltage in opposing arms.
(6) Even while the IGBT is in off-state, there may be malfunctions caused by the d*v*/d*t* of the FWD's reverse recovery and a pulse I_C may cause unnecessary heat generation. This phenomenon is called a d*v*/d*t* shoot through and becomes more likely to occur as the $+V_{GE}$ increases.
(7) Generally, the higher the $+V_{GE}$, the higher the saturation current becomes.
(8) The higher the $+V_{GE}$, the shorter the short circuit withstand capability.

2. Reverse Bias Gate Voltage -V_{GE} (Off-State)

One way to prevent dv/dt shoot through is to apply -V_{GE}. Notes when designing -V_{GE} are shown as follows.

(1) Design the -V_{GE} below the max. rated voltage of ±20V.

(2) It is recommended that supply voltage fluctuations are kept to within ±10%.

(3) IGBT turn-off characteristics are heavily dependent on -V_{GE}, especially when I_C is just beginning to switch off.

3. R_G (Gate Resistance)

Gate resistance R_G needs to be adjusted appropriately depending on the circuit configuration and environment. Notes when designing R_G are shown as follows.

(1) The switching characteristics of both turn-on and turn-off are dependent on the value of R_G, and therefore the larger the R_G, the longer the switching time and the larger the switching loss. Also, as R_G increases, the overvoltage during switching becomes smaller.

(2) The larger the R_G, the more unlikely dv/dt shoot through will occur.

(3) Switching characteristics vary greatly depending on the parasitic inductance. In particular overvoltage generated during IGBT turn-off and during FWD reverse recovery are greatly affected. Therefore, R_G needs to be designed with low parasitic inductance.

4. Drive Current

Since the IGBT has a MOSFET gate structure, gate current (drive current) is needed to charge and discharge this gate during switching. Fig.4-1 shows the gate charge (dynamic input) characteristics. The gate charge is the amount of charge required to drive the IGBT and is used to calculate the average drive current and power.

Fig.4-2 shows an example of the drive circuit and the gate voltage / current waveform. The principle of the drive circuit is to switch the forward bias power supply and the reverse bias power supply alternately with switches S1 and S2. The current that charges and discharges the gate during this switching is the drive current, and the area (shaded area) represented by the gate current waveform in Fig. 4-2 is equal to the amount of charge in Fig. 4-1.

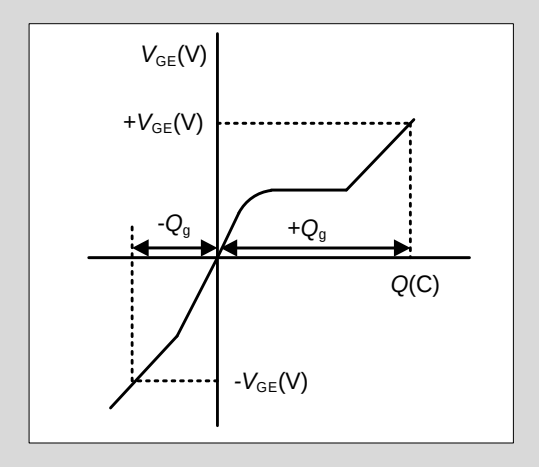


Fig.4-1 Gate charge characteristic (Dynamic input characteristics)

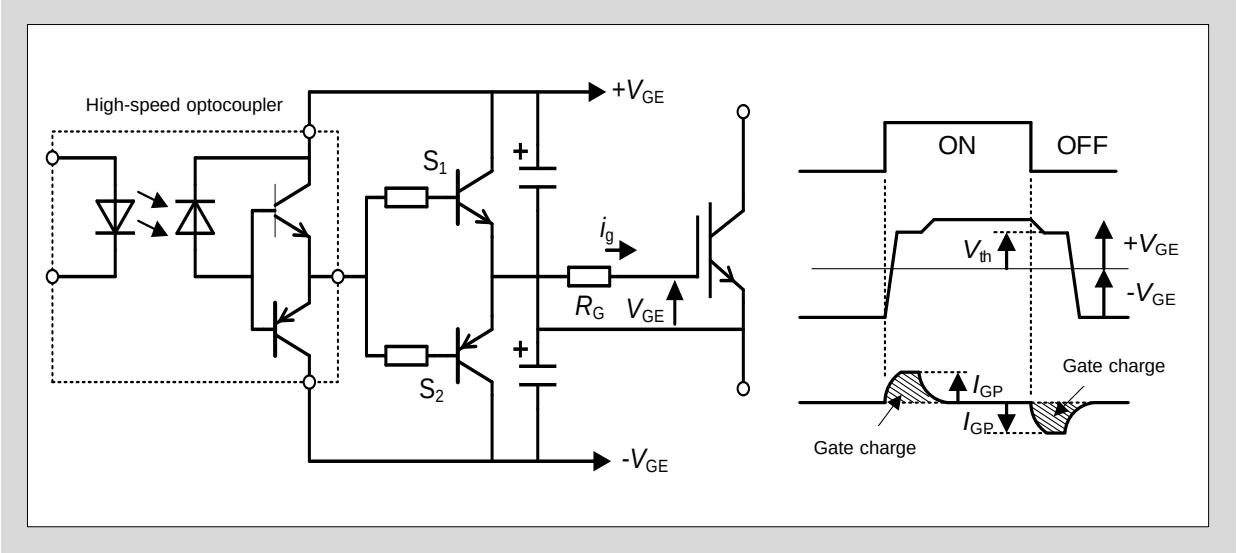


Fig.4-2 Drive circuit schematic and voltage / current waveforms

The drive current peak value I_{GP} can be approximately calculated as follows:

$$I_{GP} = \frac{|+V_{GE}|+|-V_{GE}|}{R_G}$$

$+V_{GE}$: Forward bias supply voltage
$-V_{GE}$: Reverse bias supply voltage
R_G : Drive circuit gate resistance

The average value of the drive current I_G, using the gate charge characteristics (Fig.4-1), can be calculated as follows:

$$+I_G = -I_G = f_c \cdot (|+Q_g| + |-Q_g|)$$

f_C : Carrier frequency
$+Q_g$: Gate charge from 0V to $+V_{GE}$
$-Q_g$: Gate charge from $-V_{GE}$ to 0V

It is important to design the output stage of the drive circuit in consideration of this approximate current (I_{GP} and $\pm I_G$). Furthermore, if the power dissipation loss of the drive circuit is completely consumed by the gate resistance, then the drive power (P_d) necessary to drive the IGBT is shown in the following formula:

$$P_{d(on)} = P_{d(off)} = f_C \cdot \left[\frac{1}{2}(|+Q_g|+|-Q_g|) \cdot (|+V_{GE}|+|-V_{GE}|)\right]$$

$$P_d = P_{d(on)} + P_{d(off)} = f_C \cdot (|+Q_g|+|-Q_g|) \cdot (|+V_{GE}|+|-V_{GE}|)$$

It is necessary to select gate resistance that can tolerate the loss generated by this approximation formula.

5. Setting Dead Time

In inverter circuits, etc., dead time is set for on / off switching timing to prevent short circuits between the upper and lower arms. As shown in Fig.4-3, both the upper and lower arms are in the "off" state during the dead time. Basically, the dead time needs to be set longer than the max. value of the IGBT switching time ($t_{d(off)}+t_f$). If the dead time is short, short circuit may occur between the upper and lower arms, and the heat generated by the short circuit current may destroy the device.

Also, increasing R_G will increase the switching time, so it is necessary to increase the dead time. In addition, it is necessary to consider other drive conditions, device variations, temperature characteristics, etc..

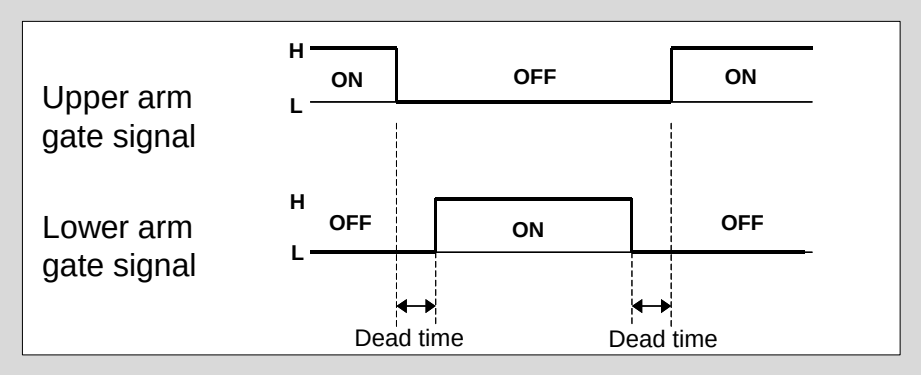


Fig.4-3 Dead time timing chart

Whether the dead time setting is sufficient is judged by checking the current of the DC supply line when there is no load. In the case of 3-phase inverter (as shown in Fig.4-4), set the inverter's outputs to no load, then apply normal input signal, and finally measures the DC line current. Very small pulse current (d*v*/d*t* current through the IGBT's miller capacitance: about 5% of the normal rated current) will be observed, even if the dead time is long enough. However, if the dead time is insufficient, then there will be a much larger short circuit current. In this case, keep increasing the dead time until the short circuit current disappears. It is recommended to perform this test at high temperature because the higher the temperature, the longer the turn-off time. Also, if $-V_{GE}$ is insufficient, the short circuit current will increase due to d*v*/d*t* shoot through. If the short circuit current does not decrease even if the dead time increases, increase $-V_{GE}$.

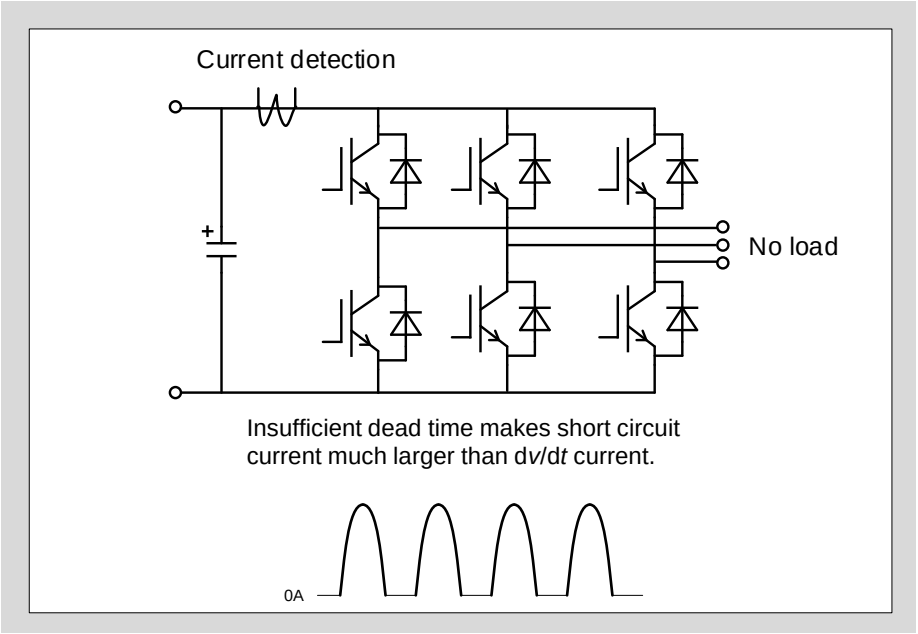


Fig.4-4 How to detect short circuit current due to insufficient dead time

6. Example of Drive Circuits

Fig.4-5 shows an example of a drive circuit using high-speed optocoupler. By using optocoupler, the input signal and the IGBT are isolated from each other. Also, since the optocoupler does not limit the output pulse width, it is suitable for applications where the pulse width change over a wide range, such as PWM controller, and is currently the most widely used. Furthermore, the turn-on and turn-off characteristics determined by gate resistance can be set separately, so it is commonly used to ensure the best settings.

In addition, there is a drive method that uses a pulse transformer for signal isolation. This method simplifies the circuit because both the signal as well as the gate drive power can be supplied simultaneously from the signal side. However, this method has the limitations of on / (off+on) time ratio of max. 50%, and reverse bias cannot be set, so it's usefulness as a control method and switching frequency regulator is limited.

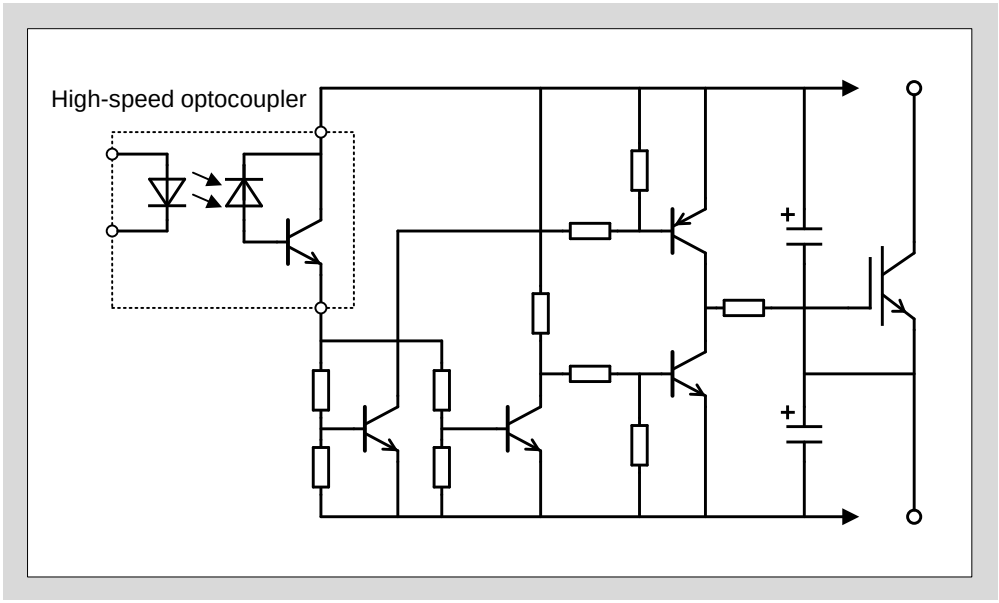


Fig.4-5 Example of drive circuit using high-speed optocoupler

7. Precautions for Drive Circuit Design and Mounting

＜Optocoupler noise tolerance＞

IGBT is a high-speed switching device, thus it is necessary to select optocoupler that has high noise tolerance for the drive circuit. Also, to prevent malfunctions, make sure that the wiring from on the primary and secondary side of the optocoupler do not cross. Furthermore, in order to make full use of the IGBT's high-speed switching capabilities, we recommend using a optocoupler with short signal transmission delay.

＜Wiring between drive circuit and IGBT＞

If the wiring between the drive circuit and the IGBT is long, the IGBT may malfunction due to gate signal oscillation or induced noise. A countermeasure for this is shown below in Fig.4-6.

(1) Make the drive circuit wiring as short as possible and finely twist the gate and emitter wiring. (Twisted wiring)

(2) Increase R_G. However, pay attention to switching time and switching loss.

(3) Separate the gate wiring and IGBT main circuit wiring as much as possible, and set the layout so that they cross each other (in order to avoid mutual induction).

(4) Do not bundle together the gate wiring or other phases.

(5) If voltage is applied to the main circuit when the gate drive circuit is defective or not operating completely (gate open), the IGBT may be destroyed. As a prevention measure, it is recommended to connect a G-E resistance R_{GE} of about 10 kΩ (see Fig. 4-6).

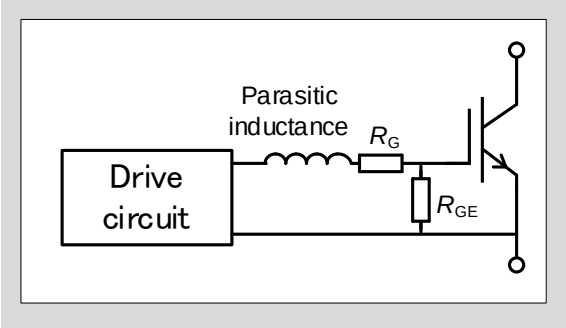


Fig.4-6 Precautions for mounting the gate drive circuit

＜Gate overvoltage protection＞

It is necessary that IGBT, like other MOSFET, are sufficiently protected against static electricity. Also, since V_{GE} max. is ±20V, if there is a possibility that voltage greater than this may be applied. As a protective measure it is necessary to connect a G-E zener diode as shown in Fig.4-7.

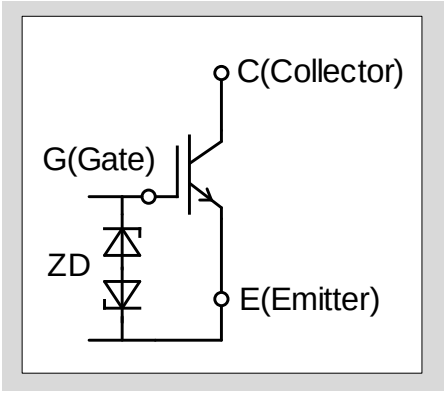


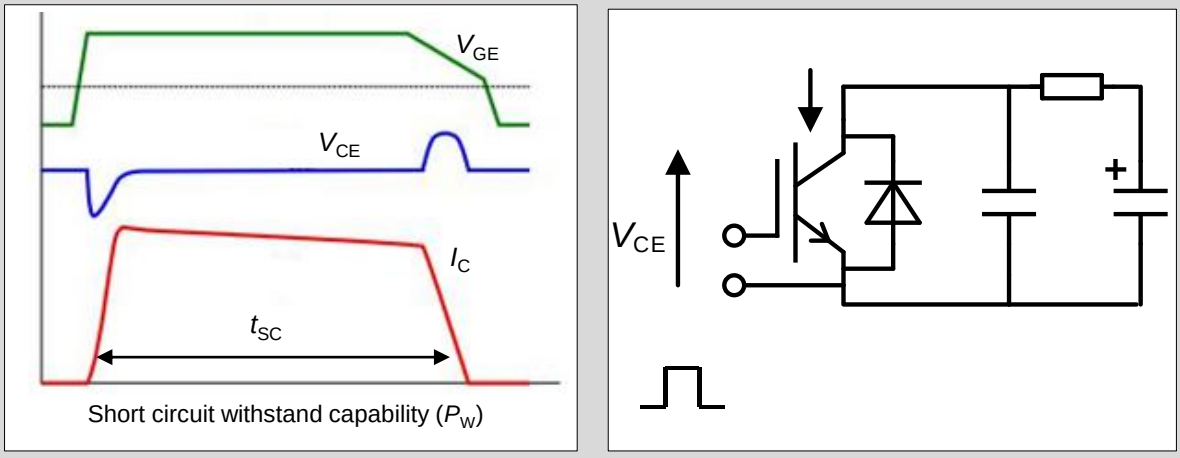
Fig.4-7 G-E overvoltage protection circuit example

＜Short circuit withstand capability＞

Overcurrent may flow in the IGBT due to the short circuit. If the overcurrent continues to flow, the temperature of the device will rise sharply, resulting in permanent destruction. As shown in Fig.4-8 (a), the short circuit withstand capability is specified by the time (t_{SC}) from the start of the short circuit current until the current is safely cut off. The short circuit withstand capability (t_{SC}) depends on conditions such as V_{CE}, V_{GE}, and T_{vj}. Generally, the higher the power supply voltage E_d and the higher the T_{vj}, the smaller the t_{SC}.

In our Discrete IGBT lineup, the V series is for applications that require long short circuit withstand capability, and High-Speed V, High-Speed W series and XS series for applications that require lower switching loss and lower saturation voltage instead of long short circuit withstand time. The short circuit withstand capability of the High-Speed W series 650V series and XS series is not guaranteed.

Fig.4-8(b) shows the circuit diagram for measuring short circuit withstand capability. When the load is short circuited, the IGBT will be subjected to high voltage / high current.



(a) Typical waveform at the time of short circuit　　(b) Measuring circuit diagram

Fig.4-8　Measuring circuit and waveform

＜Short circuit protection by V_{CE} detection＞

In this method, the operation from overcurrent detection to protection is performed on the drive circuit side, thus high-speed protection operation is possible. The short circuit protection schematic is shown in Fig.4-9. This circuit uses D1 to constantly monitor V_{CE}, so if during operation the IGBT's V_{CE} rises above the voltage limit set by D2, short circuit condition will be detected and T1 will be switched on while T2 and T3 are switched off. At this time, the accumulated charge at the gate is slowly discharged through R_{GE}, so overvoltage is suppressed when the IGBT is turned off. Fig.4-10 shows the IGBT waveform during short circuit protection.

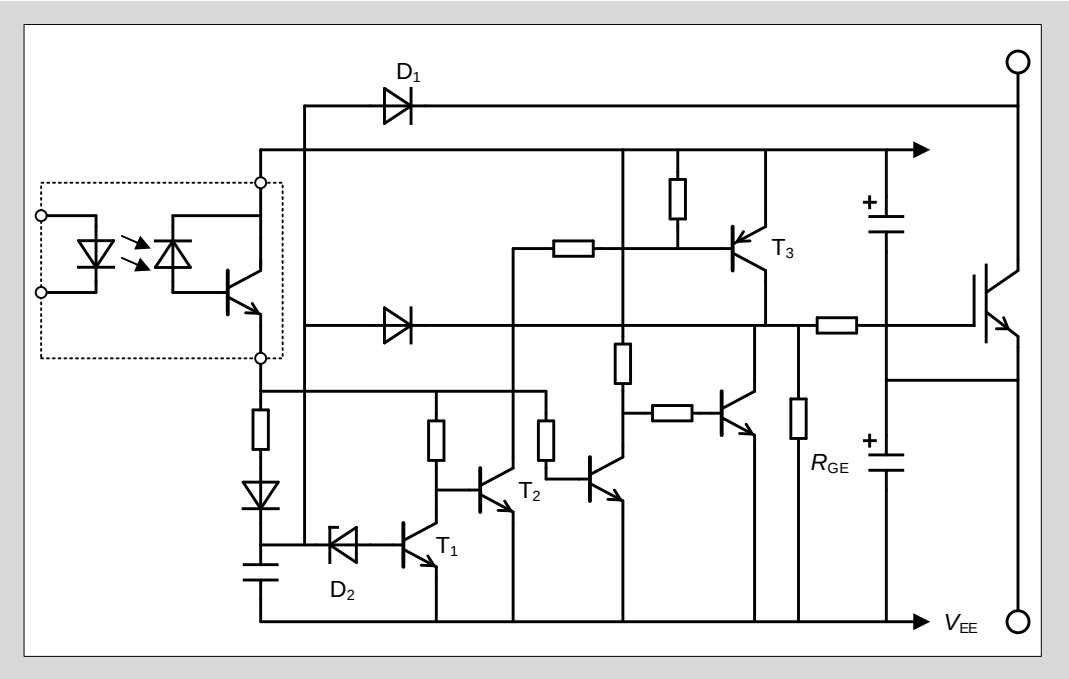
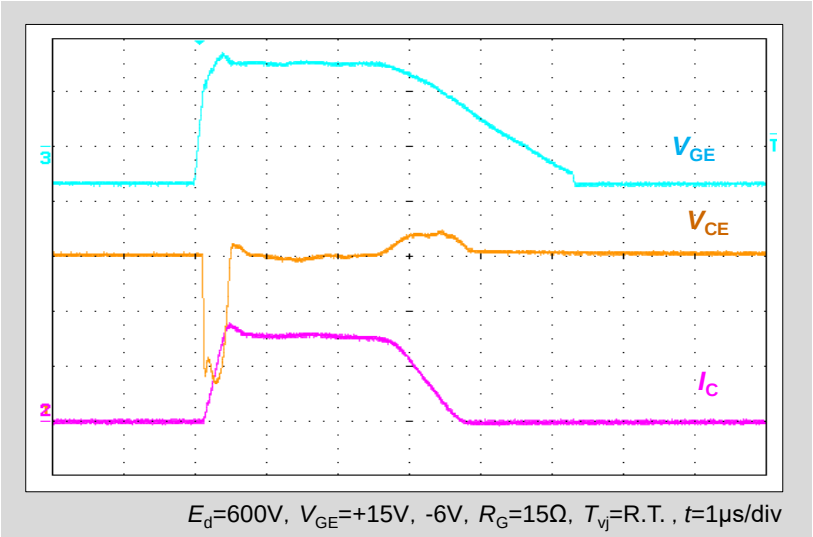


Fig.4-9 Short circuit protection schematic by V_{CE} detection



E_d=600V, V_{GE}=+15V, -6V, R_G=15Ω, T_{vj}=R.T. , t=1μs/div

Fig.4-10 Waveforms during short circuit protection

Chapter 5 Thermal Design

This chapter describes the thermal design.

1. Types of Power Loss

There are two types of discrete IGBT: IGBT-only products and products with IGBT + FWD configurations. It is necessary to consider both IGBT and FWD power losses of the latter. Fig.5-1 shows the power loss factors. Cooling capability has to be designed to keep $T_{vj(max.)}$ below the max. rated value. Calculate the power loss with on-voltage and switching loss values when the junction temperature T_{vj} is high. These data are described in the specifications.

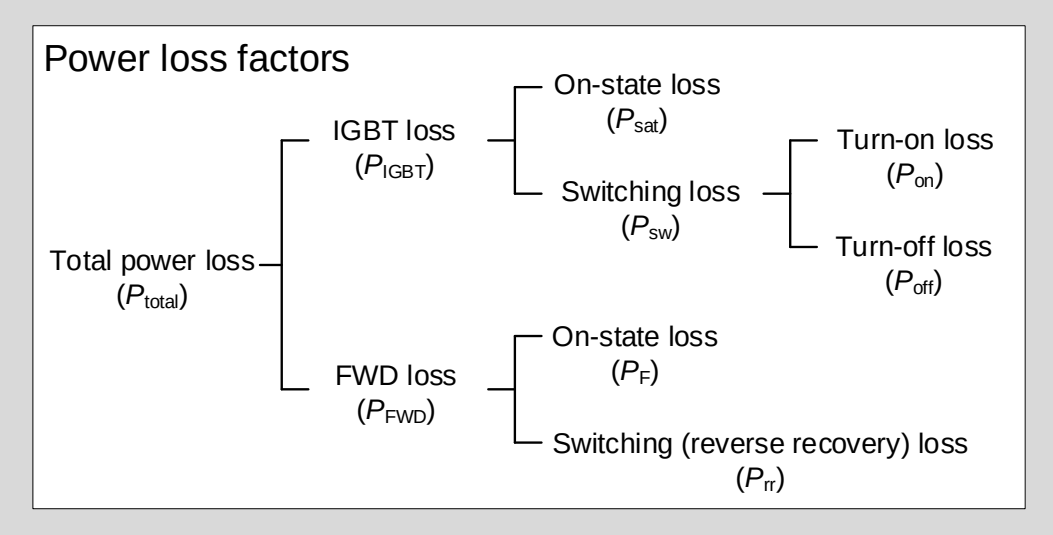


Fig.5-1 Power loss factors

2. DC Chopper Circuit Power Loss Calculations

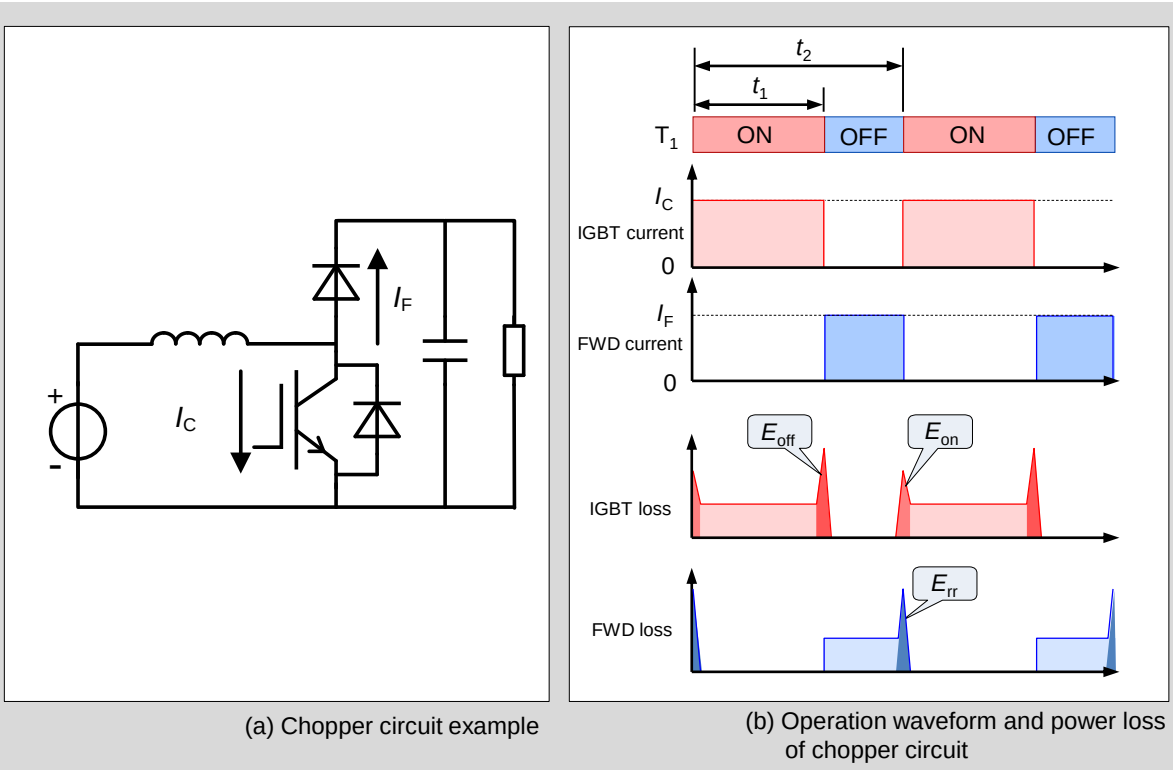
Approximate calculation can be performed by considering the current flowing through the IGBT or FWD as a series of square waves. Fig.5-2(a) shows an example of a chopper circuit. Fig.5-2(b) shows the approximate DC chopper waveforms, and the loss generated is calculated as follows.

IGBT loss (W)
= On-state loss + Turn-on loss + Turn-off loss

$$=V_{CE(sat)} \cdot I_C \cdot \frac{t_1}{t_2} + E_{on} \cdot f_C + E_{off} \cdot f_C$$

FWD loss (W)
= On-state loss + Reverse recovery loss

$$=V_F \cdot I_F - \left(1 - \frac{t_1}{t_2}\right) + E_{rr} \cdot f_C$$



(a) Chopper circuit example

(b) Operation waveform and power loss of chopper circuit

Fig.5-2 Power loss in chopper circuit

3. Concept of Heat Dissipation

During thermal design, the heat sink is selected so that the device temperature is below the permissible temperature based on the generated power loss. If the heat dissipation design is insufficient, problems such as device's failure due to temperature exceeding the permissible temperature may occur during actual operation.

＜Transient thermal impedance and steady-state thermal resistance＞

There are two types of heat dissipation method : mounting the device on a heat sink and only by the device itself. Fig.5-3 shows the former. The heat dissipation path is simulated by an electrical equivalent circuit for convenience.

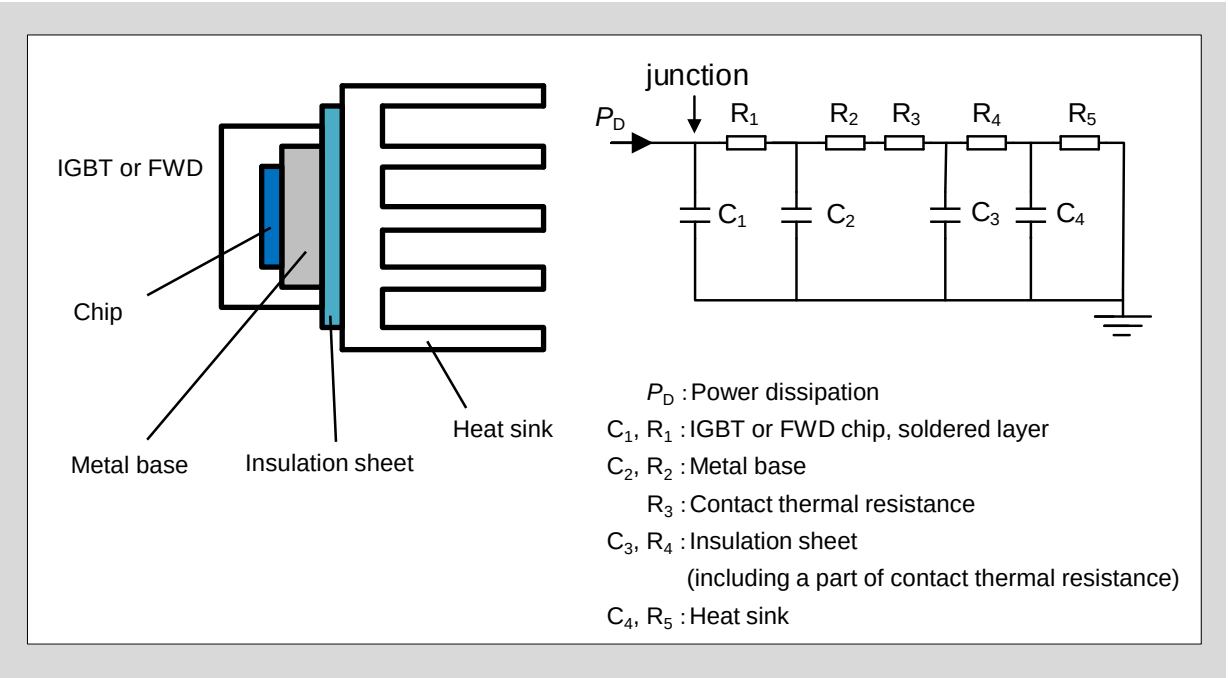


Fig.5-3 Electric equivalent circuit showing thermal behavior

The transient thermal resistance is the thermal resistance as a function of time, which is affected by the heat capacities C_1 to C_4 shown in the equivalent circuit in Fig.5-3. The max. value of the transient thermal resistance characteristics of each device is specified in the data sheet, and the repetition rate D≅0 corresponds to it. The transient thermal resistance of the heat sink can be obtained by the following equation.

$$R_{f(t)}=R_{th(f-a)}\left(1-\varepsilon^{-\frac{t}{\tau f}}\right)$$

where, $\tau f=R_{th(f-a)} \cdot V \cdot \gamma \cdot C$

$R_{th(f-a)}$: Heat sink steady thermal resistance [℃/W]
t : Time [sec]
τf : Thermal time constant of the heat sink [sec]
V : Heat sink volume [cm^3]
γ : Specific gravity [g/cm^3]
C : Specific heat [J/g• deg.]

Table.5-1 lists the specific gravity of materials required for this calculation, and Fig.5-4 shows the steady-state thermal resistance of an aluminum heat sink (coated in black).

Table.5-1 Specific gravity and specific heat of each material

Material	Specific gravity γ [g/cm³]	Specific heat [J/g• deg.]
Aluminum	2.71	0.895
Copper	8.96	0.383

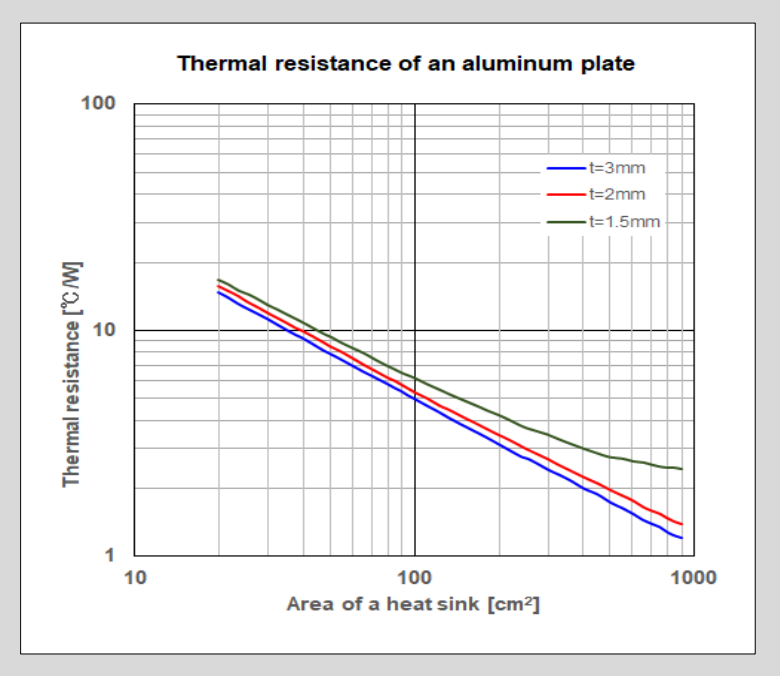


Fig.5-4 Steady-state thermal resistance of aluminum heat sink

4. Calculation of Junction Temperature

Since the steady-state thermal resistance is not affected by thermal capacitance, the junction temperature can be calculated easily.

$$T_{vj} = T_a + P_D \cdot (R_{th(j-c)} + R_{th(c-i)} + R_{th(i)} + R_{th(i-f)} + R_{th(f-a)})$$

T_{vj} : Junction temperature
T_a : Ambient temperature
$R_{th(j-c)}$: Thermal resistance between junction and case (IGBT or FWD thermal resistance)
$R_{th(i)}$: Insulation sheet resistance
$R_{th(c-i)}$, $R_{th(i-f)}$: Contact thermal resistance
$R_{th(f-a)}$: Thermal resistance of heat sink
P_D : Generated power dissipation

＜Thermal equation for transient power loss calculations＞

In general, it is sufficient to consider the steady-state T_{vj} based on the average power loss. However, practically, repetitive switching causes pulsed power loss and temperature ripples as shown in Fig.5-5. In this case, consider the power loss as a continuous constant cycles, constant-peak square wave pulses. Then the approximate peak value of the temperature ripples can be calculated using the transient thermal resistance curve given in the IGBT specification sheets as shown in Fig.5-6.

Be certain to select the heat sink that will also keep the T_{vjp} below $T_{vj\,(max)}$.

$$T_{vjp} - T_C = P \cdot [R_{(\infty)} \cdot \frac{t1}{t2} + R_{(t1+t2)} \cdot (1 - \frac{t1}{t2}) - R_{(t2)} + R_{(t1)}]$$

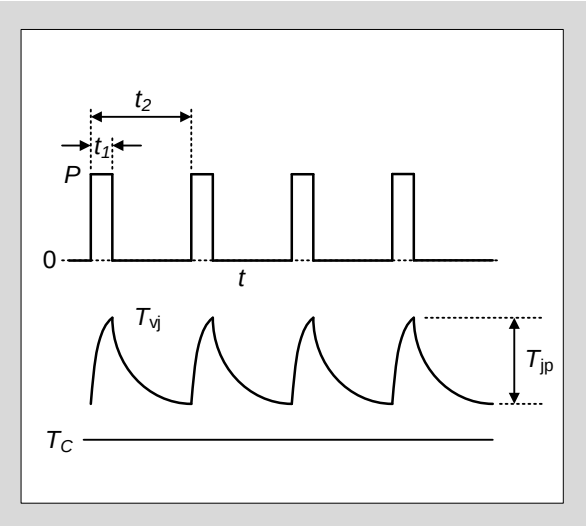


Fig.5-5 Thermal ripples

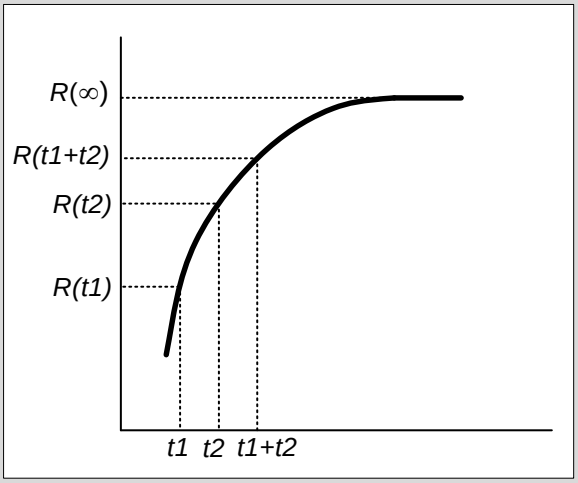


Fig.5-6 Transient thermal resistance curve

＜Transient thermal impedance characteristics of the device＞

Transient thermal impedance characteristics of the device is shown in the specification to assist in thermal designing. Fig.5-7 shows the transient thermal impedance characteristics of FGW40XS120C.

For example in Fig.5-7, in the case of a single pulse with a pulse width of 1ms, permissible power loss P_D when the device is mounted to a heat sink of 5 ℃/W under the condition of T_a=40℃ can be calculated by using the following formula:

$$P_D = \frac{T_{vj(max)} - T_a}{R_{th(f-a)} + R_{th(1ms)}}$$

$$= \frac{175\ [℃] - 40\ [℃]}{5\ [℃/W\ ] + 0.2\ [℃/W\ ]}$$

$$\cong 25.96\ [\ W\ ]$$

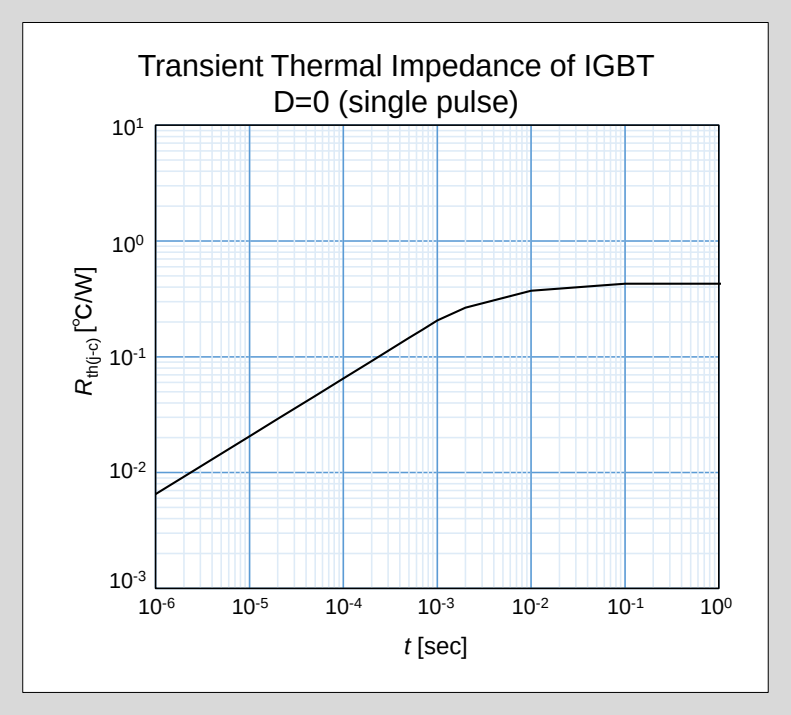


Fig.5-7 Transient thermal impedance characteristics of FGW40XS120C

Chapter 6 Precautions for Mounting and Handling

This chapter describes the precautions for mounting and handling.

1. Electrostatic Destruction Prevention Measures

Compared with small-signal MOSFET and IC, although IGBT has significantly higher electrostatic breakdown tolerance, they can be destroyed by static electricity.

＜How to remove static electricity from a conductor＞

As shown in Fig. 6-1, the static electricity charged on the conductor can be removed by proper use of conductive table mats, wrist straps and floor mats. The speed at which the charge is removed is determined by the resistance of the discharging path. Fig. 6-2 shows the equivalent circuit when the charged object of the conductor has a capacitance *C* and the path resistance is *R*. The voltage of the charged object is given as a function of time *t* as follows.

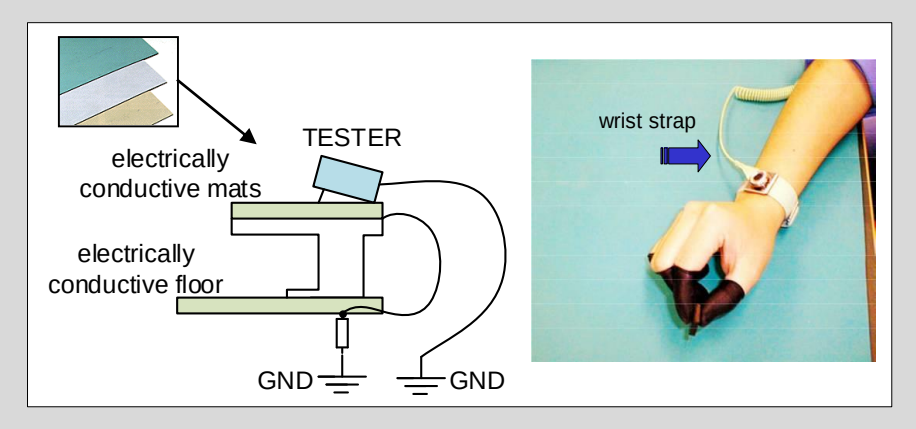


Fig.6-1 Example of measures against breakdown by static electricity

$$V = V_0 \cdot \exp\left(-\frac{t}{RC}\right)$$

V : Voltage of the charged body at time t [V]
V_0 : Initial voltage of the charged body [V]
t : Second [sec]
C : Capacitance of the charged body [F]
R : Path resistance [Ω]

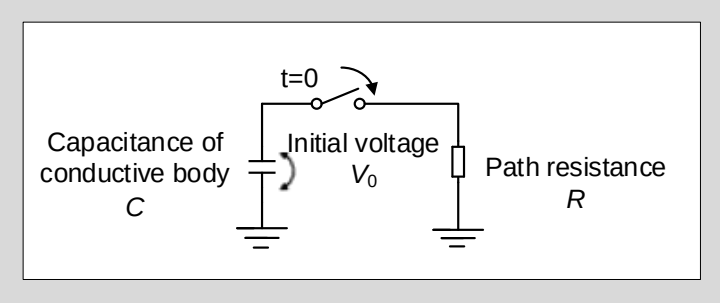


Fig.6-2 Equivalent circuit for static electricity discharge

＜Example＞

This example shows how to calculate the resistance when the static electricity level of workers is decreased to 100V or lower within 1 second according to technical document TB57-1 of the Electronic Industries Association of Japan (EIAJ, currently JEITA). Substitute the following into the formula:

V = 100V (safe voltage), V_0 = 10kV (Initial voltage of the human body or charged body)
t = 1sec. (Longest permissible time for achieving the safe voltage of 100V)
C = 200pF (Average value of human body capacitance of 100pF to 400pF)
R = Max. permissible resistance to the ground [Ω]

$$100 = 1 \times 10^{4} \cdot \exp\left(-\frac{1}{200 \times 10^{-12} \cdot R}\right)$$

Thus, R ≅ 1.09 × 10^9Ω = 1090 MΩ is obtained. From this calculation, it is found that if the resistance from the table mat, floor mat, or wrist strap to the ground is 1000MΩ or lower, discharge to a safe voltage of 100V can be achieved within 1 sec., and the devices can thus be protected against electrostatic breakdown. Table.6-1 lists the voltage range in which various devices may result in breakdown due to electrostatic discharge from workers.

Table.6-1 Breakdown voltage by device

Type	Voltage range [V]
IGBT, MOSFET	100～200
Junction FET	140～10000
C MOS	250～2000

2. Soldering

During soldering, usually the temperature of the terminal exceeds the max. T_{stg}. Pay attention to the following when soldering.

(a) Recommended mounting condition

Package	Method				
	Wave Soldering (Full dipping)	Wave Soldering (Only terminal)	Infrared Reflow	Air Reflow	Soldering iron (Re-work)
TO-247	×	◎	×	×	○

◎ : Possible ○ : Limited to once × : Not possible

Soldering temperature	Immersion time
260±5℃	10±1 sec
350±10℃	3.5±0.5 sec

(b) The immersion depth of the terminal should be 1 to 1.5 mm away from the package.
(c) Be careful not to immerse the product in the soldering liquid when mounting the device by the solder flow method.
(d) When using flux, it is desirable to use rosin-based flux, and not chlorine-based flux.

3. Processing and Mounting of Through Hole Terminal

(a) Stress to the terminals

Applying unnecessary stress to the terminals will damage the internal chip and external package. The load applied in the direction shown in Fig. 6-3 should be 1 kg or less.

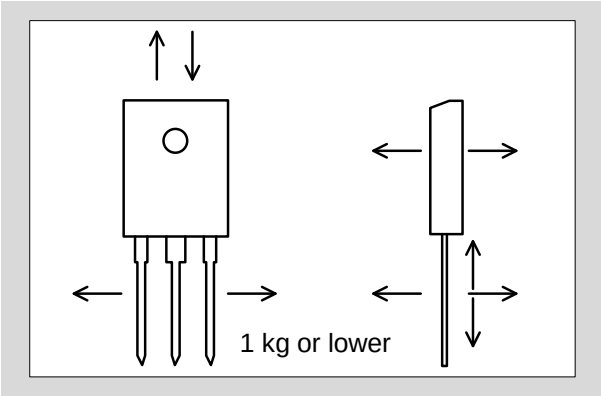


Fig.6-3 Stress to the terminals

(b) Cautions in molding terminals

If there is no other choice but to mold terminals for convenience of parts layout, pay attention to the following:

- Use special jigs that does not put stress on the internal chip and external package.
- When bending the terminal in the horizontal direction, bend it at a distance of 4.5mm or more away from the package, and keep the bending angle within 30° (Fig.6-4).
- When bending the terminal at right angle against the package, bend it at a point that is at least 4.5mm or more away from the package.
- Molding should be performed only once at a place, and do not perform re-molding or restore to the original shape.

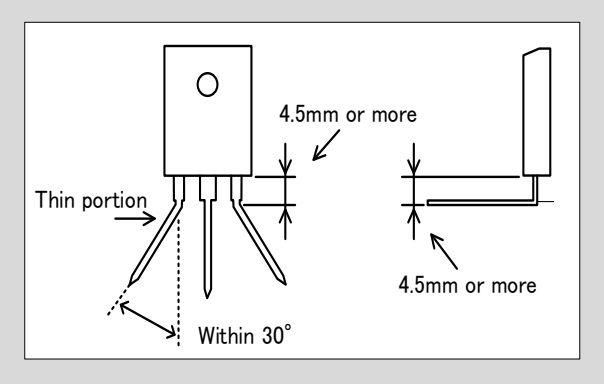


Fig.6-4 Cautions in molding terminals

(c) Insertion into printed circuit board

When inserting terminals into printed circuit board, coincide the distance between terminals and that of insertion holes to prevent excessive stress from being applied to the base of the terminals.

4. Cleaning

When soldering is performed with using flux, cleaning with solvent is required. In this case, pay attention to the following :

(a) Solvent

- Do not use flammable, toxic, and corrosive solvent.
- Never use trichloroethylene series solvent because it contains chlorine.

(b) Cleaning method

Soaking is recommended. When conducting ultrasonic cleaning, set the frequency to avoid the resonance point (several tens of kHz), and be careful not to let the device or printed circuit board to come into contact with the oscillation source directly.

5. Mounting to Heat Sink

(a) If the tightening torque of the mounting screw is too small, the thermal resistance will increase and there are risks of thermal destruction. We recommend values within the range shown in Table 6-2.

Table.6-2 Semiconductor device tightening torque

Package	Diameter of mounting hole	Used screw	Optimum tightening torque (N • cm)
TO-247	φ3.2	M3	40-60

(b) It is recommended to apply grease thinly and uniformly to improve the thermal conductivity between the device and the heat sink to improve heat dissipation.

(c) Application of thermal grease

In order to fill the gap between the device and the insulating sheet, and between the insulating sheet and the heat sink with thermal grease, apply the grease in dots to the case and the surface of the heat sink directly under the semiconductor chip, and tighten the heat sink with screws with the recommended tightening torque.

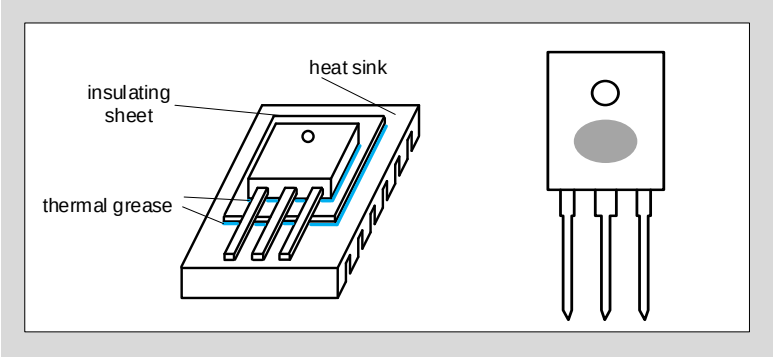


Fig.6-5 Thermal grease application

(d) Surface flatness of heat sink ≦ ±30μm

(e) Surface roughness of heat sink ±10μm

(f) Do not taper the screw holes.

Chapter 7 Typical Troubles and Troubleshooting

This chapter describes typical troubles and how to deal with them.

1. Troubleshooting

When abnormalities such as device failure occurs, it is necessary to clarify the situation and determine the cause before taking countermeasures. Referring to Table 7-1, please investigate the failure mode and analyze the causes of abnormalities by observing the irregularities outside of the device. If the cause cannot be determined by using Table 7-1, use the detailed diagram shown in Fig.7-1(a-f) to help your investigation.

Table.7-1 Device destruction mode and cause estimation

External abnormalities		Cause		Device failure mode	Check point
Short circuit	Arm short circuit	After short circuit detection, when protection is applied (turn-off), the overvoltage exceeds SCSOA and the device is destroyed		SCSOA failure (overvoltage) destruction	Matching of the operation locus and device withstand capability during arm short circuit
	Series arm short circuit (upper and lower arm short circuit)	Insufficient dead time	t_{off} increased due to insufficient -V_{GE}, dead time setting error	Overheat (short circuit withstand capability) failure	Check that t_{off} and dead time match
		dv/dt shoot through and causes short circuit failure	Insufficient -V_{GE}, long gate wiring	SCSOA and overheat failure	Check for d*v*/d*t* erroneous turn-on
		Short circuit failure due to noise etc.	Gate drive circuit malfunction, logic circuit malfunction		Circuit malfunction check
	Output short circuit	Wiring mistake, abnormal wire contact, load short circuit			Check the conditions during failure, matching of device withstand capability and protection circuit, ground fault wiring condition
	Ground fault	Wiring mistake, abnormal wire contact.			
Overload (overcurrent)		Overcurrent flows	Logic circuit malfunction	Overheat	Logic signal
			Overcurrent protection setting error		Review of overcurrent protection setting value
Overvoltage	Excessive DC voltage	Overvoltage exceeding the device withstand voltage is applied to C-E	Excessive input voltage	C-E overvoltage	Review of overvoltage protection level
			Overvoltage protection setting error		
	Excessive overvoltage	Overvoltage at turn-off exceeds RBSOA		RBSOA	Matching of turn-off operation locus and RBSOA, review of snubber circuit
		Overvoltage during FWD reverse recovery exceeds device withstand voltage		C-E overvoltage	Matching of overvoltage and device withstand voltage, review of snubber circuit
		Gate signal interruption, etc., that result in very short off pulse, causes turn-off → turn-on in very short time intervals (on the order of several hundred ns) and generate excessive reverse recovery overvoltage that exceeds the device withstand voltage (hereinafter, short off pulse reverse recovery phenomenon)	Logic or gate drive circuit malfunction due to noise		Logic and gate signals
			Electromagnetic induction from the main circuit to the gate signal line		Gate signal during high current operation / twisted wire of gate signal line / distance from main circuit to gate signal line
Drive supply voltage drop		V_{GE} drops below the design value, V_{CE} increases, heat generation (loss) increases, causing destruction	DC-DC converter malfunction	Overheat	Check circuit
			Drive supply voltage rise is too slow		
			Gate signal wiring disconnected		
Gate overvoltage		Static electricity is applied to G-E		G-E overvoltage	Check working status (static electricity countermeasures)
		The gate wiring is too long, resulting in overvoltage exceeding G-E withstand voltage			Check gate voltage
Driving with open gate		Destruction by applying C-E voltage (on voltage / withstand voltage measurement, etc.) while the gate is open		Overheat destruction	Check gate voltage
Overheat	Insufficient heat dissipation capacity	Insufficient heat dissipation capacity causes the device to overheat beyond T_{vj} max.	Loose terminal mounting screws	Overheat	Check heat dissipation condition
			Insufficient application of thermal grease		
	Thermal runaway		Cooling fan malfunction		Check logic circuit
Stress	Stress	The terminal soldering part inside the product is disconnected due to stress fatigue	Stress applied to terminals from external wiring	Electrical wiring disconnection inside the product (open)	Stress generated at terminals / mounting state of product and other parts
	Vibration		Vibration of other mounting parts applied stress to the terminals		
Reliability		The application conditions (environment, temperature change, assembly conditions at the time of mounting, storage condition, etc.) of the device and the reliability of the product does not match, causing failure of wiring inside the product, insulation structure, appearance, etc.		Failure mode is different for each case	Check based on Fig.7-1

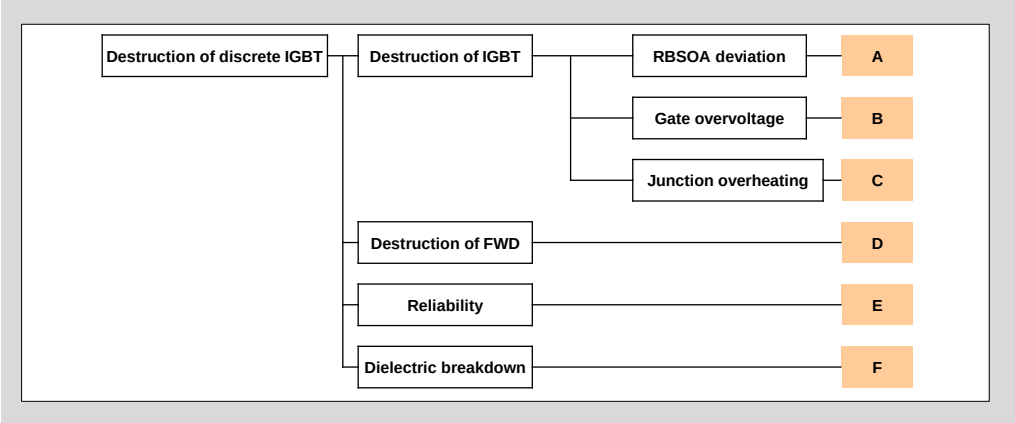


Fig.7-1 IGBT failure analysis diagram (A-E symbols are connected to the following figures)

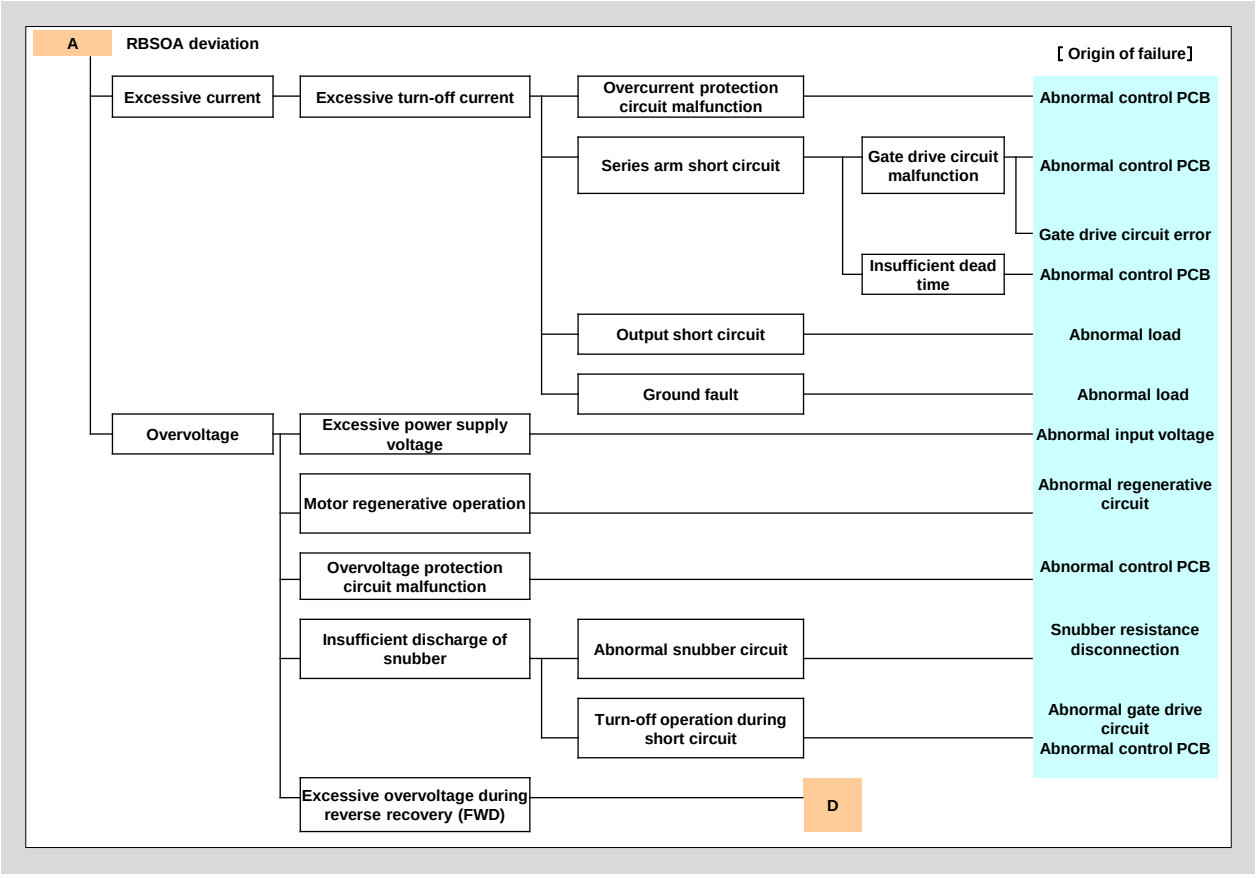


Fig.7-1(a) Mode A: RBSOA deviation

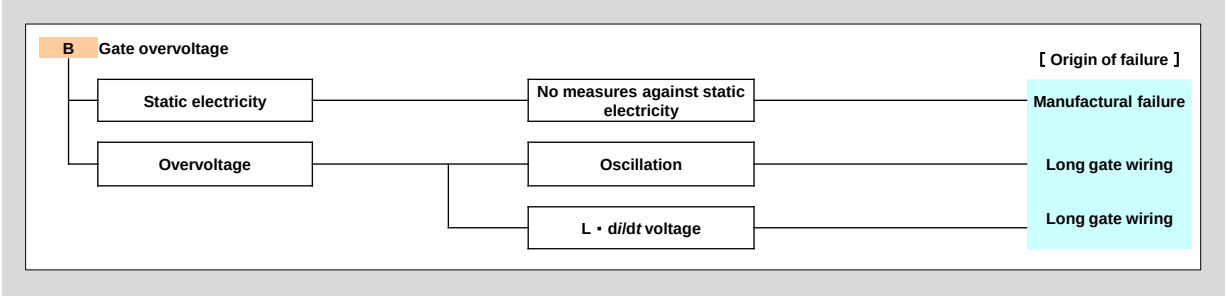


Fig.7-1(b) Mode B: Gate overvoltage

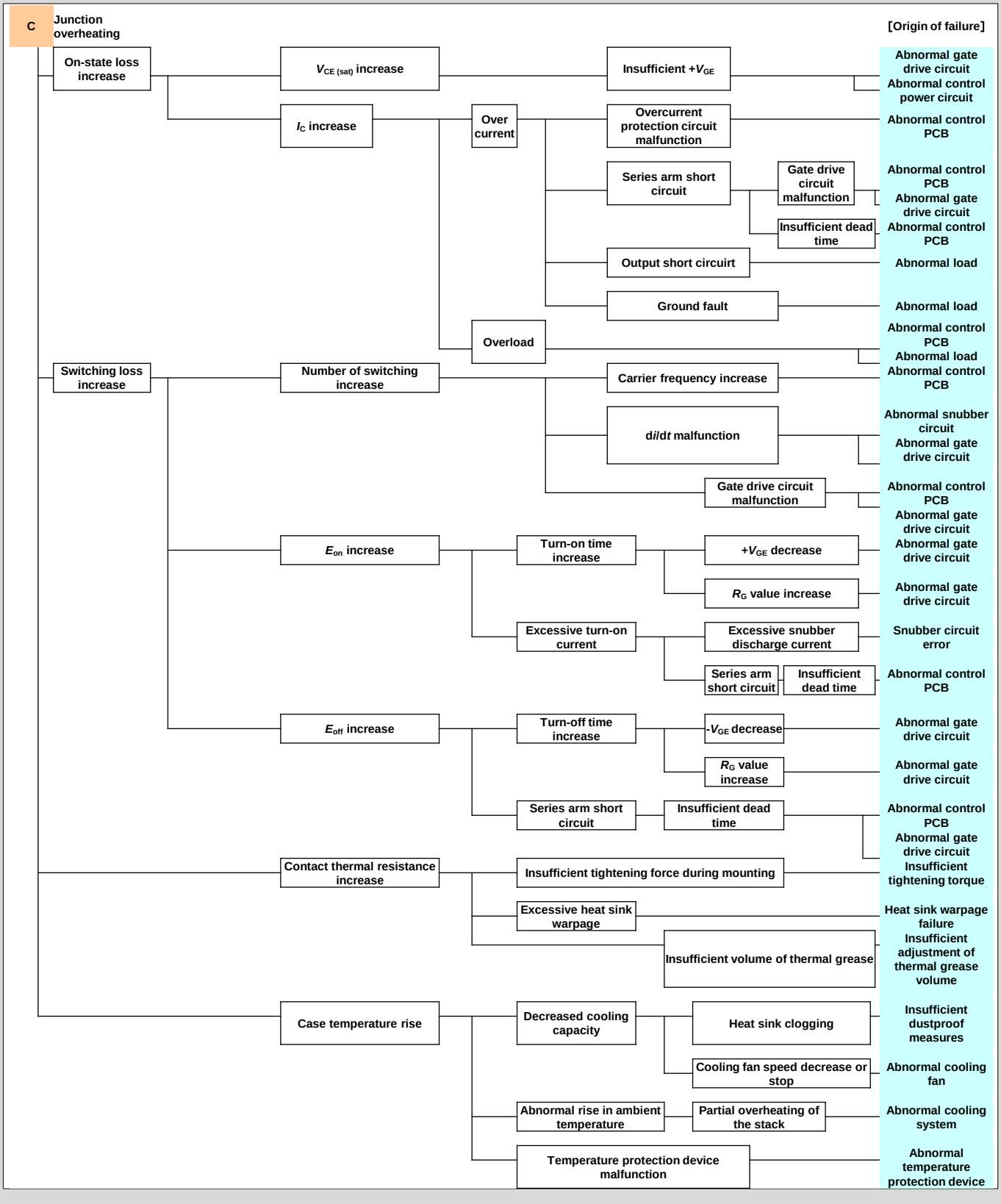


Fig.7-1(c) Mode C: Junction overheating

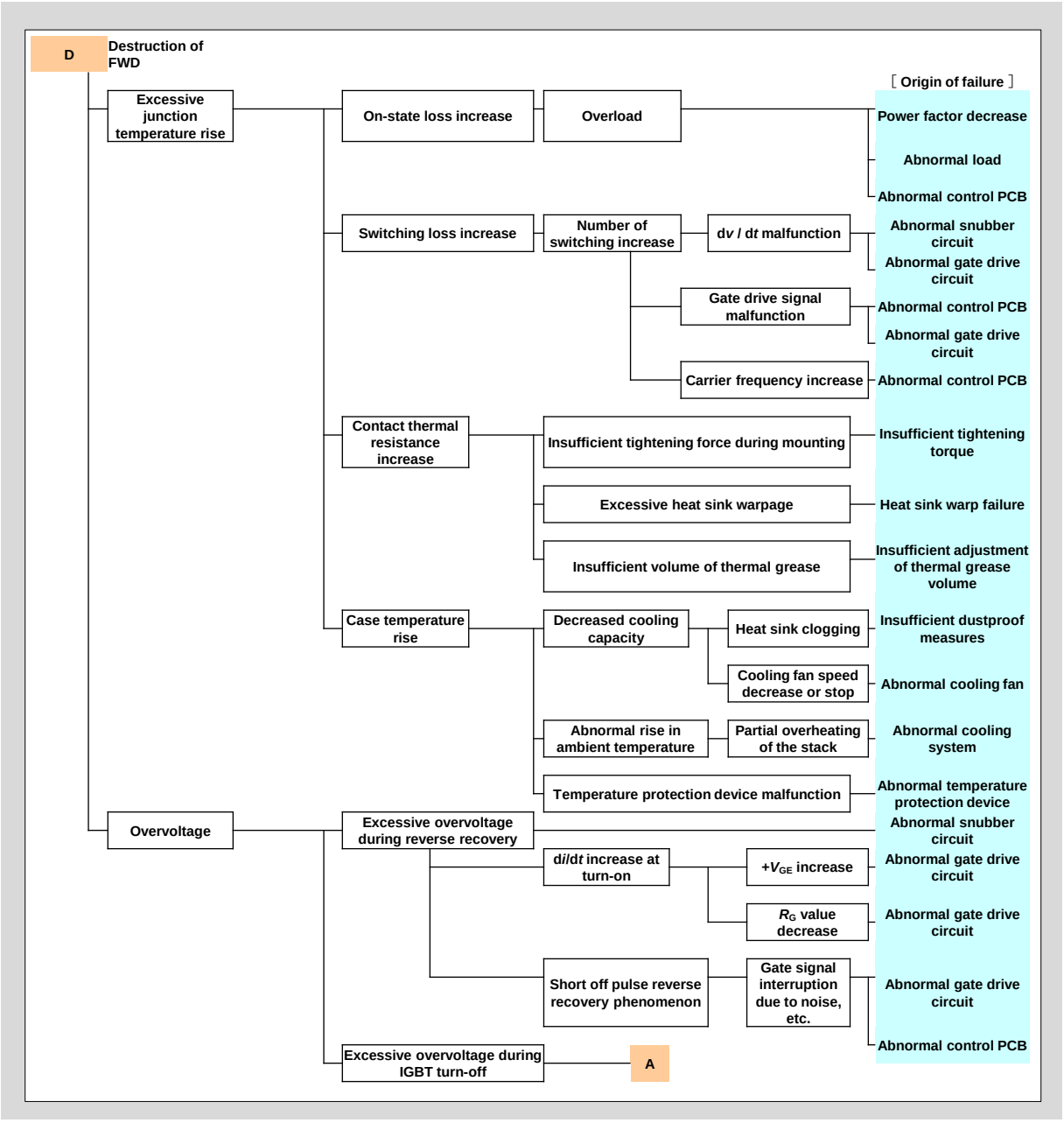


Fig.7-1(d) Mode D: Destruction of FWD

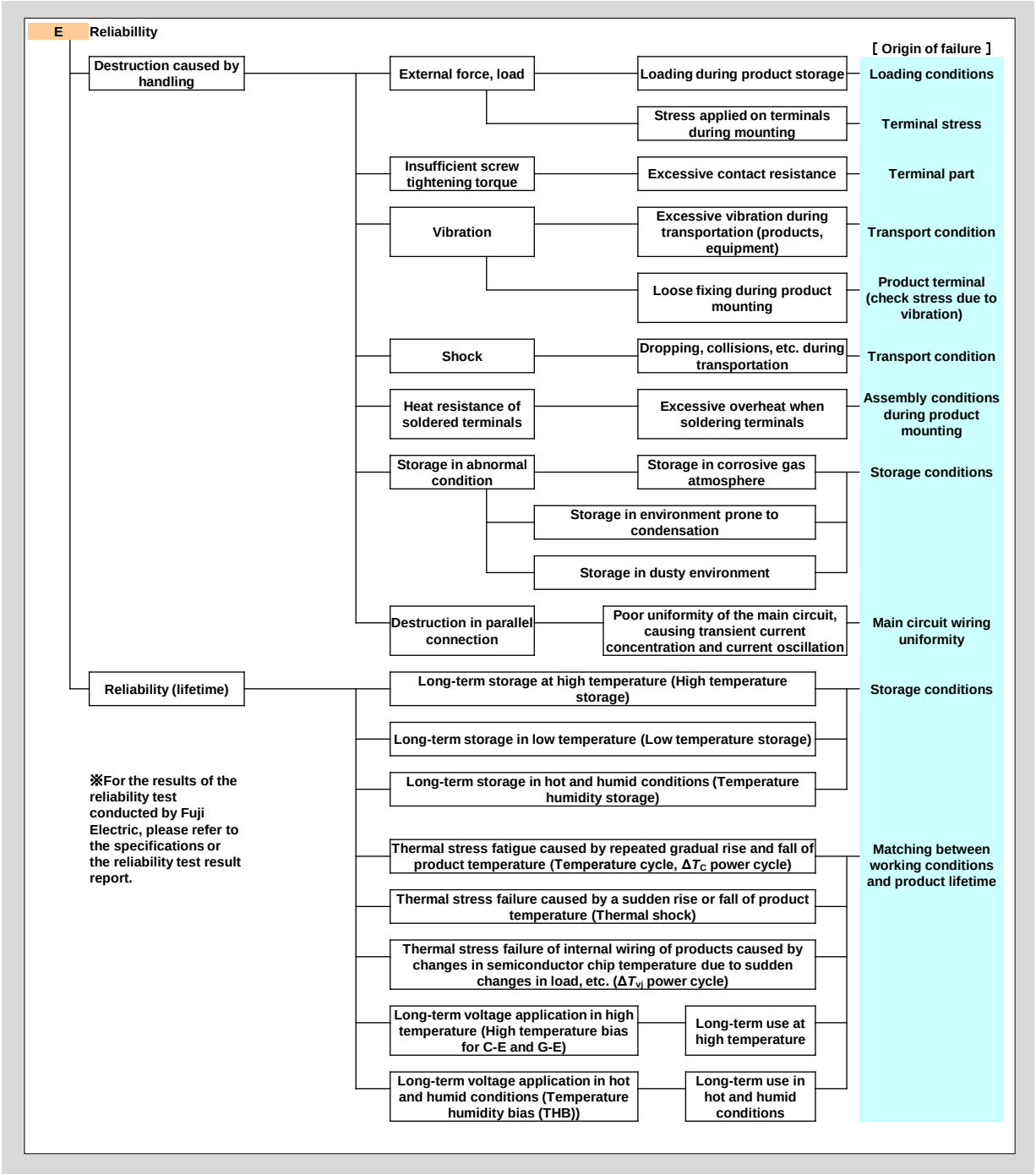


Fig.7-1(e) Mode E: Reliability

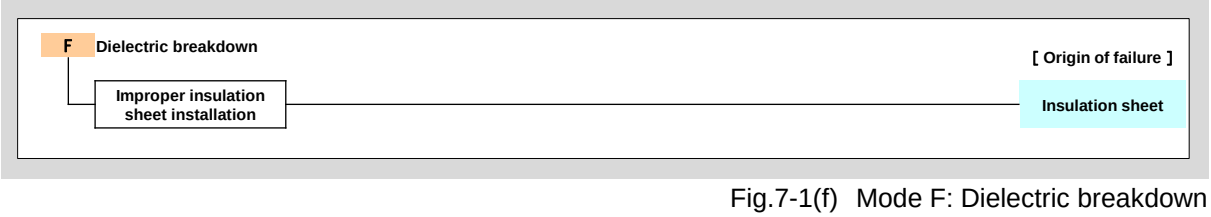


Fig.7-1(f) Mode F: Dielectric breakdown

2. IGBT Test Procedures

The following items can be determined by using a transistor curve tracer (hereinafter as CT) to check the faulty IGBT.

① G-E leakage current ② C-E leakage current (G-E must be shorted)

Other test equipment, such as a Volt-ohm multi-meter that is capable of measuring voltage/resistance and so forth to determine failures, can be used to help diagnose the fault.

＜G-E check＞

As shown in Fig.7-2, measure the G-E leakage current or resistance, with C-E shorted. If the product is normal, the leakage current should be several hundreds nA and the resistance should be several tens of MΩ to infinity. If the leakage current is more than a few nA or the resistance value is less than a few MΩ, the device may be defective.

Do not apply G-E voltage in excess of 20V. When using a Volt-ohm multi-meter, make sure the internal battery voltage is below 20V.

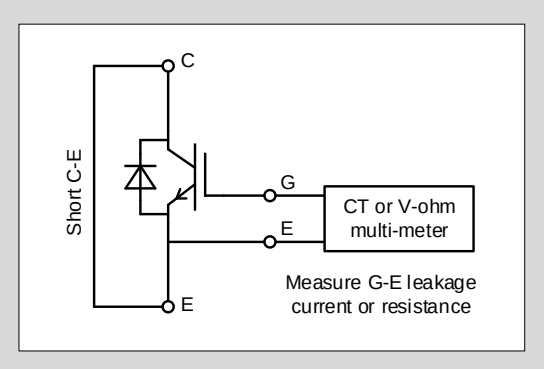


Fig.7-2 G-E check

＜C-E check＞

As shown in Fig.7-3, measure the C-E leakage current or resistance, with G-E shorted. If the IGBT is normal, the leakage current should be below I_{CES} max. specified in the datasheet. Please note the following items.

① Be sure to connect C to (+) and E to (-). Reverse connections will conduct the FWD thus making measurement impossible.

② Do not apply voltage higher than the rated value. Applying voltage higher than the rated value may destroy the device.

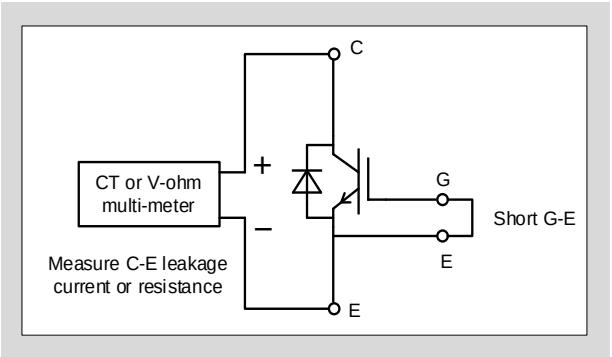


Fig.7-3 C-E check

3. Typical Troubles and Troubleshooting

＜How to avoid d*v*/d*t* shoot through during FWD reverse recovery＞

This section describes how to avoid d*v*/d*t* shoot through of the IGBT during FWD reverse recovery. Fig.7-4 shows the causes of d*v*/d*t* shoot through. In this fig., IGBT2 is reverse biased. If IGBT1 changes from off to on, FWD2 on the opposite arm goes in to reverse recover mode. At the same time, the voltage potentials of IGBT2 and FWD2 in the off-state rise, and d*v*/d*t* is generated according to the switching time of IGBT1. Since IGBT1 and IGBT2 have C_{res}, current $I = C_{res} \cdot dv/dt$ is generated through C_{res}. This current flow through R_G, resulting in rise of V_{GE}. If this V_{GE} exceeds the sum of the reverse bias voltage of IGBT2 and the threshold voltage $V_{GE\,(th)}$, IGBT2 will be turned-on, resulting in short circuit of IGBT1 and IGBT2.

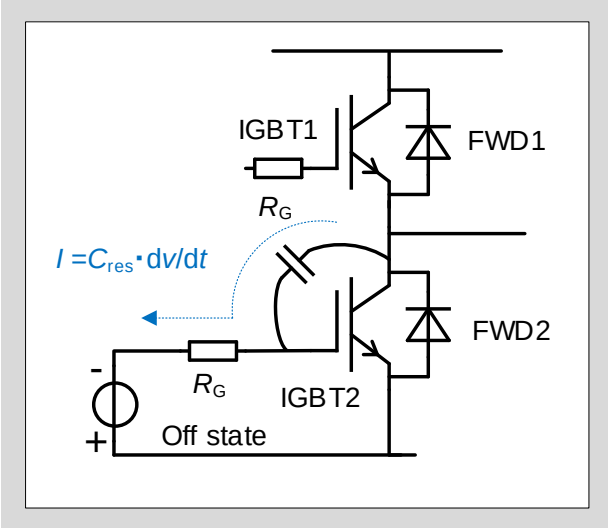
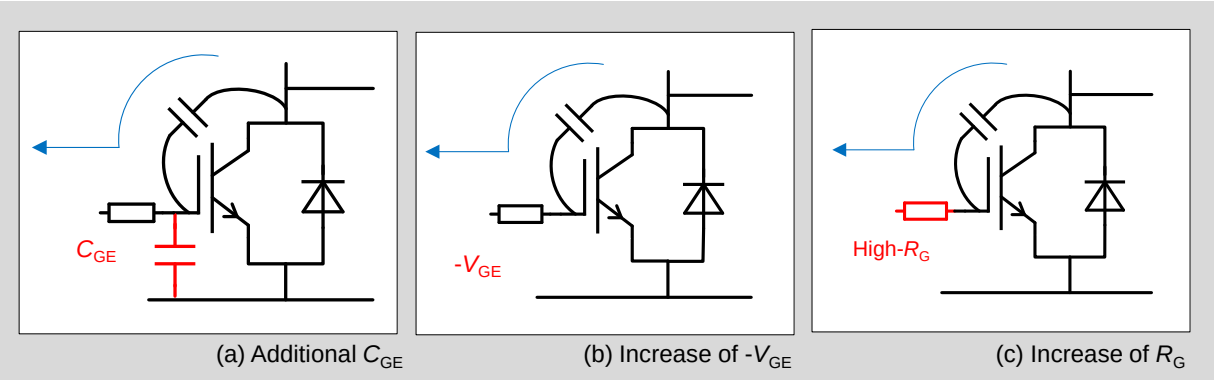


Fig.7-4 Principle of dv/dt shoot through

Fig.7-5 shows the method to avoid the shoot through.



(a) Additional C_{GE} (b) Increase of $-V_{GE}$ (c) Increase of R_G

Fig.7-5 How to avoid d*v*/d*t* shoot through

There are three methods, which are C_{GE} addition, increase of $-V_{GE}$ and increase of R_G. Check the effects of these measures as they differ depending on the gate drive circuit. Also, check the effect of these measures on switching loss.

The method to add C_{GE} is the way to decrease the current flowing through R_G by passing through C_{GE}. However, in order to charge/discharge the additional C_{GE}, switching speed becomes slower. Thus, just adding C_{GE} results in increase switching loss. However, by reducing R_G and adding C_{GE}, it is possible to avoid the shoot through without increasing switching loss.

Recommended C_{GE} is about two times the value of C_{ies} described in the specification sheet, and recommended R_G is about half the value before adding C_{GE}.

＜Energizing main circuit voltage when G-E is open＞

When checking the characteristics of a single device, if voltage is applied to C-E when G-E is open, current (*i*) will flow through C_{res} of the IGBT as shown in Fig.7-6. As a result, G-E capacitance is charged and the gate potential rises, causing the IGBT to turn-on. Thus, I_C flows and heat is generated, which may cause destruction. When driving the IGBT, be sure to drive it with a G-E signal. Also, be sure to discharge the main circuit voltage (C-E) to 0V before switching the gate signal.

Fig.7-7 shows an example of on-voltage measurement circuit. The measurement sequence is described with reference to this measurement circuit. First, turn-off the gate drive unit (GDU) (V_{GE} = 0V). Then turn-on SW1 to apply C-E voltage. Next, apply predefined forward bias voltage from the GDU to energize the IGBT, and measures the on-voltage. Lastly, turn-off the gate circuit and turn-off SW_1. This sequencing will allow for the safe measurement of device characteristics without risking destruction.

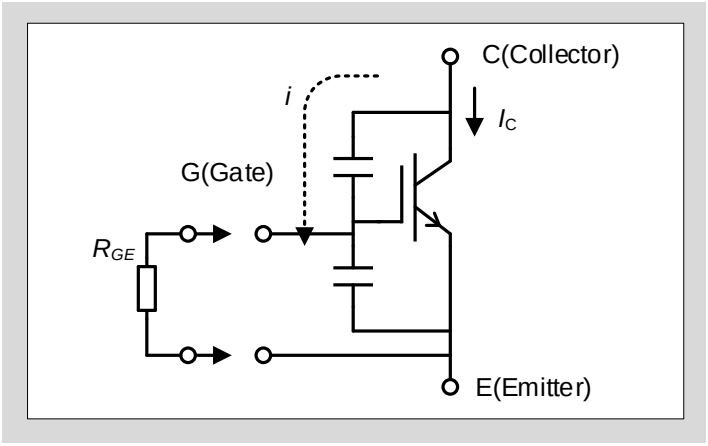


Fig.7-6 IGBT behavior when G-E is open

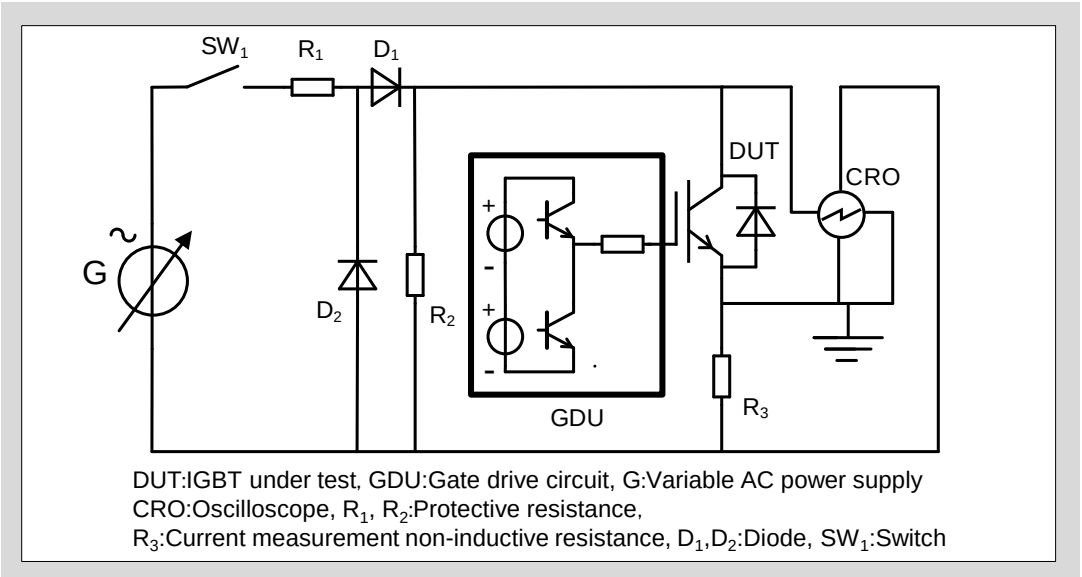


Fig.7-7 On-voltage measurement circuit

＜Diode reverse recovery from transient on-state (short off pulse reverse recovery)＞

If very short off pulses are generated when gate signal interruption happens due to noise while driving the IGBT, excessive reverse recovery overvoltage will occur. This phenomenon is called the short off pulse reverse recovery. Fig.7-8 shows the timing chart of this phenomenon.

In Fig.7-9, when an off signal T_w is generated at V_{GE} during period T_{on} in which IGBT2 is on, IGBT2 is turned off while FWD1 on the opposite arm side is turned on, and IGBT2 is immediately turned on again while FWD1 goes into reverse recovery. Normally, reverse recovery started after sufficient carriers are accumulated in the FWD. On the other hand, in the short off pulse reverse recovery, FWD goes into reverse recovery without sufficient carrier accumulation. As a result, the depletion layer spreads rapidly in the FWD, causing steep d*i*/d*t* and d*v*/d*t*, and very large C-E (A-K) overvoltage as shown in the dotted line in Fig.7-8. If the overvoltage exceeds the device voltage rating, the device may be destroyed. When designing the equipment, be careful not to design a circuit that will generate such short gate signal off pulse.

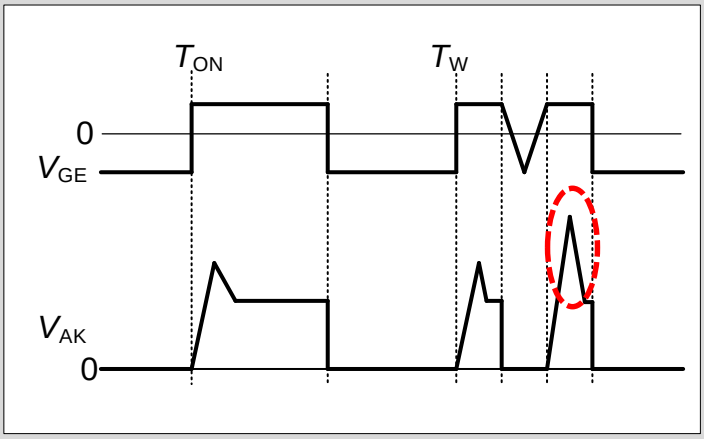


Fig.7-8 Waveforms during short off pulse reverse recovery

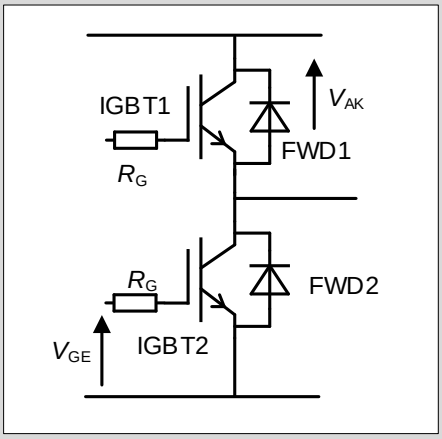


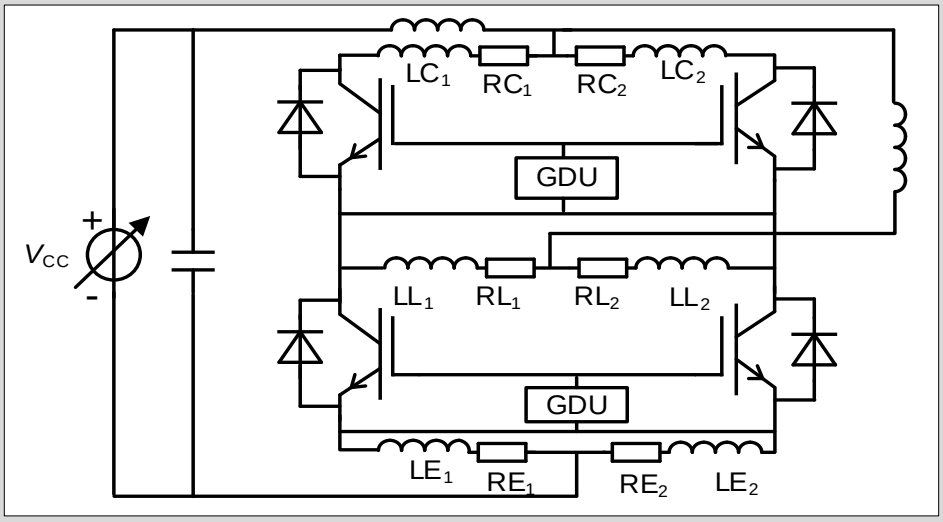
Fig.7-9 Circuit diagram

＜Precautions in parallel connection＞

When using IGBT to control large current, IGBTs may be connected in parallel. If the current is not balanced among the IGBTs, current may concentrate on one device and destroy it. The electrical characteristics of the IGBT as well as the wiring design, affect the current balance between parallel connected IGBT. In order to maintain current balance it is necessary to match the $V_{CE(sat)}$ values of all devices. When connecting in parallel, we recommend to use products from the same product lot.

When the main circuit wiring is uneven, uneven voltage is generated in the inductance of each wiring due to d*i*/d*t* during switching, and oscillating current flows through the control side wiring loop of the emitter connected in parallel, causing the gate voltage to oscillate. This oscillation may cause the IGBT to malfunction.

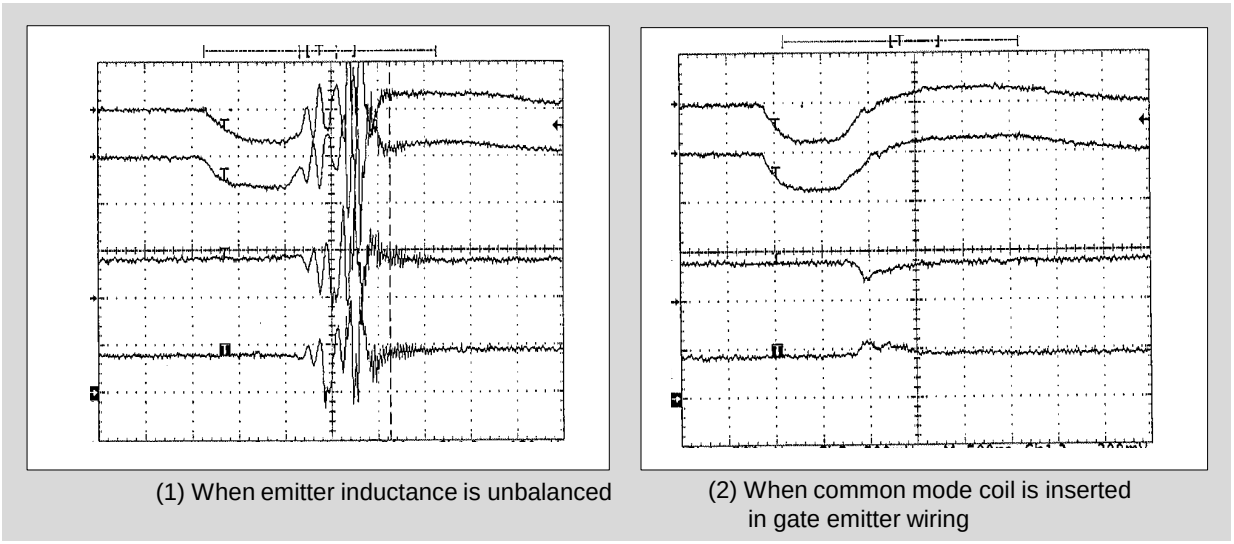
Balanced current sharing can be achieved by using symmetrical wiring to prevent the above-mentioned IGBT malfunction (see Fig. 7-10).



Wiring so that RC1=RC2, RL1=RL2, RE1=RE2,LC1=LC2, LL1=LL2,LE1=LE2

Fig.7-10 Equivalent circuit of parallel connection

Fig.7-11(1) shows the oscillation phenomenon when the wiring inductance of the emitter is made extremely unbalanced.



(1) When emitter inductance is unbalanced

(2) When common mode coil is inserted in gate emitter wiring

Fig.7-11 Waveforms of 2 parallel connection

A common mode coil can be inserted in each gate emitter wiring to eliminate the loop current in the emitter. Fig.7-11 (2) shows the waveforms with the common mode coil. Compared with Fig.7-11(1), oscillation is suppressed.

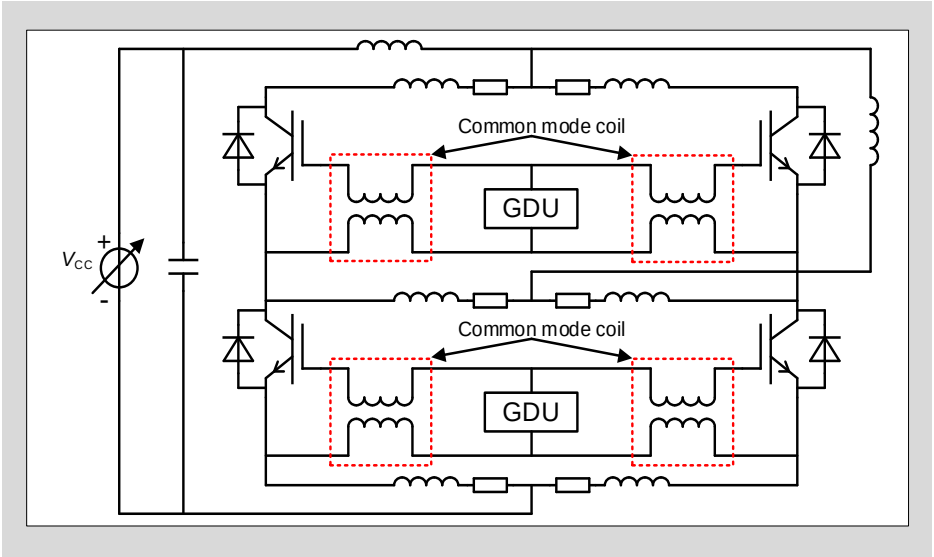


Fig.7-12 Parallel circuit with common mode coil inserted

Chapter 8 Precautions for Storage and Transportation

This chapter describes the precautions for storage and transportation.

1. Storage

(a) It is desirable that devices be stored in a place of normal temperature and humidity. Temperature and humidity are approximately 5 to 35℃ and 45 to 75%, respectively. When storing molded type power transistors in area that becomes extremely dry in winter, humidification by a humidifier is required. If tap water is used for humidification, chlorine contained in it may cause corrosion of the terminals of the device. To prevent this, use pure water or boiled water for humidification.
(b) Avoid storing devices in a place where corrosive gas is generated or subjected to much dust.
(c) Avoid storing devices in a place subjected to sharp temperature change. Otherwise condensation may occur to the devices. Store the devices in a place having min. temperature change.
(d) Pay attention not to apply load to devices during storage. In particular, if they are stored stacked on top of each other, unexpected load may be applied. Also, avoid placing heavy objects on top.
(e) Store the devices with each terminal unprocessed to avoid occurrence of corrosion, which may result in soldering defect at the time of processing.
(f) Store the devices in containers that is not affected by static electricity easily, or the one used for the delivery of the product.
(g) All storage shelves should be made of metal. Be sure to ground them.

2. Transportation

(a) Be careful not to cause impact on the devices such as dropping them, etc.
(b) When transporting large number of devices in boxes, arrange the devices by using soft spacers to prevent the contact electrode surface, etc. from being damaged.
(c) Take measures against static electricity by using conductive bags or aluminum foil to prevent static electricity being applied to G-E terminals.

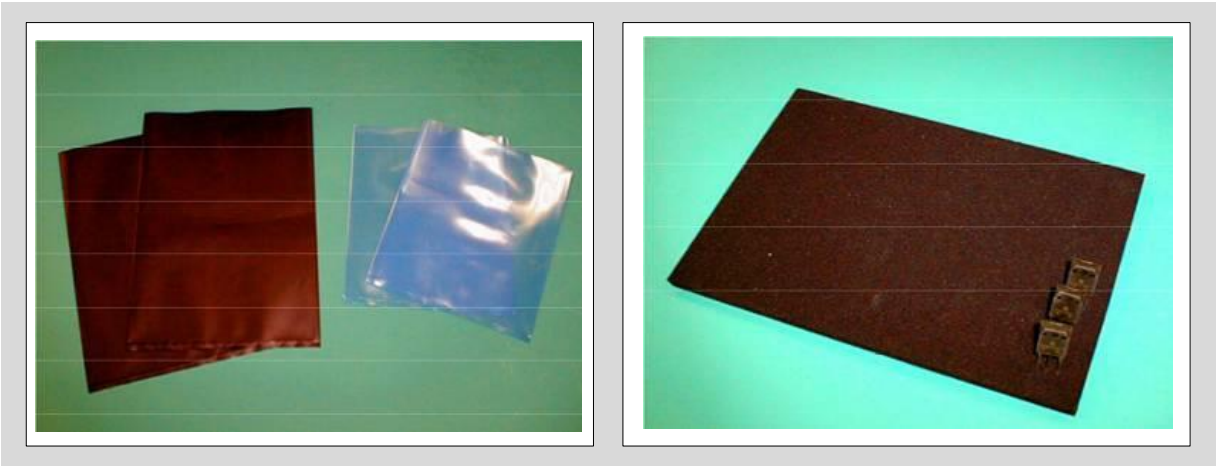


Fig.8-1 Conductive bag (left) and conductive foam (right)

3. Working Environment

(a) The person who handles the IGBT should use ground their body. Wear a wrist strap, copper ring, etc., attach a resistor of approximately 1MΩ, and ground it to prevent electric shock.
(b) At the working environment, lay a conductive floor mat or tablemat, etc. and ground it.
(c) When using measuring devices such as curve tracer, ground the measuring devices as well.
(d) When soldering, ground the solder bath to prevent the leakage voltage from the soldering iron or bath being applied to the IGBT.
(e) Hold the package body so that you do not touch the terminals directly.