Fuji Electric
Innovating Energy Technology

Application Note

3-Level Modules with Authentic RB-IGBT

Version 1.3

Content

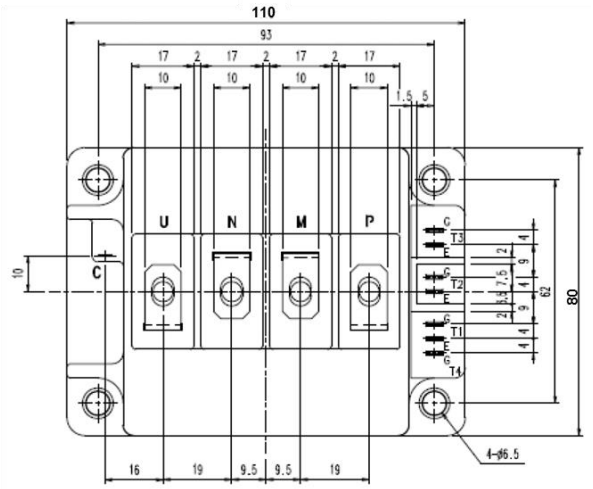
1. Introduction

Due to increase in power consumption, the power conversion efficiency and reduction of power losses in power conversion systems become more and more important. A multi-level topology is one of the most effective configurations in power conversion for DC-link power. A very common solution for improved efficiency regarding to multi-level power converters is the Neutral-Point-Clamped (NPC) 3-level power converter. A 3-level topology allows decreasing switching loss as well as a reduction in size of filter by enhanced spectral performance of output voltage and increase of switching frequency.

Fuji investigated another type of NPC 3-level power converter named advanced NPC (T-type IGBT with RB-IGBT). This generation of power converters utilizes a reverse blocking IGBT (authentic RB-IGBT) for the clamping of output to the neutral point. Besides, the reduction of switching loss, a minimization of filters and low conduction loss could be achieved.
This application note shows the basic function of the authentic RB-IGBT chip and module as well as possible applications for Wind Power, Photovoltaic (PV) and Drives circuit.

2. Basics of T-type IGBT modules

The T-type 3-level module e.g. 4MBi300VG-120R-50 is a one-leg module in M403 package with footprint of 110mm x 80mm with optimized arrangement of the terminals for the construction of NPC 3 level power converters. Figure 2.1 shows the external view in left hand side and the outline drawing of the module in right hand side with main terminals U, N, M, P on the top and auxiliary terminals arranged at the edge.



(1) M403 package (2) Out linedrawing.

Figure 2.1: T-type 3-level module 4MBi300VG-120R-50.

The equivalent circuit in Figure 2.2 demonstrates two main switches T1 and T2 made of V-Series IGBT chips (6th generation, Trench) by Fuji Electric and the clamping switches T3 and T4 (authentic RB-IGBT) which are connected in anti-parallel. Main switch IGBTs are rated with 1200V/300A for instance for the T-type IGBT module 4MBi300VG-120R-50. Due to only half DC-link voltage applied to clamping of output U to the neutral point M, the needed blocking voltage of authentic RB-IGBTs is 600V/300A. To avoid voltage spikes caused by the stray inductance when the device switches, the internal inductance should be kept very low. The measured stray inductance between each pair of main Terminals P and M, M and N, P and N are less than 40nH. This benefit is realized by integrating T1, T2 and the bi-directional switch T3, T4 into a single package.

The new technology of authentic RB-IGBT die enables bi-directional switching capability without additional diode. This feature was desired as well as developed for an improvement of loss. Conventional IGBTs don't have enough reverse blocking capability and therefore a FWD is needed. Otherwise a leakage current flows along the surface of the IGBT die when a reverse voltage is applied between Collector and Emitter, hence the module would be destroyed.

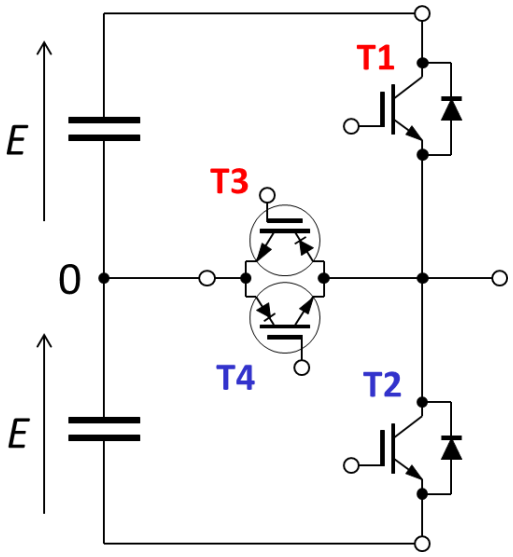


Figure 2.2: Equivalent circuit of T-type IGBTmodule with T1, T2 as main switches and T3, T4 as authentic RB-IGBT switches

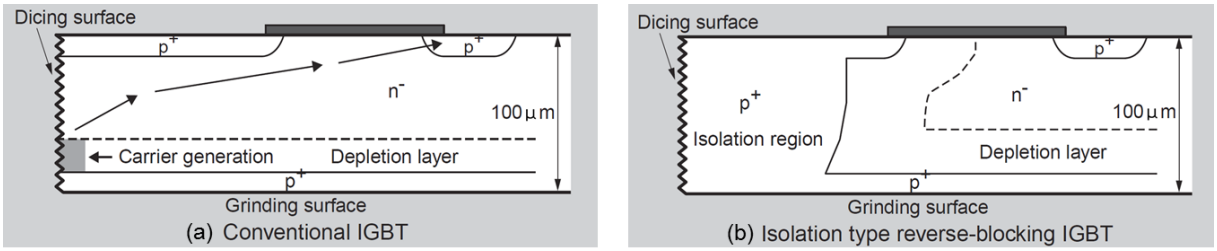
Regarding to the handling of the RB-IGBTs, the chip behaves like a regular IGBT. Hence, for turning-on, a positive voltage of 15V has to be applied between Gate and Emitter control terminals. For turning-off, the negative applied voltage should be applied between -5V and -15V. Following table emphasizes the control signals.

Table 2.1: Suitable turn-on and turn-off V_{GE} for switching mode A.
Switching mode A represents usage of main terminals as half bridge.

RB-IGBT	Turn-on	Turn-off
V_{ge}	+15V	-5V to -15V

3. Characteristics of authentic RB-IGBT

The chief difference between a conventional IGBT and authentic RB-IGBT is the reverse blocking capability. The RB-IGBT structure which belongs to NPT technology was improved by adding a junction isolation region. As shown in Figure 3.1(1), the authentic RB-IGBT structure has a junction isolation region which is missing in the conventional IGBT shown in Figure 3.1(2). The lateral face or dicing face is generated during the chip manufacturing process of cut out from the wafer, some crystal deformations and high-density crystal defects occur.



(1) Conventional chip (2) Authentic RB-IGBT

Figure 3.1: Cross sectional view of IGBTs.

At this lateral face, a continuous generation of charge carriers from the crystal defects is transported by the electric field of the applied negative voltage and lead to a large leakage current demonstrated by black arrows in Figure 3.1.

Therefore, without the junction isolation region the conventional IGBTs don't have enough reverse blocking capability because the leakage current flow through the IGBT chip when reverse voltage is applied between Collector and Emitter. On the other hand, the formed junction isolation in authentic RB-IGBT prevents leakage current flowing through authentic RB-IGBT and enable the reverse blocking capability.

A brief comparison of the characteristics of blocking voltage between conventional IGBT and authentic RB-IGBT is demonstrated in Figure 3.2.

The blue curve represents the authentic RB-IGBT with short circuited Gate-Emitter. The forward and reverse blocking capability is related to the 600V chip with same blocking voltage value. Cyan colored wave form shows an improvement and extended reverse blocking capability of authentic RB-IGBT when positive voltage of 15V is applied between Gate and Emitter. Furthermore a conventional NPT-IGBT also with V_{ge} of +15V is indicated in red. The insufficient capability of reverse blocking of the conventional IGBT is visible.

In spite of the strong distinctions, both IGBT types have almost the same structure of active area. Therefore switching speed and its trade-off curve against Von are similar. When reverse voltage is applied just after forward conduction, authentic RB-IGBT operates like a conventional FWD and reverse recovery behavior resembles each other. Regarding to trade-

off relationship between saturation voltage $V_{CE(sat)}$ and turn-off loss E_{off} for authentic RB-IGBT and conventional IGBT with diode in series, a clear benefit is obvious in Figure 3.3 for a 600V and 100A device at 125°C.

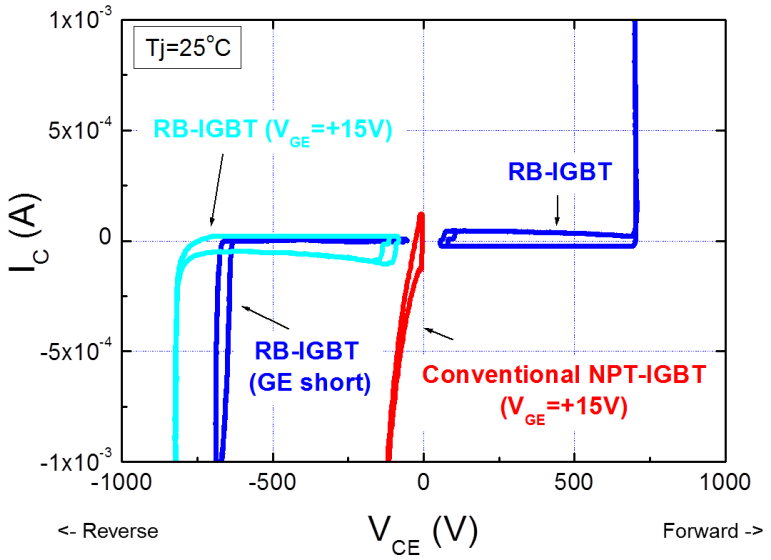


Figure 3.2: Blocking voltage characteristics of conventional IGBT and authentic RB-IGBT.

The turn-off characteristic of authentic RB-IGBT is similar to IGBT with diode.
However, authentic RB-IGBT has much lower $V_{CE(sat)}$ compared to IGBT and diode as a result of no additional diode. This improvement contributes to a minimization of power loss by using RB-IGBT as for a bi-directional switch.

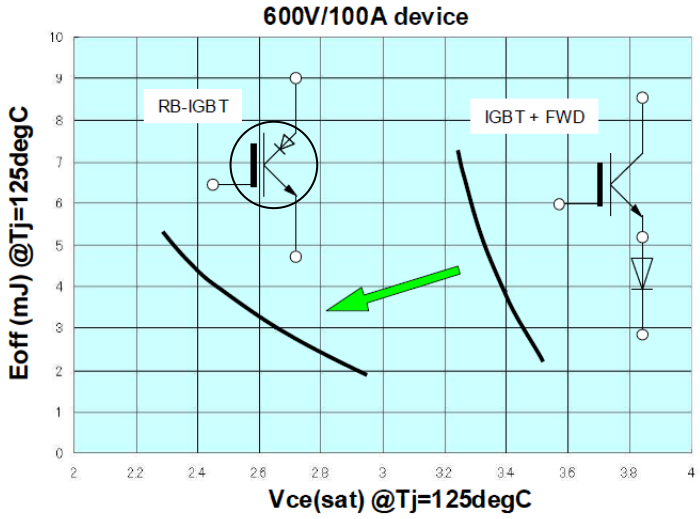


Figure 3.3: Trade-off relationship of authentic RB-IGBT and IGBT + diode.

4. Leakage current inside authentic RB-IGBT

The RB-IGBT does not have an antiparallel diode to prevent conduction of the charge carriers in the negative direction when reverse voltage is applied. The current can flow in negative direction without destroying the authentic RB-IGBT. Consequently, a small leakage current occurs.

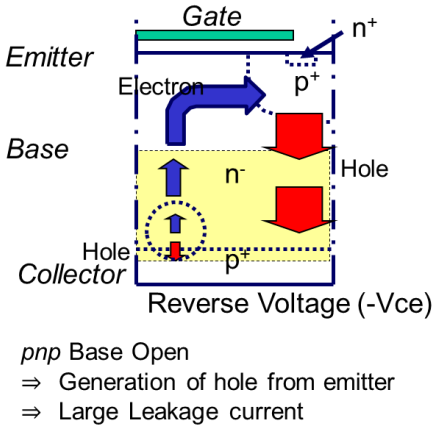
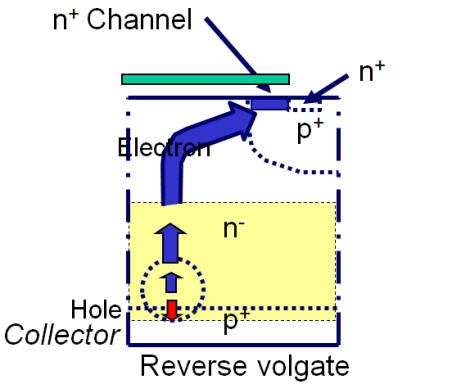


Figure 4.1: Mechanism of generated charge carriers in authentic RB-IGBT when negative voltage is applied.

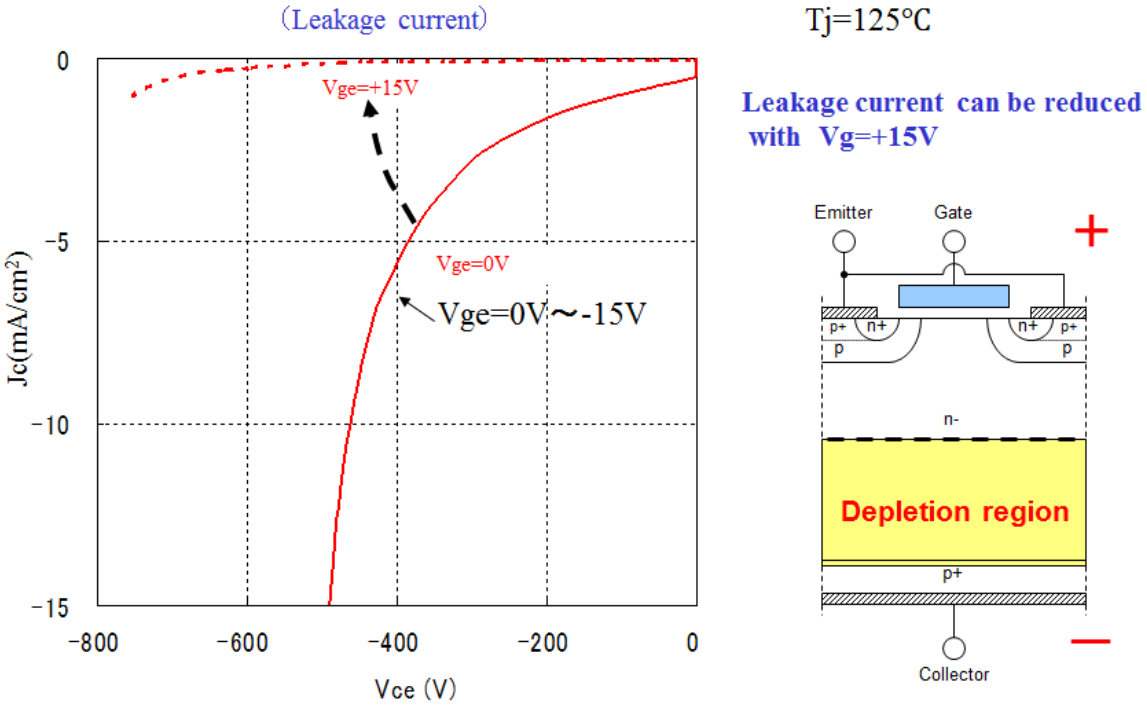
Due to the applied reverse voltage, the holes generation from Emitter to Collector takes place (big red arrows). Additional holes will be created at the other edge of the unit cell between Collector and p+ area. According to the holes generation, electrons flows through the Base into the Emitter and a leakage current occurs.
By applying a positive Gate-Emitter voltage, this leakage current can be reduced as demonstrated in Figure 4.2. As long as V_{ge} = + 15V is applied the authentic RB-IGBT is in ON-state and the generated flow of electrons due to reverse voltage decreases. The positive applied voltage eliminates the generation of holes in the pn crossover and electrons are absorbed into the n+ channel. Only a very small leakage current remains.
For example, T3 is used in the FWD mode which means that T4 switches in commutation with T2. Then T3 should always be in ON-state with V_{ge} of + 15V to keep the leakage current small.



Electron flows the n+ of Emitter
⇒ Not generation of Hole
"pn diode operation"
⇒ Small Leakage current

Figure 4.2: Reduction of charge carriers due to positive Gate-Emitter voltage of + 15V.

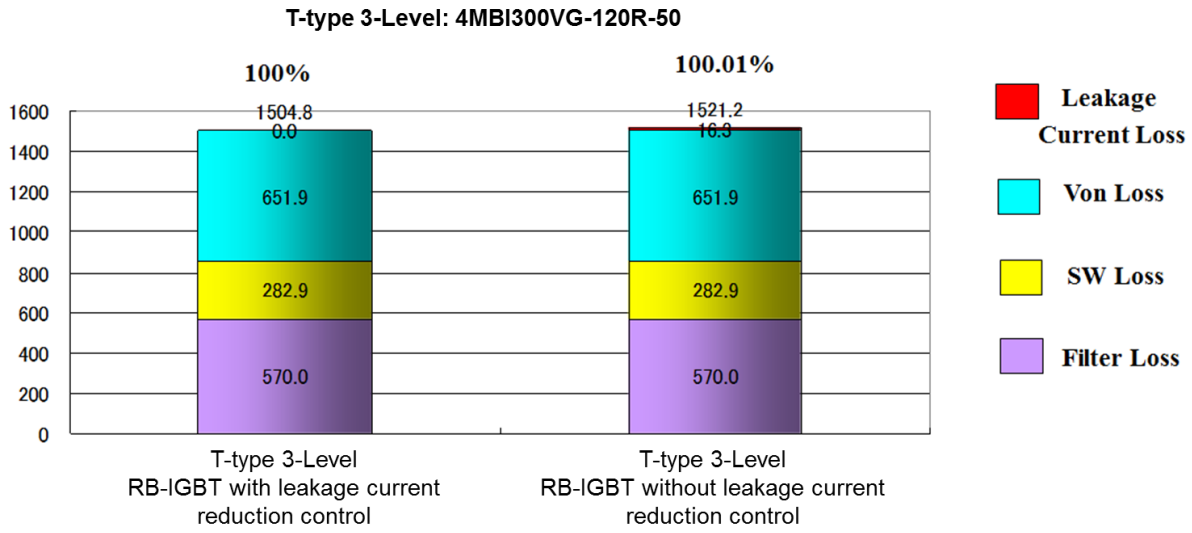
In Figure 4.3 (1), the reduction of charge carriers is demonstrated. The density of charge carriers is less during the ON-state of authentic RB-IGBT than in OFF-state. Figure 4.3 (2) shows the area of depleted charge carriers.



(1) Jc and Vce characteristics (2) Depletion region of charge carriers

Figure 4.3: Leakage current characteristics Effect of ON-state Vge.

The improvement in leakage current loss is shown in Figure 4.4. Without the reduction control of leakage current, the loss will increase by 0,01%. At first, this might sound not as a huge improvement but regarding to leakage current loss over time it is not negligible.



(1) With leakage current control (2) Without leakage current reduction control

Figure 4.4: Loss comparison of PWM Inverter

V_{cc} = 400V, I = 145A, cos(ϕ) = 1,V_{dc} = 330V + 330V,

mulation rate = 0,98, T_j = 125°C, R_g = 8,2/ - 39Ω.

5. Switching time

The switching behavior of the main terminals of T-type IGBT devices is comparable to other V-Series IGBT chips by Fuji Electric. Surely, the switching characteristic is influenced by various parameters as Gate resistances $R_{G(on)}$ and $R_{G(off)}$. However, the four important parameters of switching time are t_r (rise time), t_{on} (turn-on time), t_f (fall time) and t_{off} (turn-off time) which is measured with the circuit shown in Figure 5.1.

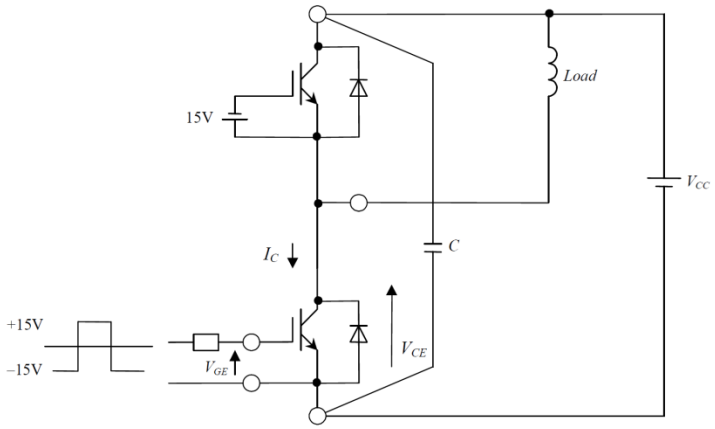


Figure 5.1: Measurement circuit for switching characteristics.

Figure 5.2 defines the switching times during turn-on and turn-off. In order to turn-on the IGBT, the applied Gate-Emitter voltage V_{GE} should be about +/- 15V. The - 15V voltage level

represents the IGBT in OFF-state. After increasing V_{GE} the IGBT starts turn-on as soon as V_{GE} is beyond 0V. When V_{GE} reaches the threshold voltage $V_{GE(th)}$, the IGBT starts to conduct and continuous Collector current I_C rises at the beginning of t_r. The reverse recovery current of FWD determines the over shoot current peak which turns into the Collector current during reverse recovery time t_{rr}. Then the IGBT is now in ON-state.

Regarding to the turn-off of IGBT from ON-state, the voltage applied between Gate and Emitter (V_{GE}) should be set to - 15V. At 90% of positive V_{GE}, the IGBT starts turn-off. When VCE is increased to VCC level, continuous Collector current starts to decrease. t_f is defined from 90% until 10% of I_C. After that the IGBT is in OFF-state.

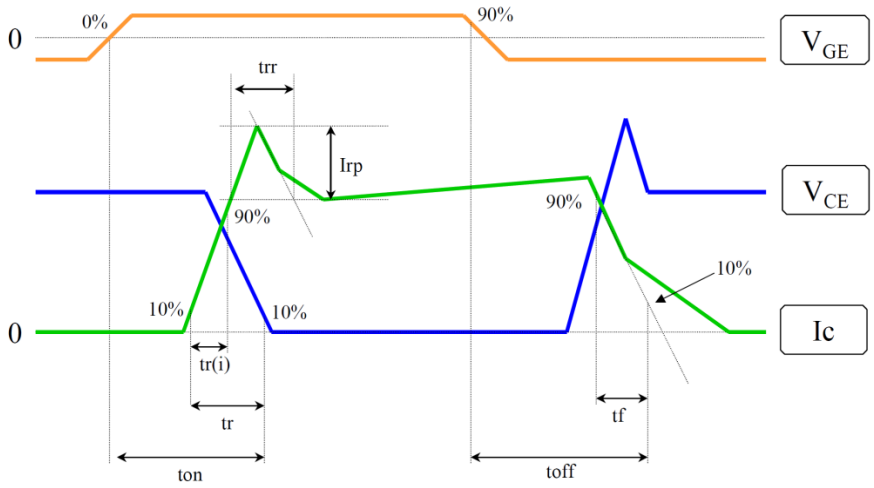


Figure 5.2: Definition of switching times.

The following table gives an overview about turn-on and turn-off time of main terminal switch with $R_{G(on)}$ = 10Ω and $R_{G(off)}$ = 1Ω.

Table 5.1: Turn-on and turn-off time for switching mode A. Switching mode A represents usage of a 3-Level operation for T1 and T2 with the load connected to M - U.

Turn-on time	t_{on}	SW mode: A	–	0,75	1,30	µs
	t_r	V_{cc} = 400V	–	0,45	0,80	
	t_r(i)	I_c = 300A	–	0,15	–	
Turn-off time	t_{off}	V_{ge} = ± 15V	–	0,60	1,00	
	t_f	R_g = +10 / -1Ω	–	0,10	0,35	

6. Dead time

The dead time can easy be calculated as following equation.

$$t_{dead} = t_{off,max} - t_{d(on),min}$$

Where $t_{off,max}$ represents the maximum turn-off time of an IGBT, and $t_{d(on),min}$ represents the minimum turn-on delay time. The value of the maximum turn-off time $t_{off,max}$ can be taken from that datasheet. The turn-on delay time $t_{d(on),min}$ is calculated by the difference of the turn-on time and rise time (t_{on} - t_r).

Switching times for T3/T4:

Table 6.2: Turn-on and turn-off time for switching mode B.

Turn-on time	t_{on}	SW mode: B	–	0,45	1,05	µs
	t_r	V_{cc} = 400V	–	0,27	0,53	
	t_r(i)	I_c = 300A	–	0,12	–	
Turn-off time	t_{off}	V_{ge} = ± 15V	–	1,32	3,00	
	t_f	R_g = +10 / -1Ω	–	0,11	0,35	

Switching mode B represents usage of a 3-Level operation for T3 and T4 with the load connected to P-U or U-N.

Hence, the dead time between T3/T4 and T1/T2 is calculated as follows

$$t_{off,max} = 3{,}00\mu s \quad of\ T3/T4$$
$$t_{d(on),min} = t_{on} - t_r = 0{,}75\mu s - 0{,}45\mu s = 0{,}3\mu s \quad of\ T1/T2$$
$$t_{dead} = t_{off,max} - t_{d(on),min} = 3{,}00\mu s - 0{,}3\mu s = 2{,}7\mu s$$

7. Switching mode

In total there are 2 different switching modes available the for Fuji Electric's 3-level modules. The circuit diagram with DC-link voltage is shown in Figure 7.1.

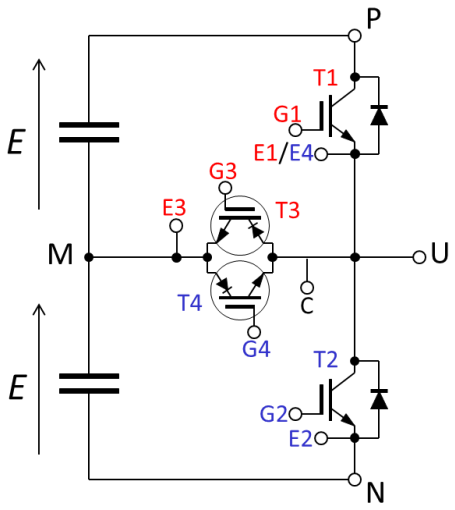


Figure 7.1: Circuit diagram of T-type 3 level module using authentic RB-IGBT with DC link voltage.

Table 7.1 demonstrates an overview of operating switches in dependency of chosen switching mode. The ON-state of a switch means a bias Gate voltage level of + 15V every time. Contrary the OFF-state represents a reverse bias Gate voltage level of - 15V. When a switch is declared in SW-state then the IGBT is connected to the drive circuit and gets an input Gate signal.

Table 7.1: Switching mode A and B of T-type 3 level module using authentic RB-IGBT presented.

SW Mode	Load L	T1	T2	T3	T4
A	M – U	SW	OFF	OFF	ON
	M – U	OFF	SW	ON	OFF
B	P – U	OFF	OFF	SW	ON
	U – N	OFF	OFF	ON	SW

SW: Connection to drive circuit and input gate signal
ON: Bias voltage of gate + 15V
OFF: Bias voltage of gate - 15V
$V_{cc1} = 2 \cdot V_{cc}$

A-Mode:

The A-Mode is used in the case that the load is clamped between M and U. Here, T1 switches while T3 is OFF and T4 is ON which again means that T4 behaves like a diode. T2 is OFF in this switching mode. In the inverse case T3 is ON while T4 is OFF and T2 is now switching. T1 is in OFF-state the whole time period.

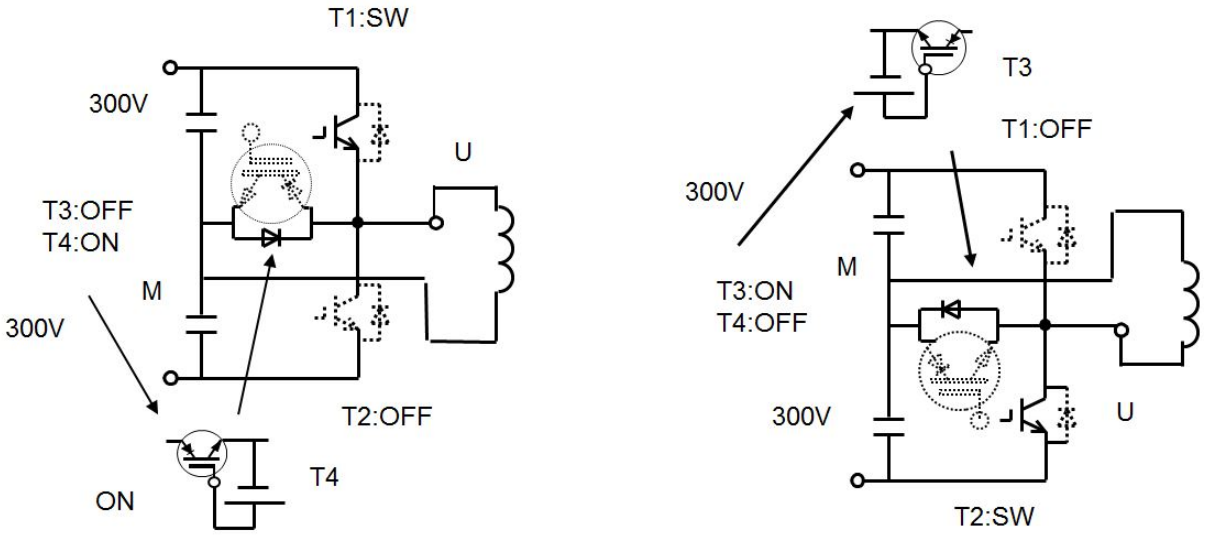


Figure 7.2: Switching mode A. Lines show working devices.
Dotted lines are devices in OFF-state.

B-Mode:

In mode B, one of the authentic RB-IGBTs is switching during the other is in ON-state. Consider T3 switches then T4 is used as FWD. In order to keep the leakage current inside of T4 as low as possible T4 has to be in On-state. In the first case the load is clamped between U and P. T3 switches while T4 is in ON-state and acts like a FWD as shown in Figure 7.3. It even demonstrates the case of clamped load between U and N where T4 switches when T3 is ON. Unused devices are marked with dotted lines.

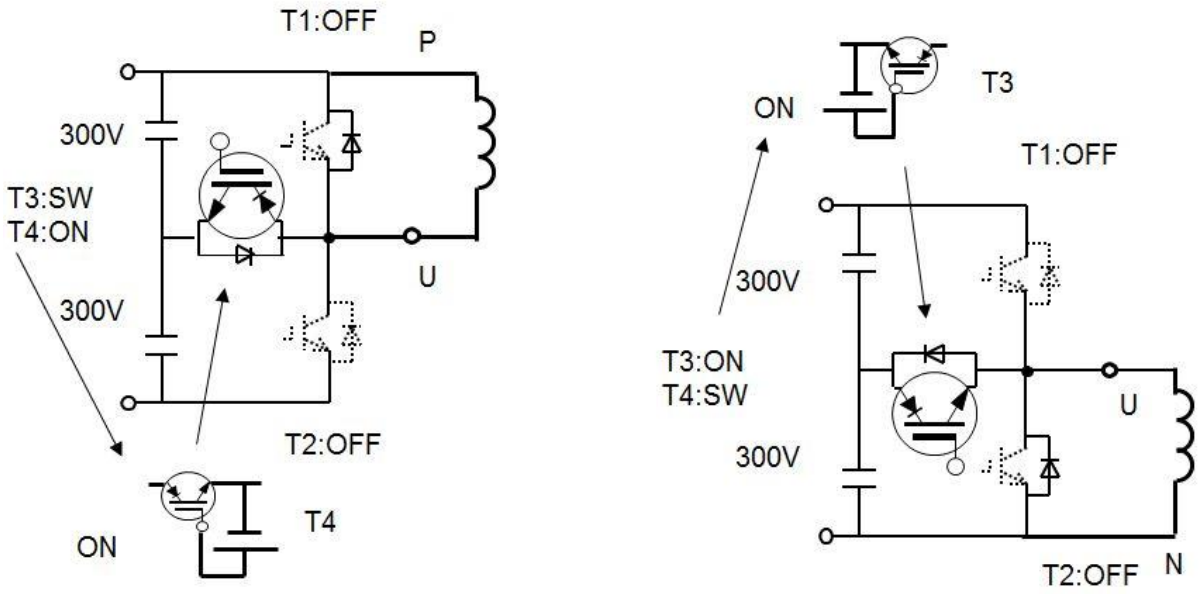
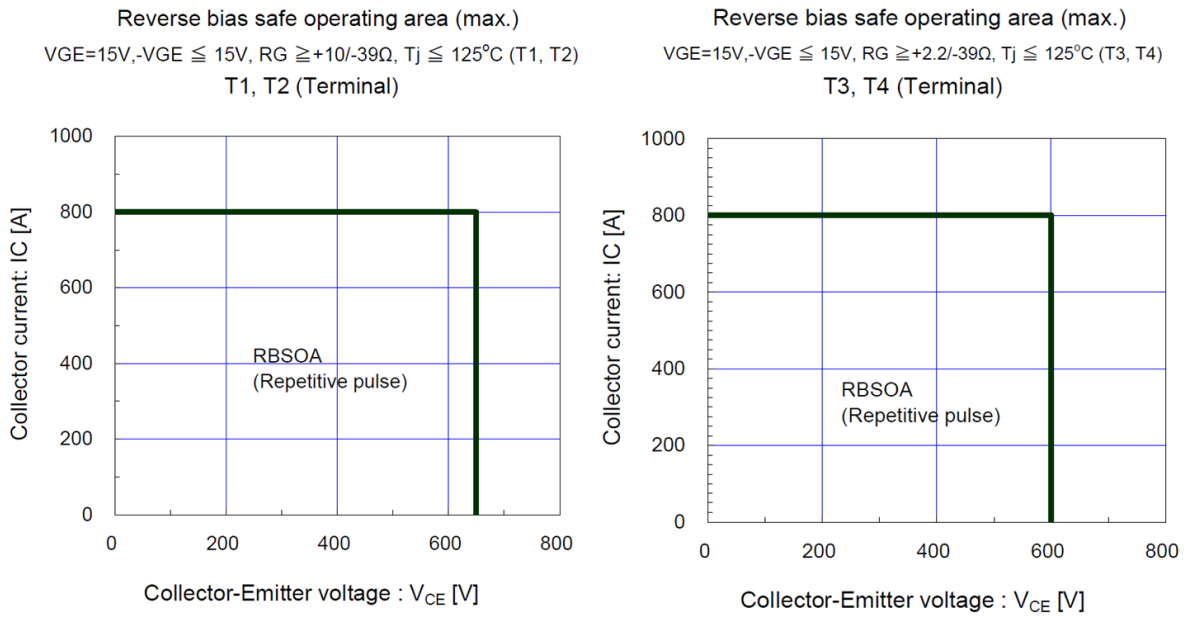


Figure 7.3: Switching mode B. Lines show working devices.
Dotted lines are devices in OFF-state.

8. RBSOA and SCSOA behavior (400A/600V module)

Safe operating area (SOA) is the voltage and current condition in which a power semiconductor device can be expected to operate without self-damage. The safe area refers to the area under the curve in the shown figures below. It is determined by V_{CE} and I_C.



(1) T1,T2 (2) T3,T4

Figure 8.1: Reverse bias safe operating area (RBSOA) and short circuit safe operating area for 4MBi400VG-060R-50. $+V_{GE}$ = 15V, - V_{GE} = - 15V. R_G is the recommended value of datasheet, T_j = 125°C.

In case of a turn-off of IGBT, I_C is decreased and V_{CE} is increased. The reverse bias safe operating area defines the locus of V_{CE} and I_C waveforms so that breakdown of the IGBT or diode will not occur. The solid line in Figure 8.1 represents the RBSOA for the main switches of 4MBi400VG-060R-50.

In the event of a turn-off from short circuit (non-repetitive) condition, the IGBT has a SOA defined by V_{CE} and I_C which is named SCSOA. This condition is only valid for a short pulse time which is declared in Table 8.1.

Table 8.1: Short-circuit withstand capability for T1, T2 and T3, T4.

	Condition				
	Pulse width min $[\mu s]$	V_{cc} $[V]$	$+V_{ge}$ $[V]$	R_g	T_j [°C]
T1,T2	9	400	15	Recommended value	125
T3,T4	10	200	15	Recommended value	125

9. Switching pulse

The Figure 9.1 below demonstrates the definition of a 3 Level switching pattern. Using the T-type configuration the 3 different levels of energies are realized by a positive, zero and negative level. The output voltage or load is connected to the neutral point that is indicated by the ground connection.

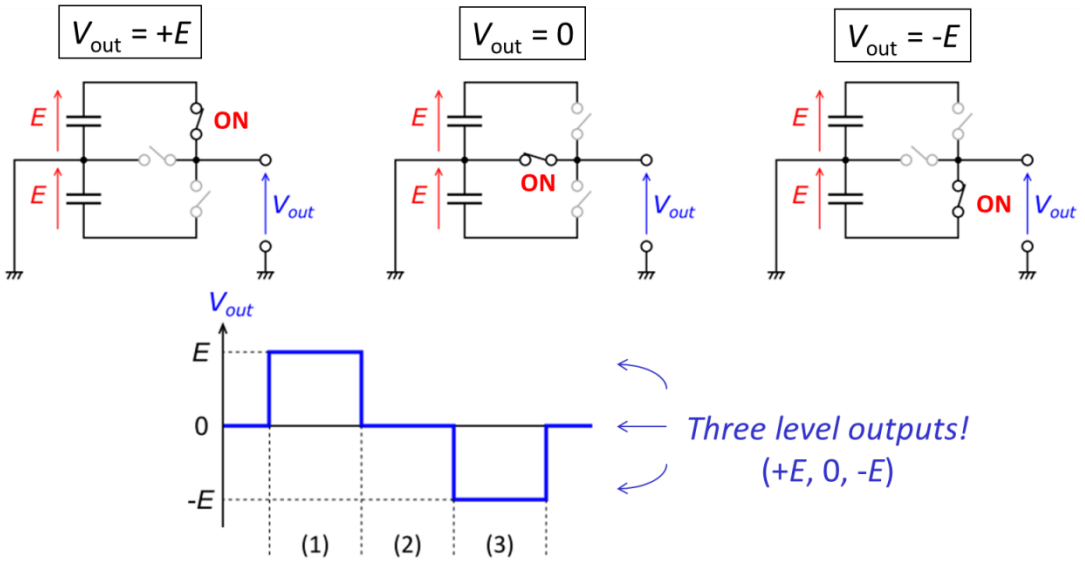


Figure 9.1: 3-Level pulse waveform for a connected load between phase out and neutral point clamp.

The pulse pattern of the output waveform using a 3-level topology is shown in Figure 9.2

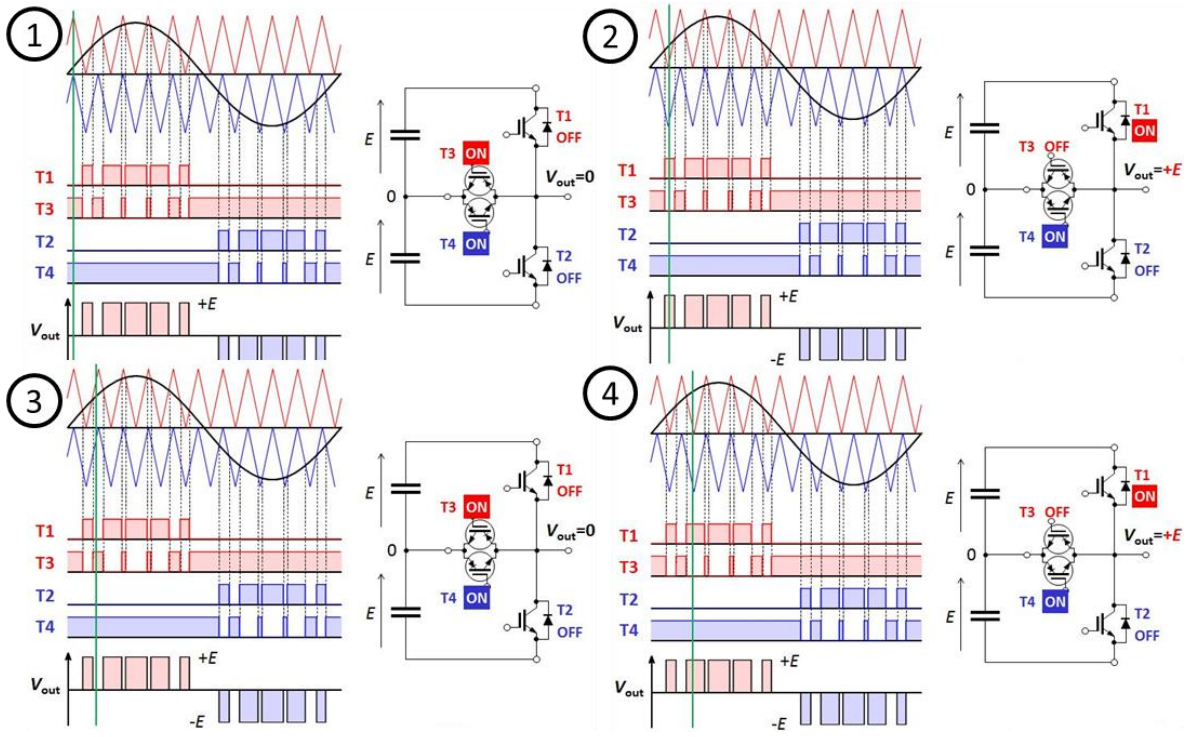


Figure 9.2: Pulse output waveform between output and neutral point clamp 0.

Enumeration from 1 to 4 explains what kind of pulse pattern is present at a certain output voltage level. In order to keep it simple only the first 4 patterns are shown. Subsequent pattern can easily be determined.

10. 3-Level topologies

Fuji Electric's authentic RB-IGBT is not the only way to create a 3-level topology. There are several other topologies to realize a 3-level configuration. Two well-known topologies which are called I-type and T-type reach comparable advantages to Fuji's 3-level solution.

I-type:

I-type uses four IGBT chips which are aligned in a vertical way. In this case, T1 and T4 are called outer switches due to their localization of the circuit. On the other hand T2 and T3 are the inner switches. It is possible to distinguish these two types of switches because of the diodes clamped between T1, T2 as well as T3, T4. The advantage of the topology is that the chips only have to block half of applied voltage by reason of two IGBT chips in series. Additionally, the breakdown voltage V_{CES} of all switches (T1 to T4) are only half of a 2-level inverter which leads to less loss. The disadvantage of the topology is the usage of many switches and therefore many components. The ON-state voltage V_{ON} increases as a result of all IGBTs in series. Every single IGBT ON-state loss contributes to the total ON-state loss and leads to higher loss than in a 2-level inverter.

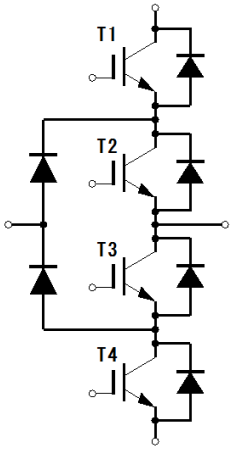


Figure 10.1: I-type topology.

T-type:

This topology has less components than T-type and looks quite similar to Fuji Electric's T-type IGBT solution. Instead of authentic RB-IGBT this topology uses two IGBT chips and two diodes. One IGBT is connected in series with a diode in blocking direction and connected

antiparallel with the other IGBT and diode which is a common-Collector configuration in the middle clamp. The merit of this topology is the reduction of V_{ON} loss because only a single IGBT T1 and T2 in series and less switches. Therefore one IGBT chips has to block the full voltage.
Consequential the chip needs to be higher rated and implies higher loss. T1 and T2 have the same breakdown voltage as the 2-level half bridge without an advantage.

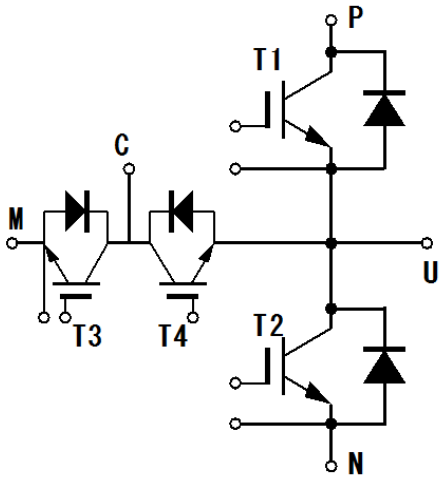


Figure 10.2: T-type topology.

T-type with RB-IGBT:

The T-type IGBT solution by Fuji Electric has the same advantages as the regular T-type con-figuration according to number of components and low V_{ON} loss due to single switch in series. The additional merit of this topology is even lower loss by reason of the usage of authentic RB-IGBT. A single authentic RB-IGBT can substitute an IGBT and diode in series which leads to a miniaturization and less loss. The obvious disadvantage in T-type is the necessity of full blocking voltage capability of main switches and breakdown voltage of T1, T2 as in 2-level topologies.

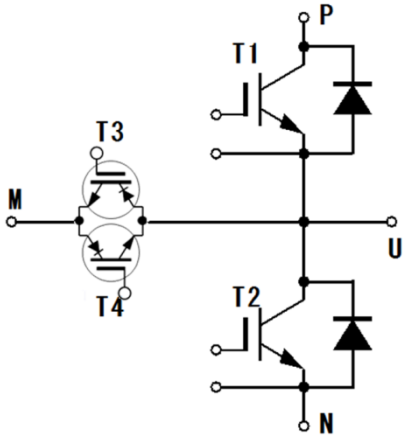
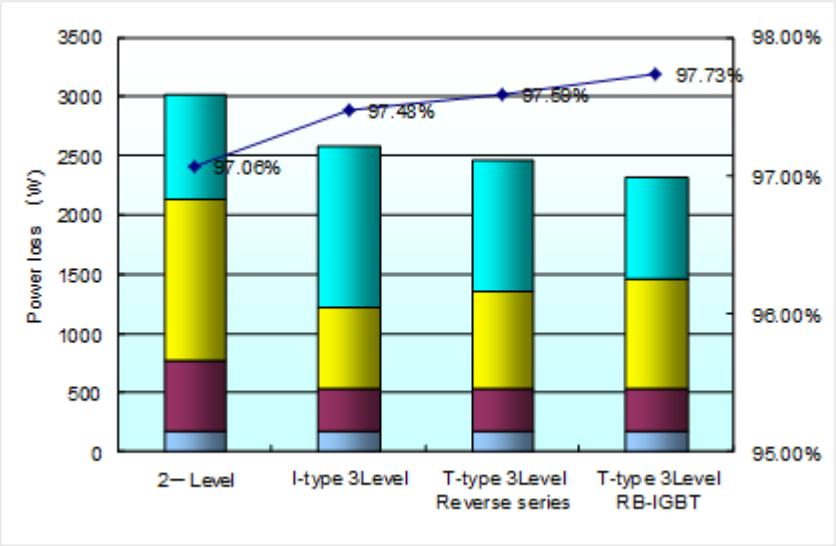


Figure 10.3: T-type RB-IGBT topology.

11. Loss comparison

The advantage of a 3-level inverter topology is quite obvious in the comparison of loss shown in Figure 11.1. The conditions for inverter power loss calculation (f_C = 10kHz) are same for every topology. The 2-level inverter acts as reference for the 3-level topologies. Clearly, all 3-level configurations have less power loss due to the remarkable reduction of switching loss (yellow bar). Fixed loss is kept constant and contains for instance conduction loss of the system. Reduction of filter loss is the consequent of better sinusoidal output waveform hence less needed filter. In precisely, the V_{ON} loss of 2-level inverter is smaller compared to I-type 3-level or A- T-type 3-level with reverse series by the reason of only one IGBT switch in 2-level configuration. The series connection of two IGBTs as in I-type 3-level leads to lower switching loss. In case of T-type 3-level with RB-IGBT, IGBT V_{ON} loss is smaller than I-type 3-level, even the topology uses 4 switches with FWD in total. On the contrary, T-type 3level with RB-IGBT uses two IGBT and two authentic RB-IGBT which leads to less V_{ON} loss. Remarkable is that the efficiency of T-type 3-level with RB-IGBT is 97,73% and T-type 3-level with reverse series is 97,59%. This improvement of 0,14% is significant for the save of energy over time when the inverter operates several years.



Vdc=660V(330V;330V), Io=145A, cos θ =1,fc=10kHz,Vo=400Vac

Figure 11.1: Loss comparison of different topologies. 2-level inverter provides the basis for the other topologies.

Additionally, big benefit can be seen regarding to the device loss in dependence on the switching frequency. Up to 30kHz the A-NPC 3-level (T-type) topology has lower total loss than other topologies. This is demonstrated in Figure 11.2.

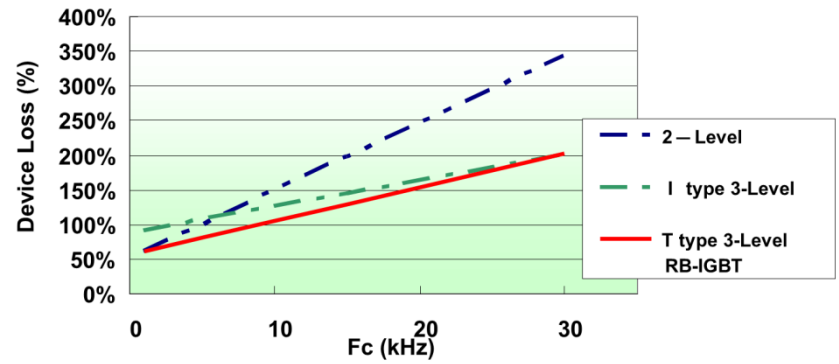


Figure 11.2: Loss comparison of different topologies in dependence on the switching frequency.

12. Connecting to DC-link

The best way of mounting busbars to an IGBT module is to keep the busbars parallel to each other and very close together. For example, just an isolation laminate should distinguish the busbars from each other. Figure 12.1 gives an idea how to connect busbars.

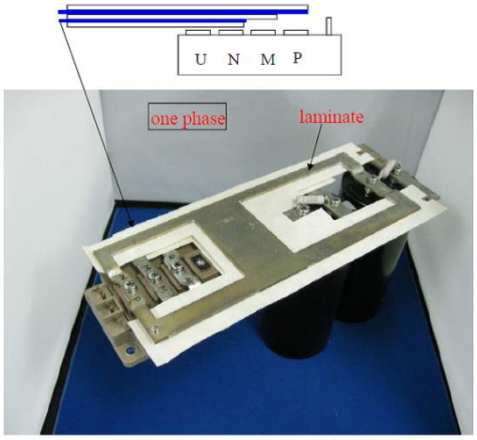


Figure 12.1: Busbars connection to T-type IGBT module with the schematic drawing above, where blue bars represent the isolation laminate and white ones represent the busbar metal layers.

The schematic drawing in Figure 12.1 shows the array of three metal layers (white bars) and two layers of isolation laminate (blue bars), and gives an example how to connect the busbars to the power module. The lowest layer is a metal plate connected to the N point of the module. The following stack of layers contains isolation laminate, metal plate which is connected to M point, isolation laminate and P point connection to the module again by a metal plate. In this figure, the phase out terminal is designed for a single phase measurement setup. This setup can easily be extended to a setup with a 3-phase circuit (fig. 12.2):

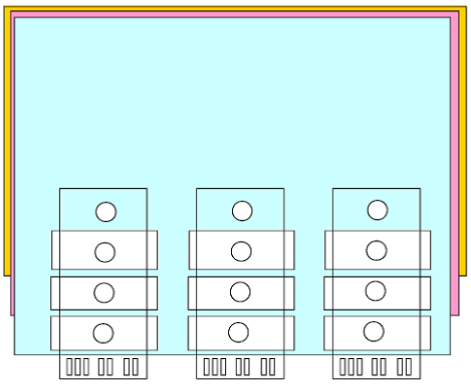


Figure 12.2: 3-phase constellation of T-type IGBT module.

This is only example how to connect the capacitors to the 3-level module. Own solutions can be realized with respect to the needed shortest way of terminals to the busbars.

13. Switching waveforms of authentic RB-IGBT

The authentic RB-IGBT die has in principal two modes, the switching mode and the recovery mode. This chapter describes examples of waveforms, and measurement circuit is shown in Figure 13.1. This circuit measures the switching behavior of T3 (authentic RB-IGBT) and the recovery behavior of the diode of T1. Same circuit can be used to measure switching of T1 and the recovery of T4 (authentic RB-IGBT). For the capturing of the switching waveforms, the temperature was kept constant at room temperature (25°C). The half of applied DC-link voltage was 400V which is the potential between M and P terminal. The nominal current was always 300A. Additionally, the capacitance of snubber capacitor was 1,84µF and the wiring inductance was 34nH.

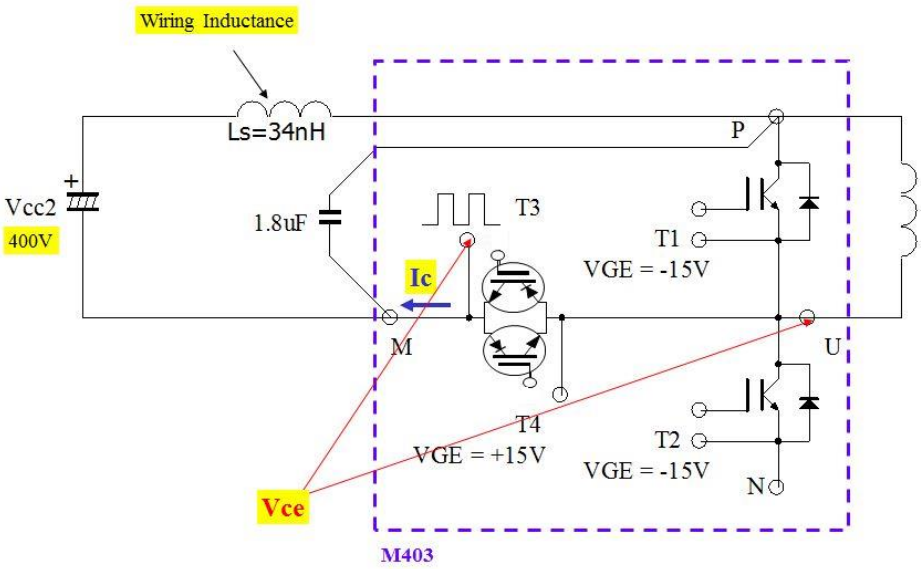


Figure 13.1: Circuit of measurement for switching of T3 and diode of T1.

Switching of T3 and FWD of T1 in recovery mode:

In this case, the ON Gate resistance was 8,2Ω and the OFF gate resistance was 39Ω. For the switching of T3, the Gate-Emitter voltage alternates between + 15V and - 15V,and T4 is steady ON-state (V_{GE}= + 15V).

The turn-off of authentic RB-IGBT should be relatively slow. This conclusion is based on the realistic Gate-Emitter bias voltage which makes almost no remarkable oscillation of V_{CE}. Also even the overvoltage of roughly 200V occurred, but still in the voltage blocking capability of authentic RB-IGBT. Consequently, the Collector current could be very fast fall time and no tail current which makes turn-off switching loss smaller.

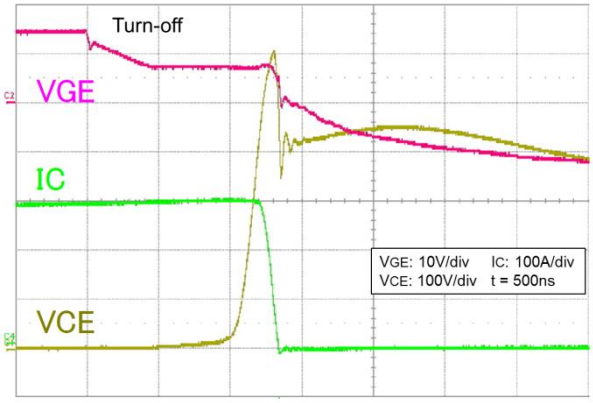


Figure 13.2: Turn-off waveforms of authentic RB-IGBT.

Turn-on of authentic RB-IGBT is faster than the turn-off as shown in Figure 13.3. Approximately 190A of reverse recovery current is visible in the current peak which leads to only a small bump on V_{GE} and makes turn-on switching loss smaller.

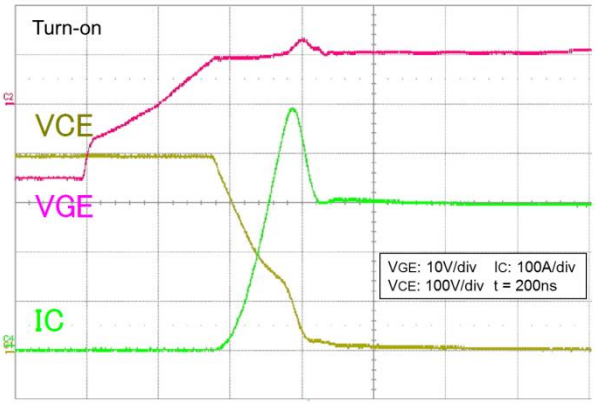


Figure 13.3: Turn-on waveforms of authentic RB-IGBT.

Switching of T1 and T4 in recovery mode:

During turn-on of Main switch IGBT T1 with 10Ω of $R_{G(on)}$, T4 authentic RB-IGBT performs reverse recovery from its ON-state, like as diode. The reverse recovery waveforms are shown in Figure 13.4. Wiring inductance and snubber capacitor are rated in before as 34nH and 1,84µF. The smaller enough reverse recovery current and the lower enough voltage spike could be obtained. So that the reverse recovery loss could be smaller.

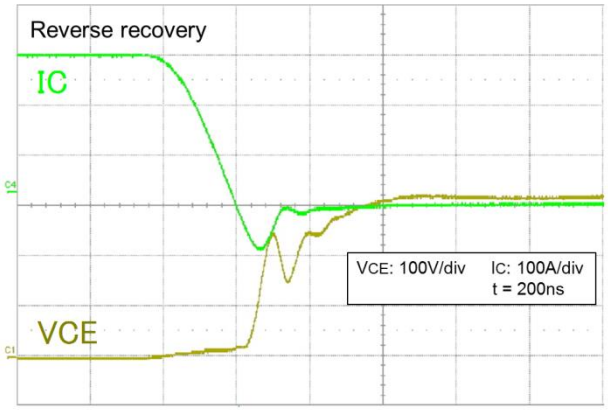


Figure 13.4: Reverse recovery waveforms of authentic RB-IGBT.

Short circuit behavior for authentic RB-IGBT:

Figure 13.5 shows the short circuit waveforms of the authentic RB-IGBT as for 10µs of short circuit withstand capability. This test was done at 125°C with a 400V of DC-link voltage. The pulse of V_{GE} applied was + 15V and 0V for turn-off. The Gate resistances were + 8,2Ω and -100Ω. As Figure 13.5 demonstrates the RB-IGBT is able to withstand such a short circuit condition for 10µs.

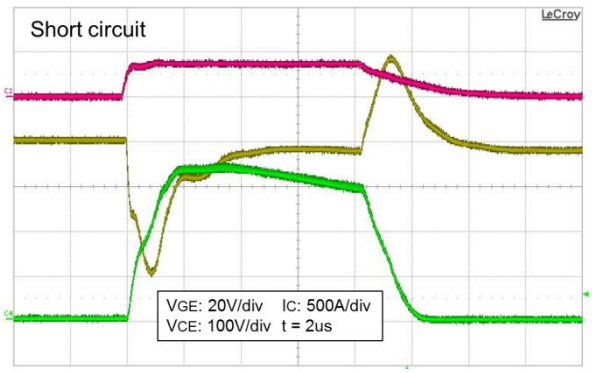


Figure 13.5: Short circuit behavior of authentic RB-IGBT. Test conditions: T_j = 125°C, V_{CE} = 400V, V_{GE} = + 15/- 0V, R_G = + 8.2/- 100Ω, snubber = 0.67µF.

14. Paralleling 3-level IGBT module (M403)

In order to achieve higher current output from IGBT modules, parallel connection of the devices is necessary. According to the parallel connection of the power modules, it also leads to a paralleling of all IGBTs and Diodes. Additionally, it is very important to setup the parallel connection in a symmetric way which is required to take care about the static and dynamic balancing parameters. Table 14.1 shows the parameters that influence the balancing (current sharing) of IGBT modules:

Table 14.1: Influencing factors of paralleling power modules.

Parameter	Influence on	
IGBT		
$V_{CE(sat)} = f(I_C, V_{GE}, T_j)$	static symmetry	
$I_C = f(V_{GE}, T_j)$		dynamic symmetry
$V_{GE(th)}$		dynamic symmetry
IGBT driver		
$t_{on}, t_{off}, t_r, t_f$		dynamic symmetry
Commutation loop		
Stray inductance (internal + external)	static symmetry	dynamic symmetry

All the above mentioned factors have an influence on the current sharing between the modules. Ignoring the factors will lead to a current imbalance between the modules, which mean that one module carries more current than the other. Therefore, current derating has to be taken into account while designing the parallel connection. In other words, paralleling two 300A rated modules can achieve around 576A to 540A (with considered derating of 4% to 10%) of current rating equivalently.

Connecting 2 modules in parallel:

For paralleling the M403 package to achieve higher output currents, those should be connected as shown in Figure 14.1. In order to realize a 3-phase inverter as seen in the center of Figure 14.1 with paralleled power modules, each module faces the other with the opposite side of control-terminals. The DC-Link voltage capacitors are located in the middle of the inverter. After mounting the bus bars to P, M and N, it is recommended to use snubber-capacitors on top of the module shown in Figure 14.1.

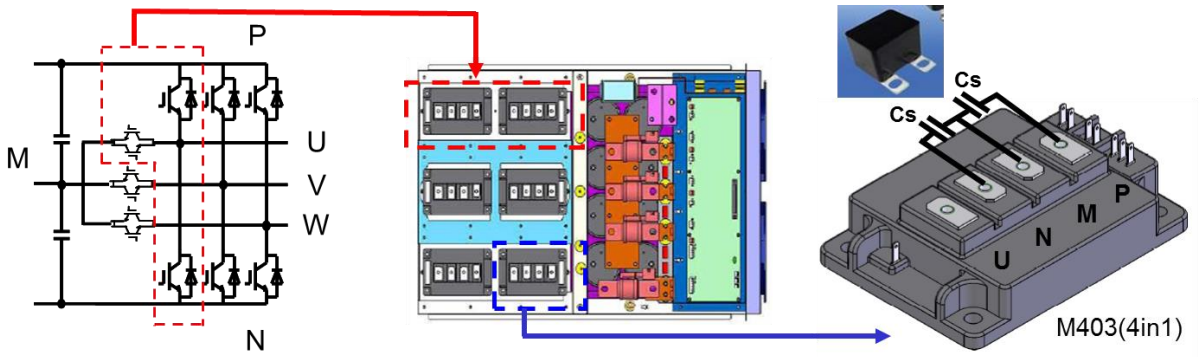


Figure 14.1: Basic scheme of 3-phase inverter with paralleled power modules.

How to design the bus bars for such an inverter is obvious in Figure 14.2 where three metal plates build the positive, middle and negative connection to the capacitors. Remarkable is the pattern of these metal plates. Every single metal plate has another stamp design according to the location of the main terminals of the module. Insulation foil between the plates prevents a short circuit in the inverter even the plates are piled up closely.

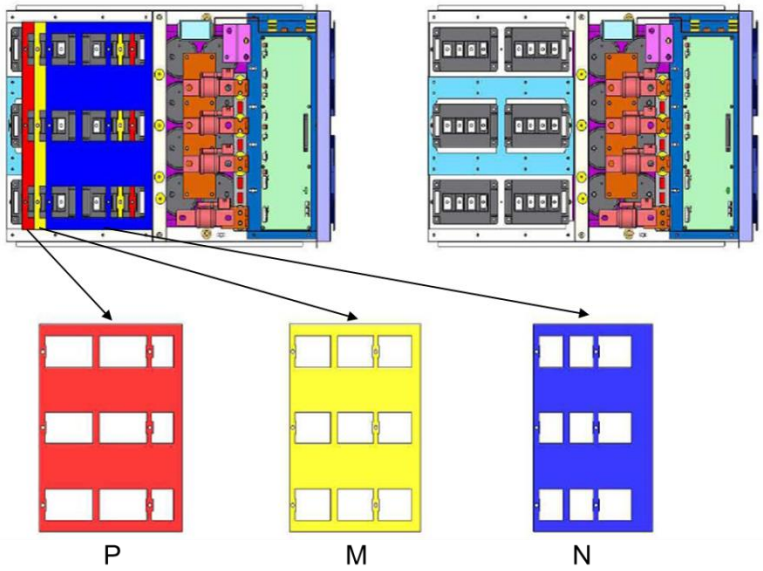


Figure 14.2: Basic scheme of 3-phase inverter with paralleled power modules and busbar design.

Waveforms of two paralleled modules:

The following pictures show up the highly symmetric current waveform of two modules in parallel. The above mentioned parameters which lead to a symmetric current distribution have been taken into account during the design of the inverter. The main and most important parameters are listed below:

- Static parameters
- Dynamic parameters
- Same batch of IGBT/FWD chips
- Planar bus bars design

- Symmetric bus bars design

With respect to the above mentioned parameters, highly symmetric output currents can be achieved. Figure 14.3 demonstrates the current sharing of a 150kW inverter with 5kHz of switching frequency in operation mode. The current has been measured at T1 which is the upper IGBT of the main leg.

Channel 1 (yellow) represents the Gate-Emitter voltage of the switching IGBT. Channel 2 and 3 (red and blue) stand for the Collector current of each paralleled module. The DC-Link voltage is shown by Channel 4 (green).

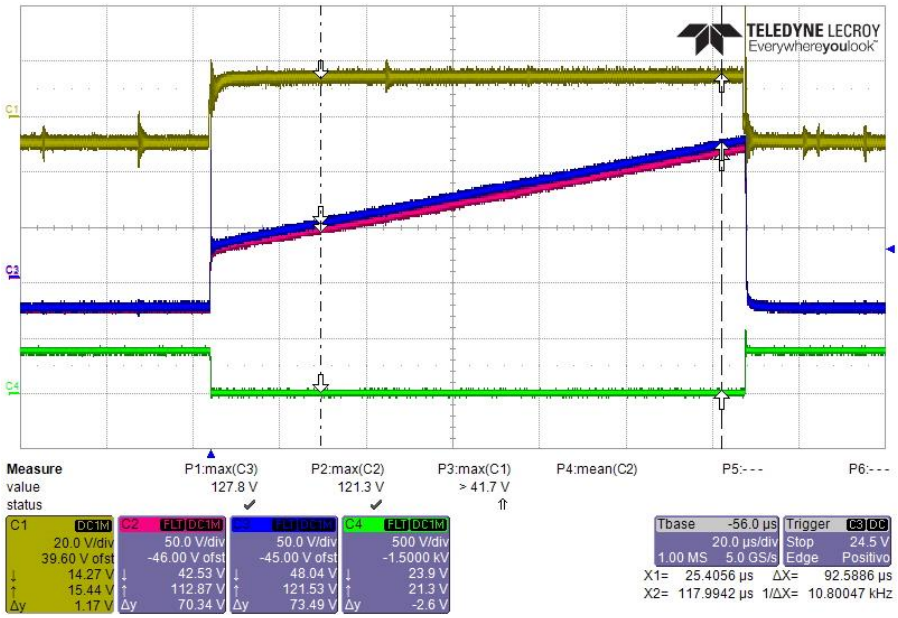


Figure 14.3: Waveform of T1 of a 150kW inverter.

Overall, it is very obvious that the current (red and blue) through both modules is highly symmetric and almost identical. The over-shoot current at turn-on is lower than half of the rated current of the module 4MBI300VG-120R-50. Hence, there is no problem to concern about the current peak.

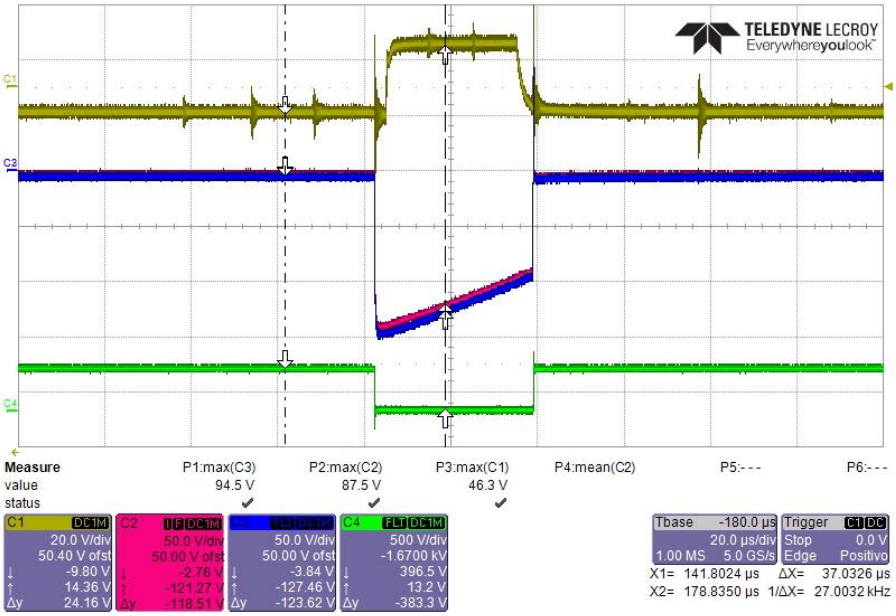


Figure 14.4: Waveform of T4 of a 150kW inverter.

Figure 14.4 demonstrates the waveform of T4 in operation of a 150kW inverter. As visible the current sharing does not differ from one module to the other. The parallel currents are flown in the same way and almost no discrepancy is obvious.

15. Driving the 4MBI300VG-120R-50

Driving the 3-Level module seems difficult at the beginning. The following short description shows how to connect the auxiliary terminals from the power module to the Gate driver.

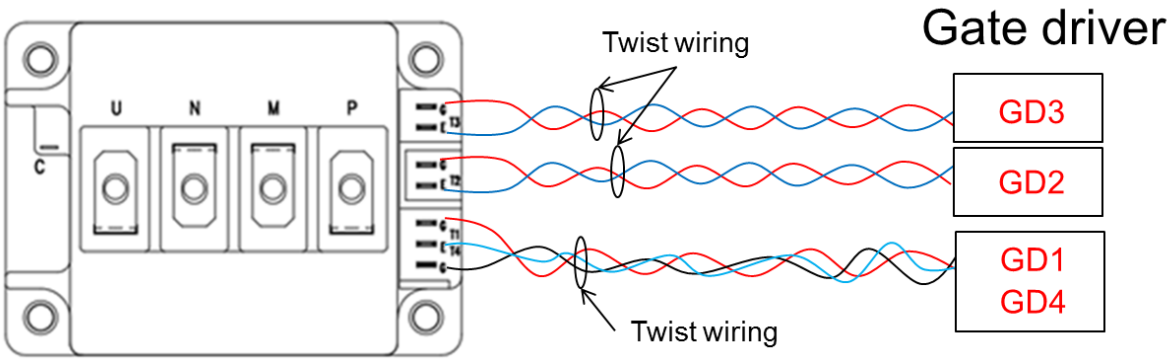


Figure 15.1: Auxiliary wiring of Gate driver to power module.

The auxiliary Emitter terminal of T1 and T4 has the same potential hence the Gate driver GD1 and GD4 can use the common Emitter wiring and common power supply. In total three Gate drive interfaces are necessary to driver the 3-Level module shown in Figure 15.1.

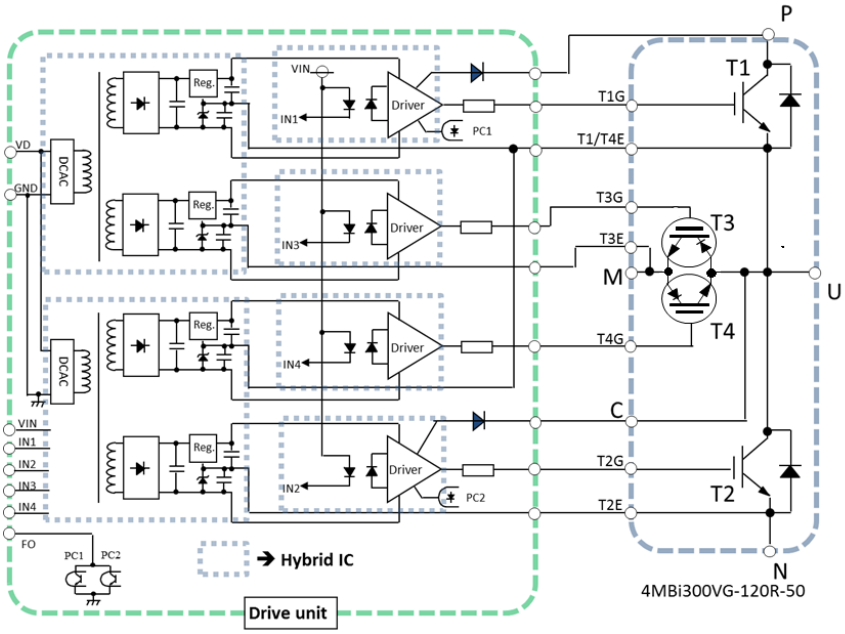


Figure 15.2: Example of Gate drive circuit (block diagram).

In the following, an example of how to setup a driver for a single M403 RB-IGBT module is shown. The driving circuit contains two 2in1 DC-DC converter and four driver units to drive the IGBTs and RB-IGBTs. While the two upper driver units are responsible for T1 and T3, the lower driver units handle T4 and T2. This is demonstrated in Figure 15.3.

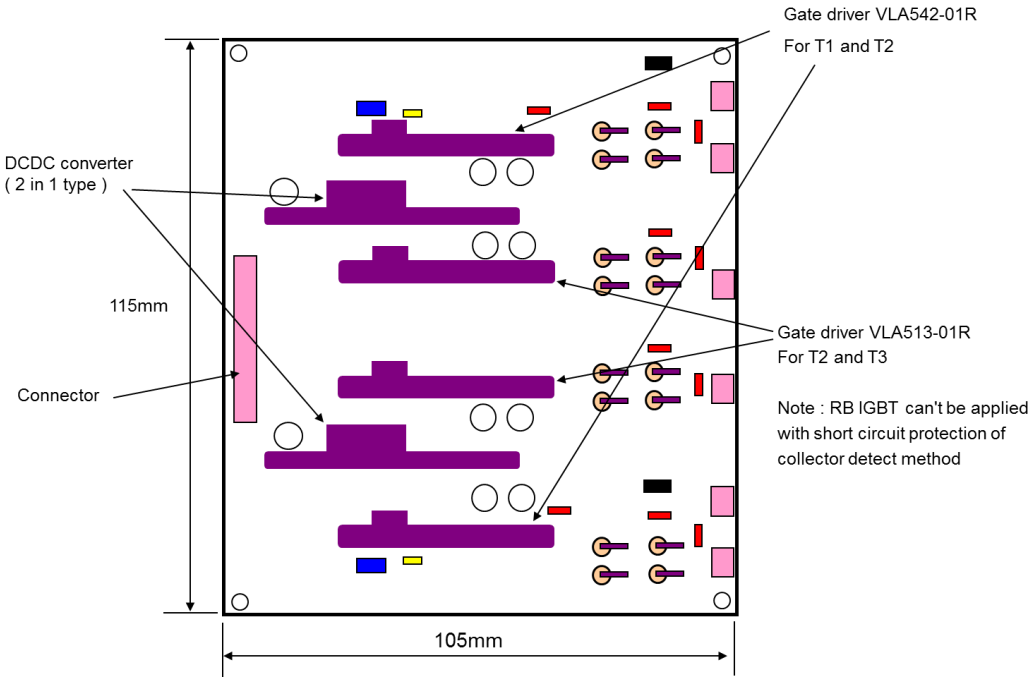


Figure 15.3: Outline view of driver.

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