Chapter 6

Cooling Design

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This section explains the cooling design.

For safe IGBT operation, the junction temperature (Tj) must never exceed Tj(max). Therefore, it is necessary to have a cooling design capable of keeping the junction temperature below Tj(max), even during overload conditions.

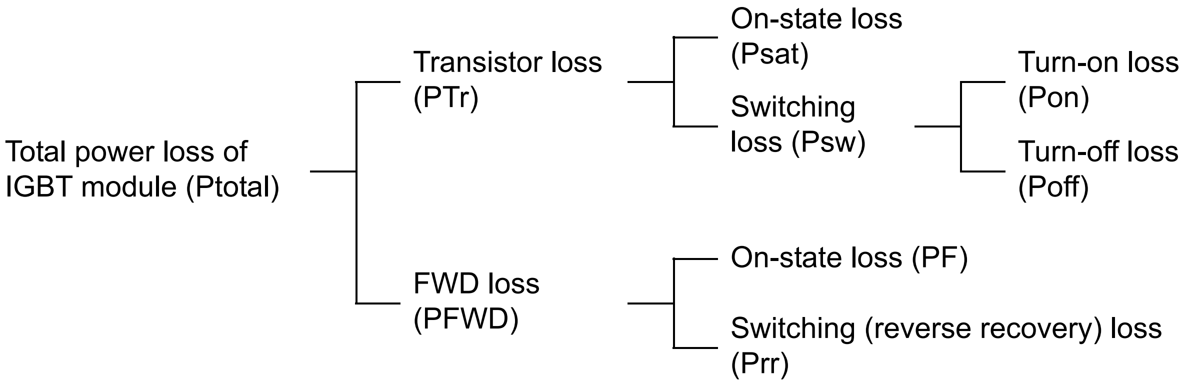
1 Power dissipation loss calculation

In this section, the simplified methods of calculating power dissipation for IGBT modules are explained. However, the detailed calculation tool of IGBT simulator is available on the Fuji Electric WEB site. It helps to calculate the power dissipation and thermal design for various working condition of various Fuji IGBT modules.

1-1 Types of power loss

An IGBT module consists of IGBT chips and FWD chips. The sum of the power losses from these sections equals the total power loss for the module. Power loss can be classified as either on-state loss or switching loss. A diagram of the power loss factors is shown as follows.

Power loss factors



The on-state power loss from the IGBT and FWD sections can be calculated using the output characteristics, while switching loss can be calculated from switching loss vs. collector current characteristics. Use these power loss calculations in order to design cooling sufficient to keep the junction temperature Tj below the maximum rated value.
The on-voltage and switching loss values to be used here, are based on the typical junction temperature Tj (125°C or 150°C are recommended).
For characteristics data, refer to the module specification sheets.

1-2 DC chopper circuit power loss calculations

For easy approximate calculations, consider the current flowing to the IGBT or FWD as a train of square waves. Fig.6-1 is a diagram showing the approximate waveforms of a DC chopper circuit. At collector current Ic the saturation voltage is represented by $V_{CE(sat)}$ and switching energy is represented by Eon and Eoff. At FWD forward current I_F, V_F represents the on- voltage and E_{RR} represents the energy loss during reverse recovery. Using the above parameters, IGBT power loss can be calculated as follows:

IGBT power dissipation loss (w) = On-state loss + Turn-on loss + Turn-off loss

$$= \left[t1/t2 \times V_{CE(sat)} \times I_C\right] + \left[fc \times \left(E_{on} + E_{off}\right)\right]$$

FWD power dissipation loss (w) = On-state loss + Reverse recovery loss

$$= \left[(1-(t1/t2)) \times I_F \times V_F\right] + \left[fc \times E_{rr}\right]$$

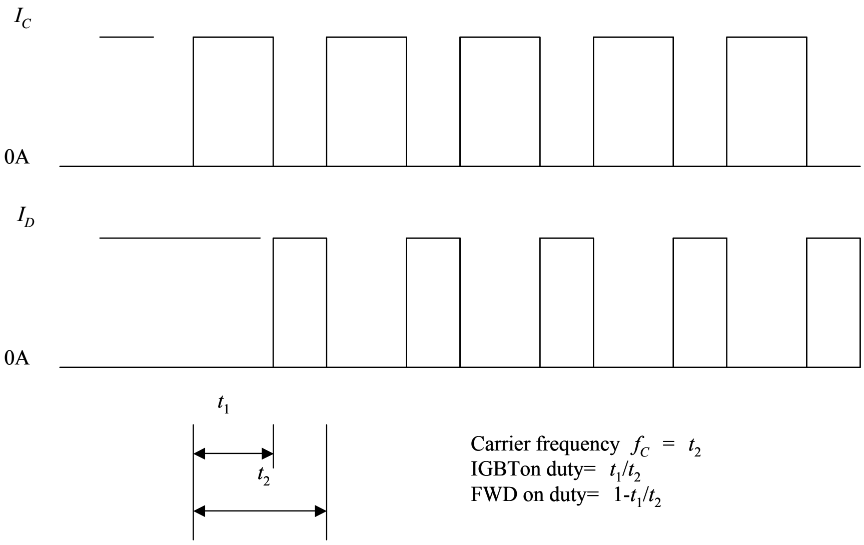


Fig. 6-1 DC chopper circuit current waveforms

The DC supply voltage, gate resistance, and other circuit parameters, may deviate from the standard value listed in the module specification sheets. In this event, approximate values can be calculated according to the following rules:

- DC supply voltage Ed(VCC) deviation
  On voltage: Not dependent on Ed(VCC)
  Switching loss: Proportional to Ed(VCC)

- Gate resistance deviation
  On voltage: Not dependent on gate resistance
  Switching loss: Proportional to switching time and dependent on gate resistance

1-3 Sine-wave VVVF inverter application power dissipation loss calculation

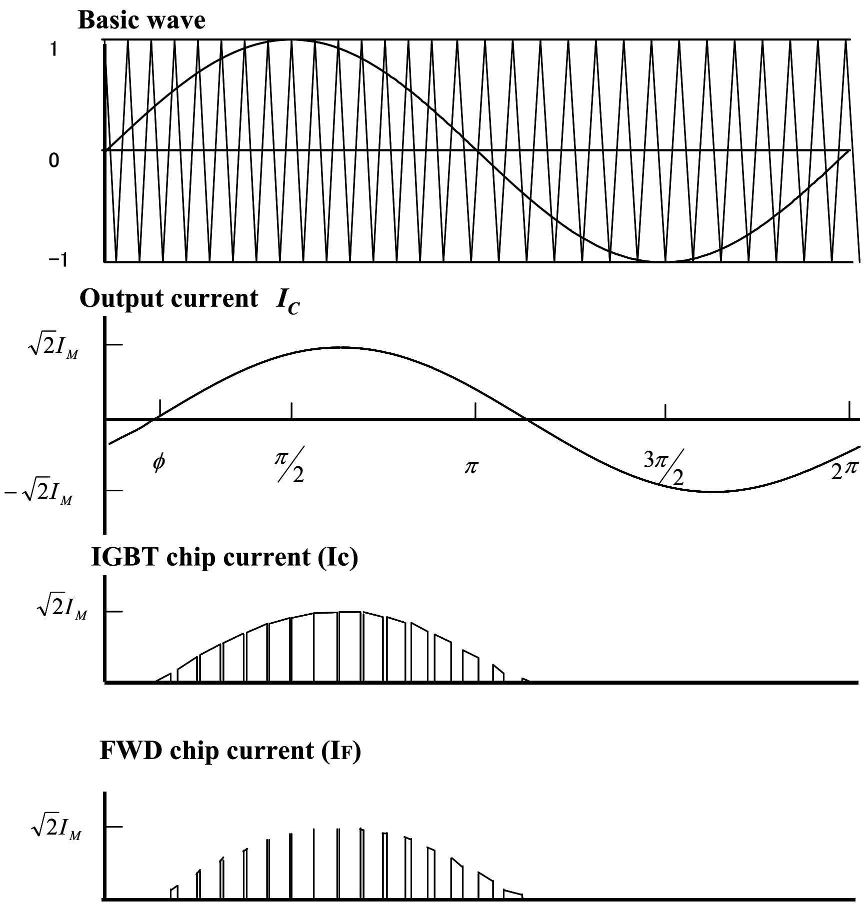


Fig. 6-2 PWM inverter output current

When using a VVVF inverter for a PWM control, the current value and operation keep changing as shown in Fig.6-2. Therefore, it is necessary to use computer simulations in order to make detailed power loss calculations. However, since computer simulations are very complicated, the following is an explanation of a simple method that generates approximate values.

Prerequisites

For approximate power loss calculations, the following prerequisites are necessary:
- Three-phase PWM-control VVVF inverter for sine-wave current output
- PWM control based on the comparison of sine-waves and sawtooth waves
- Output current in ideal sine-wave form

Calculating on-state power loss (Psat, P_F)

As displayed in Fig.6-3, the output characteristics of the IGBT and FWD have been approximated based on the data contained in the module specification sheets.

On-state power loss in IGBT chip (P_{sat}) and FWD chip (P_F) can be calculated as follows:

$$\left(P_{sat}\right) = DT\int_0^x I_C V_{CE(sat)} d\theta$$
$$= \frac{1}{2} DT\left[\frac{2\sqrt{2}}{\pi} I_M V_O + I_{M^2} R\right]$$

$$\left(P_F\right) = \frac{1}{2} DF\left[\frac{2\sqrt{2}}{\pi} I_M V_O + I_{M^2} R\right]$$

DT, DF: Average conductivity of the IGBT and FWD at a half wave of the output current. (Refer to Fig.6-4)

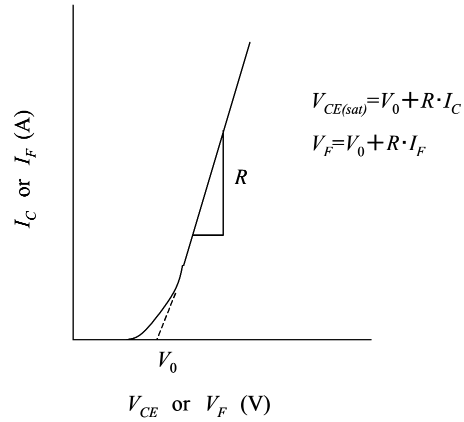


Fig. 6-3 Approximate output characteristics

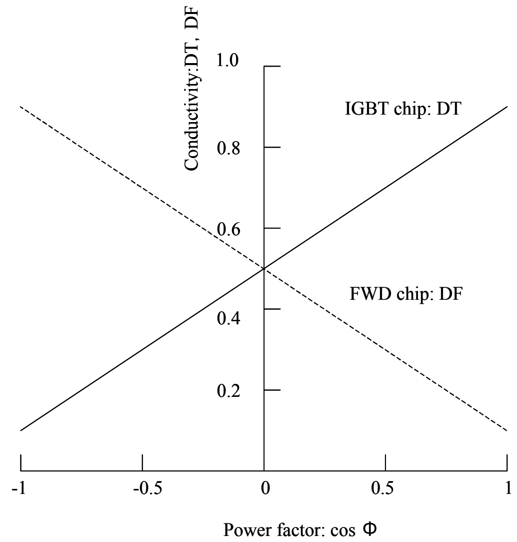


Fig. 6-4 Relationship between power factor sine-wave PWM inverter and conductivity

Calculating switching loss

The characteristics of switching loss vs. I_C are generally approximated using the following equations and Fig.6-5 (Module specification sheet data).

$$E_{on} = E_{on'}\left(I_C / ratedI_C\right)^a$$

$$E_{off} = E_{off'}\left(I_C / ratedI_C\right)^b$$

$$E_{rr} = E_{rr'}\left(I_C / ratedI_C\right)^c$$

a, b, c: Multiplier

Eon', Eoff', Err': Eon, Eoff and Err at rated IC

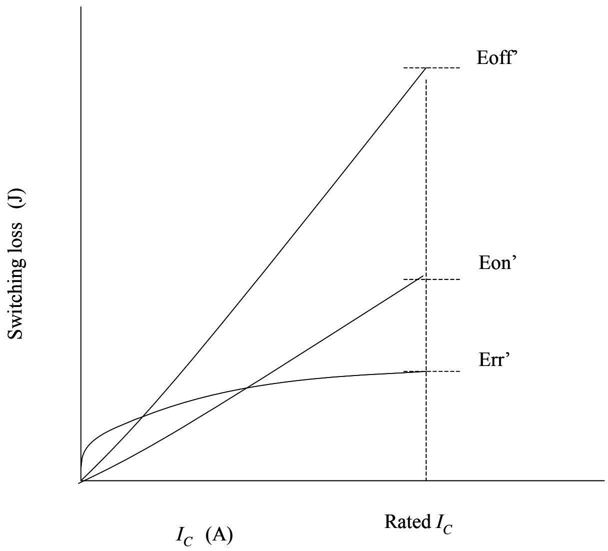


Fig. 6-5 Approximate switching losses

The switching loss can be represented as follows:

• Turn-on loss (P_{on})

$$P_{on} = fo\sum_{K=1}^{n}(E_{on})k \qquad \left(n: Half-cycle\ switching\ count = \frac{fc}{2fo}\right)$$

$$= foE_{on}'\frac{1}{rated\ I_{C^a}}\sum_{k=1}^{n}\left(I_{C^a}\right)k$$

$$= foE_{on}'\frac{n}{rated\ I_{C^a}\times\pi}\int_0^{\pi}\sqrt{2}I_{M^a}\sin\theta d\theta$$

$$\fallingdotseq foE_{on}'\frac{1}{rated\ I_{C^a}}nI_{M^a}$$

$$= \frac{1}{2}fcE_{on}'\left[\frac{I_M}{rated\ I_C}\right]^a$$

$$= \frac{1}{2}fcE_{on}\left(I_M\right)$$

E_{on}(IM):Ic= E_{on} at I_M

• Turn-off loss (P_{off})

$$P_{off} \fallingdotseq \frac{1}{2}fcE_{off}\left(I_M\right)$$

$E_{off}(I_M)$:Ic= E_{off} at I_M

• FWD reverse recovery loss (P_{rr})

$$P_{off} \fallingdotseq \frac{1}{2} fcE_{rr}(I_M)$$

$E_{rr}(I_M)$:I_c= E_{rr} at I_M

Calculating total power loss

Using the results obtained in section 1.3 subsection 2 and 3.

IGBT chip power loss: $P_{Tr} = P_{sat} + P_{on} + P_{off}$

FWD chip power loss: $P_{FWD} = P_F + P_{rr}$

The DC supply voltage, gate resistance, and other circuit parameters will differ from the standard values listed in the module specification sheets.
Nevertheless, by applying the instructions of this section, the actual values can easily be calculated.

2 Selecting heat sinks

Most of power diodes, IGBTs, transistors and other power devices are designed to have high voltage isolation between electrodes and base plate. This type of module can be mounted and compactly connected in a variety of equipment, because multiple devices can be mounted on a single heat sink. However, in order to ensure safe operation, the power loss (heat) generated from each module must be transferred efficiently. This is the reason why heat sink selections are very important. The basic of heat sink selection will be described in the following sections.

2-1 Thermal equations for on-state power loss calculations

The heat conduction of a power semiconductor can be simulated as an electric circuit. For this example, only one IGBT module is mounted on the heat sink, the equivalent circuit is shown in Fig.6-6

Using the above equivalent circuit, the junction temperature (Tj) can be calculated using the following thermal equation:

$$Tj = W \times \{Rth(j-c) + Rth(c-f) + Rth(f-a)\} + Ta$$

Note that the case temperature (T_c) and heat sink surface temperature mentioned here are measured from the base plate of the IGBT module directly underneath the chip. As shown in Fig.6-7, the temperature at all other points may be low due to the heat spreading of the heat sink, and this needs to be taken into consideration in final heat sink selection. Next, the equivalent circuit of an IGBT (2-pack-module) and a diode bridge mounted on a heat sink is shown in Fig.6-8. The thermal equations in this case are as follows:

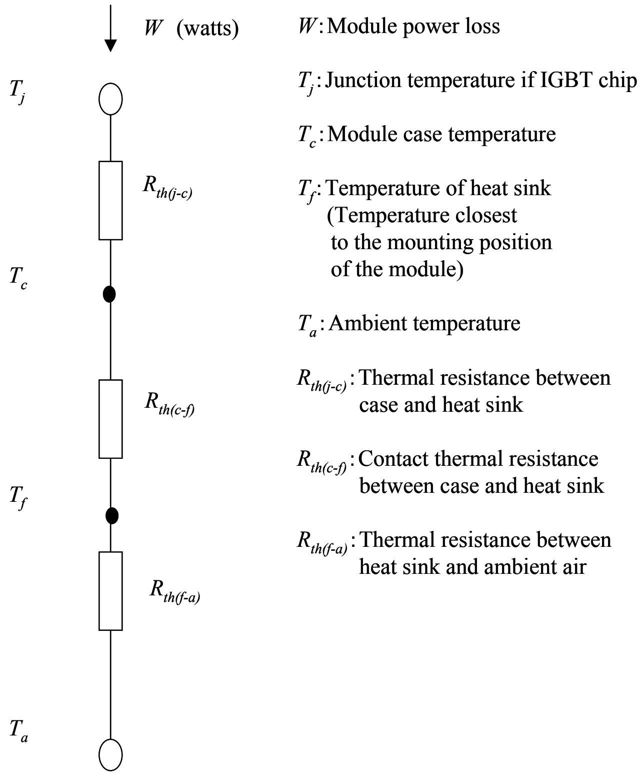
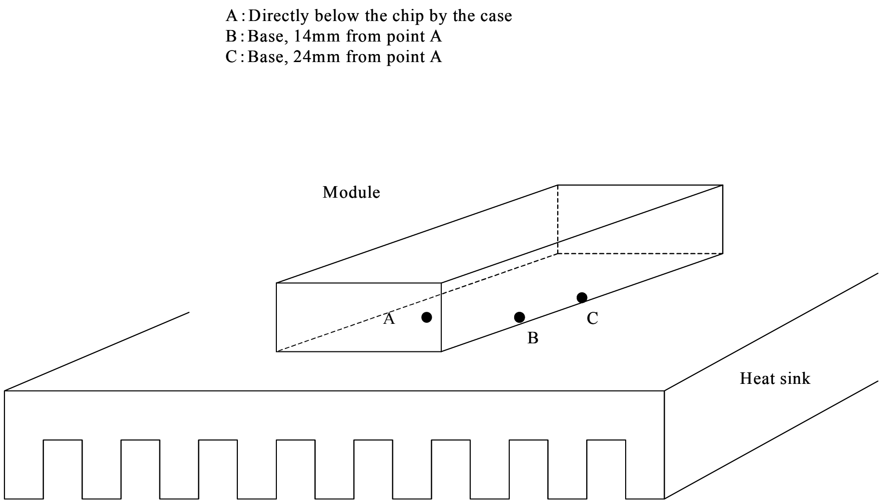


Fig. 6-6 Thermal resistance equivalent circuit

$$Tj(d) = Wd \times [Rth(j-c)d + Rth(c-f)d] + [(Wd + 2WT + 2WD) \times Rth(f-a)] + Ta$$

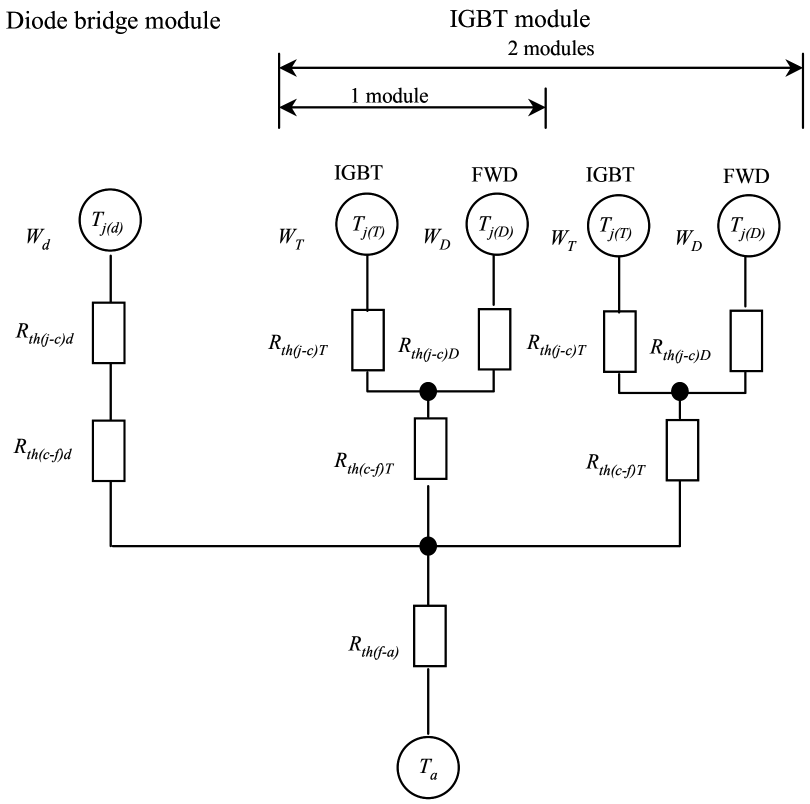
$$Tj(T) = WT \times Rth(j-c)T + [(WT + WD) \times Rth(c-f)T] + [(Wd + 2WT + 2WD) \times Rth(f-a)] + Ta$$
$$Tj(D) = WD \times Rth(j-c)D + [(WT + WD) \times Rth(c-f)T] + [(Wd + 2WT + 2WD) \times Rth(f-a)] + Ta$$

Use the above equations in order to select a heat sink that can keep the junction temperature (T_j) below T_j(max).



	Point A	Point B	Point C
T_C (°C)	51.9	40.2	31.4
T_f (°C)	45.4	36.9	30.2

Fig. 6-7 Example of case and heat sink temperature measurement



W_d, $T_{j(d)}$, $R_{th(\ )d}$: Diode bridge (For one module)
W_T, $T_{j(T)}$, $R_{th(\ )T}$: IGBT (Each element)
W_D, $T_{j(D)}$, $R_{th(\ )D}$: FWD (Each element)

Fig. 6-8 Thermal resistance equivalent circuit

2-2 Thermal equations for transient power loss calculations

In general, as described above steady-state T_j calculation provides enough information for heat sink design, however, actual operation has temperature ripples as shown in Fig.6-10 because repetitive switching produce pulse wave power dissipation and heat generation.

First consider the power loss as a train of constant cycles, and constant-peak square pulses. Then calculate the approximate peak of the temperature ripples using the transient thermal impedance curve given in the module specification sheets.

Be certain to select a heat sink that will also keep the T_{jp} below T_j (max).

$$Tjp - T_C = P \times \left[R(\infty) \times \frac{t1}{t2} + \left(1 - \frac{t1}{t2}\right) \times R(t1+t2) - R(t2) + R(t1) \right]$$

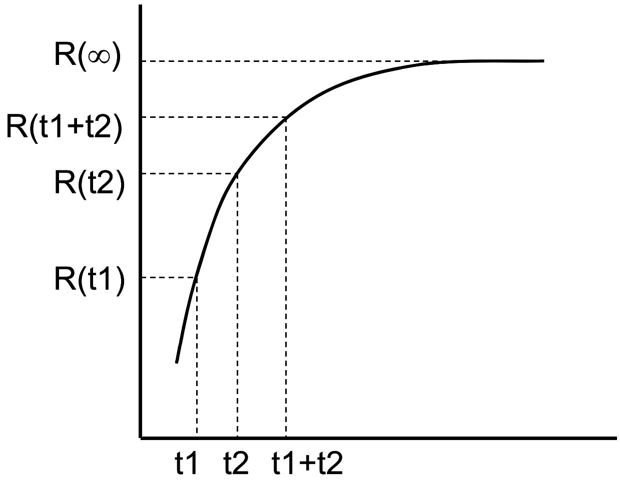


Fig. 6-9 Transient thermal resistance curve

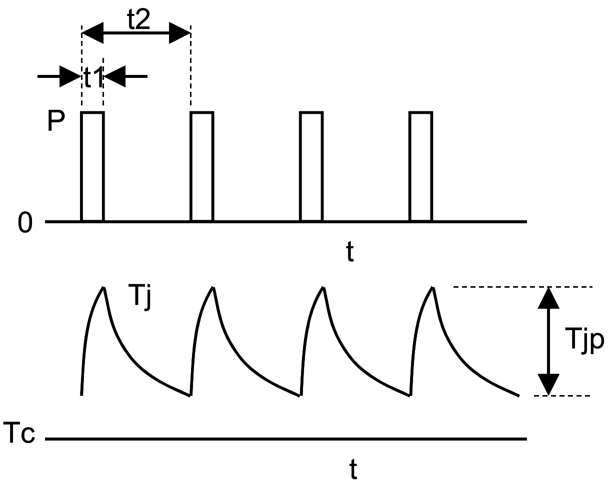


Fig. 6-10 Thermal ripples

3 Heat sink mounting precautions

3-1 Heat sink mounting

Since thermal impedance depends on IGBT mounting position, following attention should be taken into account:

- When mounting single IGBT module, the exact center of the heat sink generally results the lowest thermal impedance.
- When mounting multiple IGBT modules, determine the individual position on the heat sink according to the amount of heat generation from each module. Design more space for the modules that has higher heat generation.

3-2 Heat sink surface finishing

The mounting surface of the heat sink should be finished to a surface roughness of 10μm or less and a warpage of 50μm or less for every 100mm length. If the heat sink surface is not enough flat,
A drastic increase in the contact thermal resistance (Rth(c-f)) may be observed. If the flatness of the heat sink does not match the above requirements, IGBTs after mounted would have risk of extreme stress on the DBC substrate installed between the silicon chip and base plate. High voltage isolation failure would be concerned.

3-3 Thermal grease application

To obtain stable and low thermal contact resistance, a thermal greasing method between the heat sink and the IGBT base plate is highly recommended.

There are several methods of thermal grease application, such as roller, stencil mask and so on. Thermal grease helps the heat transfer from IGBT modules to heat sink, however the grease layer has also thermal capacity its. Therefore, when over thick thermal grease results chip temperature increase. On the other hand, extremely thermal grease application also may have a risk of chip temperature increase if the gap between the thermal grease and heat sink exists due to heat sink surface roughness or warpage. Therefore, the thermal grease layer must have the suitable thickness, otherwise the silicon chip may become higher than Tj(max), which results IGBT module destruction in the worst case. For these reasons, thermal grease application with stencil masks is recommended to help the uniform and stable application on the modules base plate.

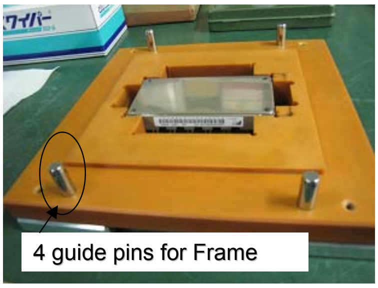
Figure 6-11 shows the schematic view of the thermal grease application using a stencil mask. The basic procedure is to apply the specified weight of thermal grease to the base plate surface of the IGBT module through a stencil mask. Subsequently fix the thermal-greased IGBT modules are mounted on the heat sink by tightening the screws with specific mounting torque recommended for respective products. In this way, the thermal grease is applied uniformly. Fuji Electric can supply stencil mask patterns on request.

1.Back to Room Temp.

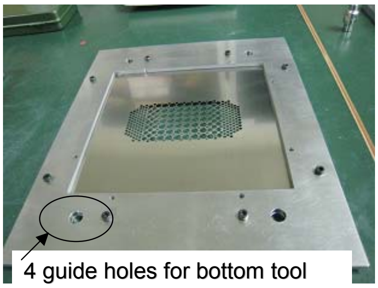
2.Mesure weight of IGBT

3.Adjust zero

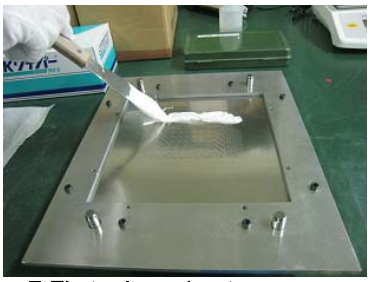
4.Bottom tool

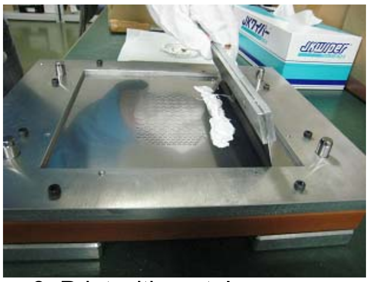


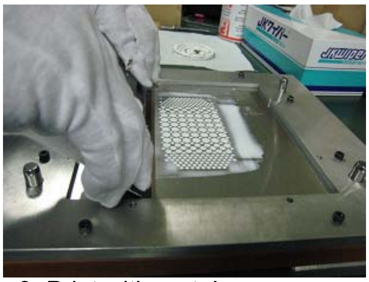
5.Set IGBT module

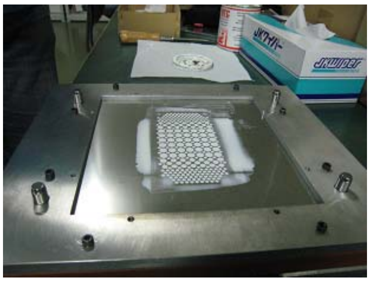


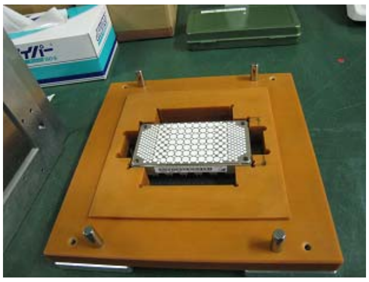
6.Metal mask and Frame


7.Fix tools and put grease with Knife


8. Print with metal squeegee (begin)


9. Print with metal squeegee (end)


10.After printing


11. Open metal mask

12. Check grease weight

Fig. 6-11 Schematic view of thermal grease application example

For the uniform thermal grease application, the required weight can be calculated as follows.

$$\text{Thermal grease thickness (um)} = \frac{\text{Weight of thermal grease (g)} \times 10^4}{\text{Baseplate area of IGBT module (cm}^2\text{)} \times \text{Density of thermal grease (g/cm}^3\text{)}}$$

It is recommended to estimate minimum weight of the thermal grease from the formula above before applying the the thermal grease. The recommended thickness thermal grease after mounted is 100µm.

However, the optimal thickness of thermal grease should be properly decided because it depends on the grease characteristics and its application method.

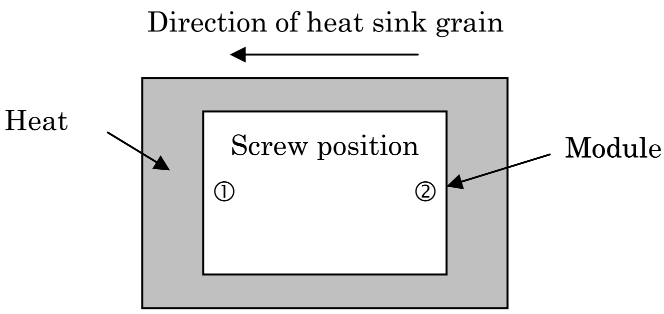
The recommended types of thermal grease are shown in Table 6-1.

Table 6-1 Example of thermal grease

Product name	Manufacturer
G746	Shin-Etsu Chemical Co., Ltd.
TG221	Nihon Data Material Co.,Ltd
SC102	Toray Dow-Corning Co., Ltd.
YG6260	Toshiba Silicone Co., Ltd.
P12	Wacker Chemie AG
HTC	ELECTROLUBE.

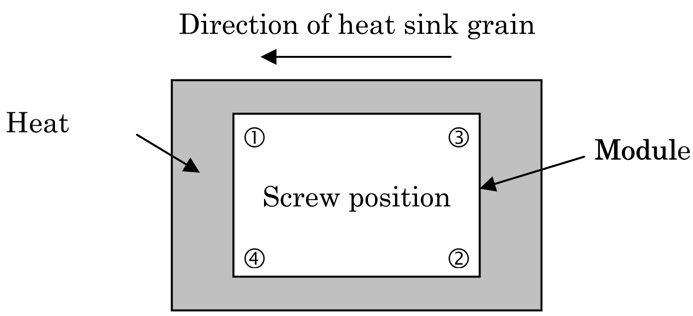
3-4 Mounting procedure

Diagrams in Figure 6-12 show how to tighten mounting screws to IGBT modules. Each screw must be tightened within a specified torque range, which is indicated in each IGBT module specification. An insufficient tightening torque may cause the poor contact thermal resistance and/or become mechanically loose during operation. On the other hand, an over torque may physically damage the IGBT case.



	Torque	Sequence
Initial	1/3 specified torque	①→②
Final	Full specified torque	②→①

(1) Two-points mounting



	Torque	Sequence
Initial	1/3 specified torque	①→②→③→④
Final	Full specified torque	④→③→②→①

(2) Four-points mounting

Fig. 6-12 Screw sequence for IGBT module

3-5 IGBT module mounting direction

When mounting the IGBT module on extrusion heatsink, it is recommended to place the module lengthwise in the direction of the heat sink grain. This reduces the effects of physical deformation of the heat sink shape.

3-6 Temperature verification

After deciding mounting position of IGBT module on the heatsink it is recommended to check the temperature of each position and confirm that the junction temperature (T_j) of each module if is within the design range.
For reference, Fig.6-12 is a diagram of how to measure the case temperature (T_c).

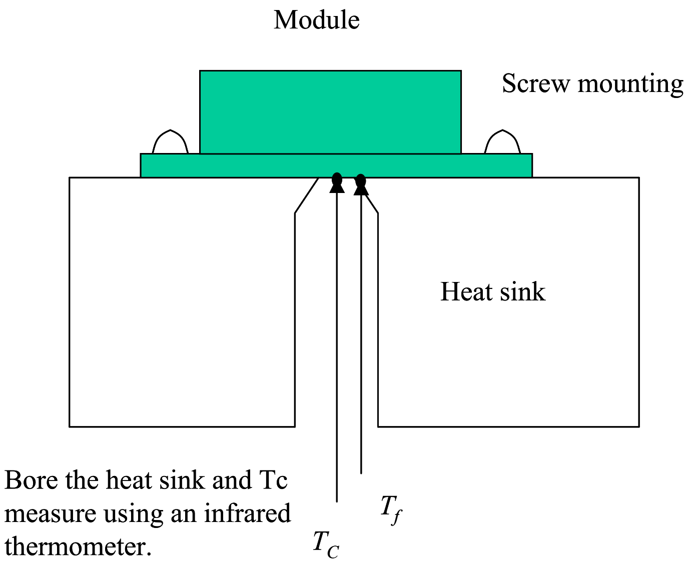


Fig. 6-13 Measurement of case temperature (Tc)

WARNING

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   The contents are subject to change without notice for specification changes or other reasons. When using a product listed in this Catalog, be sur to obtain the latest specifications.

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   - OA equipment
   - Communications equipment (terminal devices)
   - Measurement equipment
   - Machine tools
   - Audiovisual equipment
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