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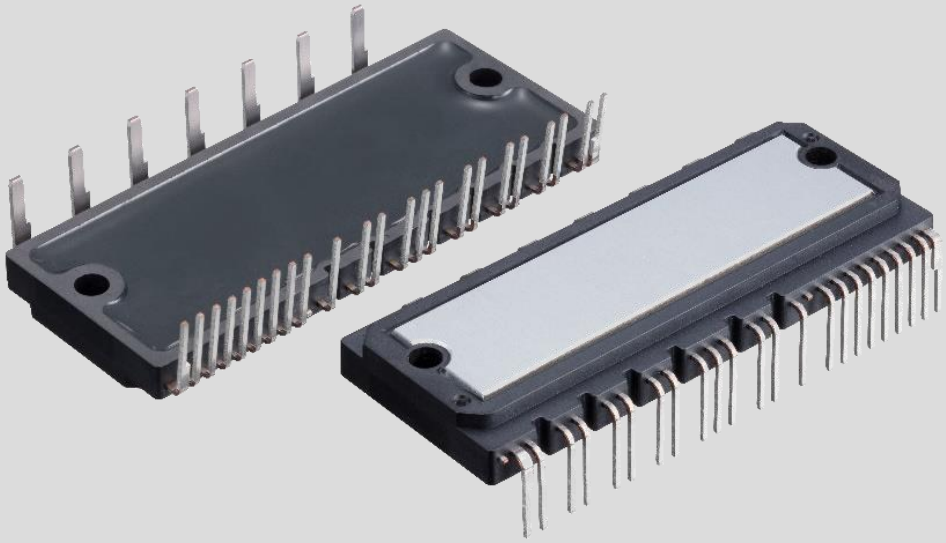

Small IPM (Intelligent Power Module)
P642 Series
6MBP**XT*065-50
Chapter 1 Product Outline

Application Manual

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Fuji Electric Co., Ltd.

MT6M15234 b

Chapter 1 Product Outline

1. Introduction

This manual describes the following contents for Fuji IGBT Intelligent-Power-Module “Small-IPM P642 series”

- Product summary
- Explanation of terminal symbols and terms
- Detailed explanation and design guideline of control terminals and power terminals
- Recommended wiring, layout and mounting guidelines

1.1 Product features

- 7th generation IGBT technology reduces power loss and realizes energy saving of equipment.
- Expansion of operating current by guaranteed T_{vjop}=150℃ and time limited T_{vj}=175℃ operation.
- Expansion of overload operating area by higher accuracy of short circuit protection detection.
- Lineup of 650V / 50A, 75A.

1.2 Built-in drive circuit

- The control IC of upper side arms have built-in high voltage level shift circuit (HVIC).
- The IPM can be driven directly by a microprocessor. The high-side IGBT can be driven directly. The voltage level of input signal is 3.3V or 5.0V.
- No reverse bias power supply is required due to short wiring length between the built-in drive circuit and IGBT and the impedance of the drive circuit is low.
- The IPM doesn’t need insulated power supplies for high-side drive because the IPM has built-in bootstrap diodes (BSD).

1.3 Built-in protection circuit

- The following built-in protection circuits are incorporated in the IPM device:
  (OC): Overcurrent protection
  (UV): Under voltage protection for power supplies of control IC
  (LT) or (OH): Temperature sensor output function or Overheating protection
  (FO): Fault status output

- The OC protection circuit protects the IGBT from overcurrent due to load short-circuit and arm short-circuit. This protection circuit adopts both sense current method and external shunt resistor method, thus arm short-circuit protection is possible.
- The UV protection circuit is triggered when there is voltage drop at the control power supply and the high-side drive power supply. It is integrated into all IGBT drive circuits.
- The OH protection circuit protects the IPM from overheating. It is built into the low side control IC (LVIC).
- The temperature sensor output function outputs temperature as analog voltage. It is built into LVIC.
- The FO function outputs an alarm signal when the IPM detects abnormal conditions. By outputting an alarm signal to the microprocessor unit (MPU), it is possible to shut down and prevent destruction of the system.

1.4 Compact package

- This IPM adopts aluminum insulating metal substrate (IMS) and has excellent heat dissipation.
- The pitch between control terminals is 2.54mm.
- The pitch between power terminals is 10mm.
- Total power loss is reduced by improving the trade-off between Collector-Emitter saturation voltage $V_{CE(sat)}$ and switching loss.

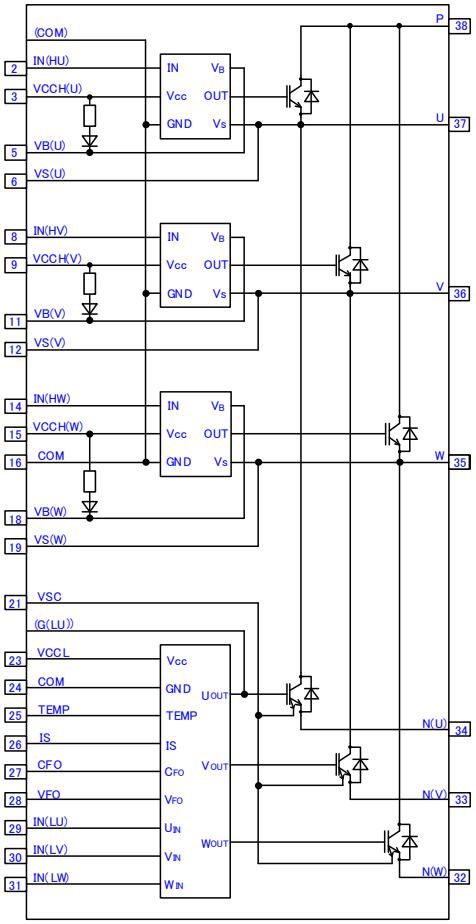


Fig. 1-1 Internal circuit diagram

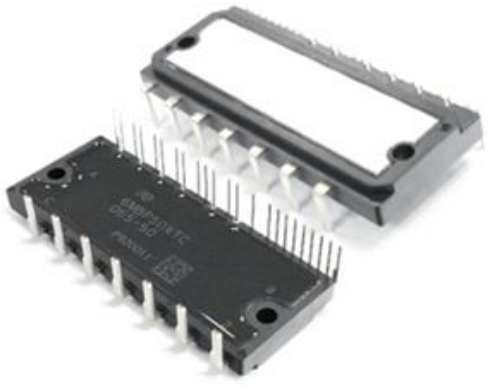


Fig. 1-2 Package external view

2. Product Lineup and Target Application

Table 1-1 Lineup

Type Name	IGBT Rating		Isolation Voltage [Vrms]	Variation
	Voltage [V]	Current [A]		
6MBP50XTA065-50	650	50	2500Vrms Sinusoidal 60Hz, 1min. (Between shorted all terminals and IMS)	LT*1
6MBP50XTC065-50				LT*1 OH*1
6MBP75XTA065-50		75		LT*1
6MBP75XTC065-50				LT*1 OH*1

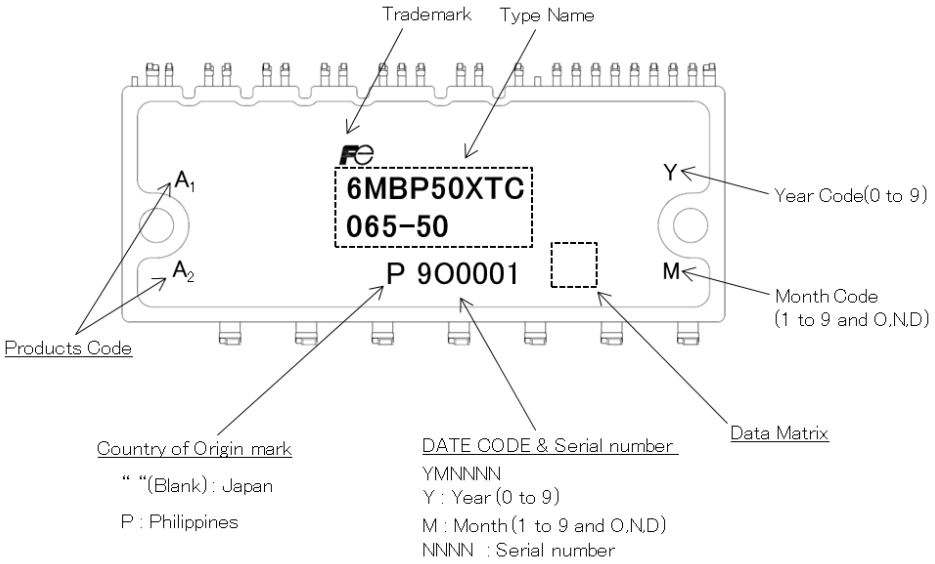
*1 (LT): Temperature sensor output function
(OH): Overheating protection

3. Definition of Type and Marking Specification

• Type Name

6 MBP 50 X T C 065 –50

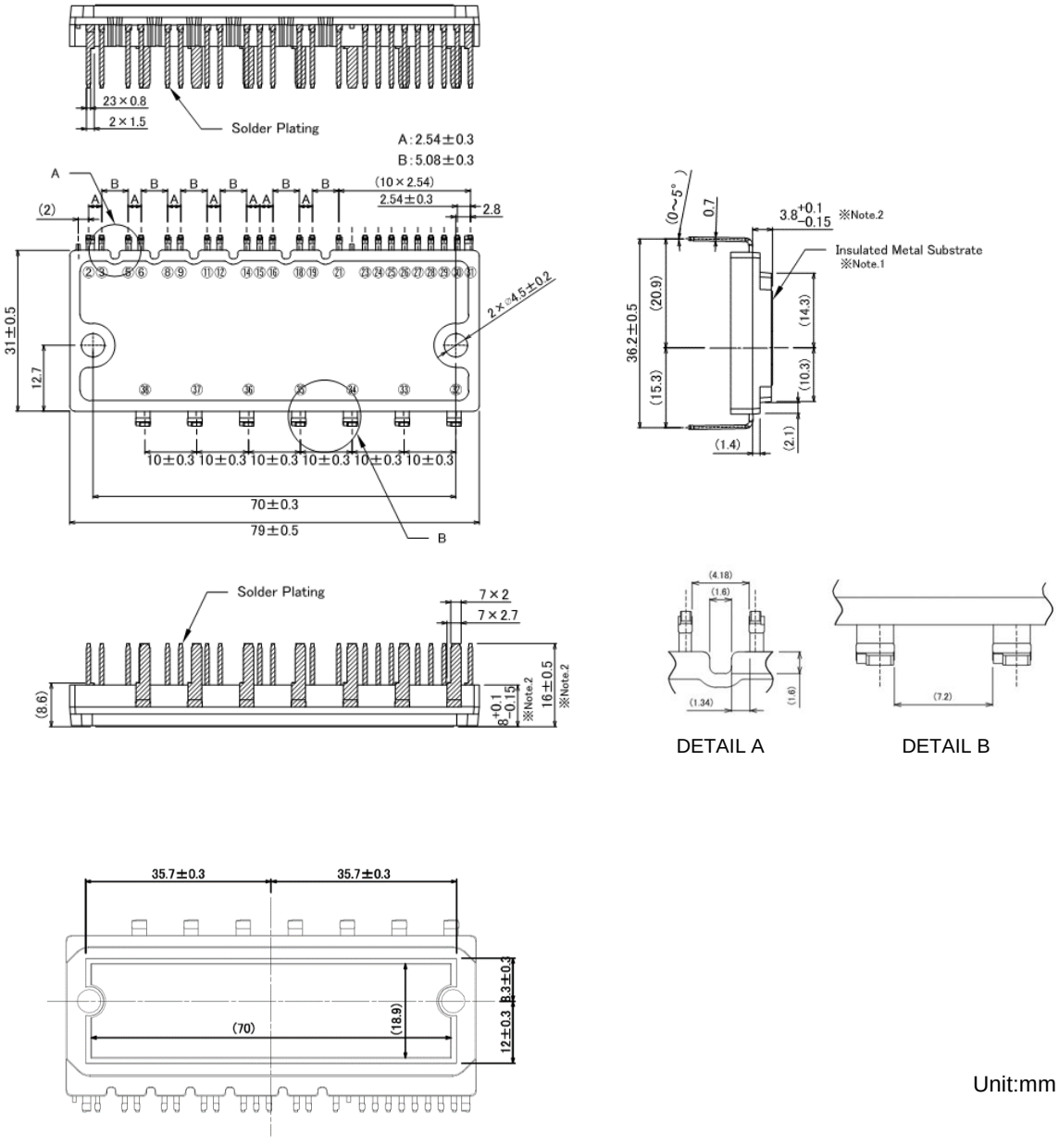
- Additional model number (Option)
  50 : RoHS
- Voltage rating
  065 : 650V
- Additional series code
  A : Temperature sensor output
  C : Temperature sensor output and Overheat protection
- Series name
  T: Package type
- Series name
  X: Chip generation
- IGBT current rating
  50:50A, 75:75A
- Indicates IGBT-IPM
- Number of switching elements
  6 : 6 switching elements



TYPE NAME	PRODUCT CODE	
	A_1	A_2
6MBP50XTA065-50	A	A
6MBP50XTC065-50	A	C
6MBP75XTA065-50	B	A
6MBP75XTC065-50	B	C

Fig. 1-3 Marking specification

4. Package Outline Dimension



Unit:mm

Note.1
The IMS (Insulated Metal Substrate) is deliberately protruded to improve the thermal conductivity between IMS and heat-sink.

Note.2
Thickness from the package surface to the back side including the IMS.

Fig. 1-4 Case outline drawing

5. Absolute Maximum Ratings

An example of the absolute maximum ratings of 6MBP50XTA065-50 is shown in Table 1-2.

Table 1-2 Inverter Block Absolute Maximum Ratings at T_{vj}=25℃, T_c=25℃, V_{CC}*1=15V, $V_{B(*)}$=15V (unless otherwise specified)

Item	Symbol	Rating	Unit	Description
DC Bus Voltage	$V_{DC\ (terminal)}$	450	V	DC voltage that can be applied between P-N(U),N(V),N(W) terminals. Please refer to Fig. 1-5 for details.
Bus Voltage (Surge)	$V_{DC(Surge,terminal)}$	500	V	Peak value of the surge voltage that can be applied between P-N(U),N(V),N(W) terminals during switching operation. Please refer to Fig. 1-5 for details.
Collector-Emitter Voltage	$V_{CE(chip)}$	650	V	Maximum collector-emitter voltage of IGBT and repeated peak reverse voltage of FWD. Please refer to Fig. 1-5 for details.
Collector Current	I_C	50	A	Maximum collector current of IGBT at T_c=25℃, T_{vj}=150℃*2
Peak Collector Current	I_{CP}	100	A	Maximum pulse collector current of IGBT at T_c=25℃, T_{vj}=150℃*2
Forward Current	I_F	50	A	Maximum forward current of FWD at T_c=25℃, T_{vj}=150℃*2
Peak Forward Current	I_{FP}	100	A	Maximum pulse forward current of FWD at T_c=25℃, T_{vj}=150℃*2
Collector Power Dissipation	P_{D_IGBT}	132	W	Maximum power dissipation per IGBT at T_c=25℃, T_{vj}=150℃*2
FWD Power Dissipation	P_{D_FWD}	89	W	Maximum power dissipation per FWD at T_c=25℃, T_{vj}=150℃*2
Self Protection DC Bus Voltage (arm short-circuit)	$V_{DC(sc)}$	400	V	Maximum DC voltage at which IGBT can be safely shut off by the IPM's protection function during short-circuit or overcurrent. Please refer to Fig. 1-5 for details.
Maximum Virtual Junction Temperature of Inverter Block	T_{vj}	175	℃	Maximum virtual junction temperature of IGBT and FWD*3
Operating Virtual Junction Temperature of Inverter Block	T_{vjop}	-40 ~ +150	℃	Virtual Junction Temperature of IGBT and FWD during continuous operation *3

Table 1-2 Control Circuit Block Absolute Maximum Ratings at T_{vj}=25℃, T_c=25℃,V_{CC} [*1]=15V, $V_{B(*)}$=15V (continued)

Item	Symbol	Rating	Unit	Description
High-side Supply Voltage	$V_{CCH(U)}$ $V_{CCH(V)}$ $V_{CCH(W)}$	-0.5 ~ 20	V	Voltage that can be applied between VCCH(U)-COM, VCCH(V)-COM, VCCH(W)-COM terminals.
Low-side Supply Voltage	V_{CCL}	-0.5 ~ 20	V	Voltage that can be applied between VCCL-COM terminals.
High-side Bias Absolute Voltage	$V_{VB(U)-COM}$ $V_{VB(V)-COM}$ $V_{VB(W)-COM}$	-0.5 ~ 670	V	Voltage that can be applied between VB(U)-COM, VB(V)-COM, VB(W)-COM terminals.
High-side Bias Voltage for IGBT Gate Driving	$V_{B(U)}$ $V_{B(V)}$ $V_{B(W)}$	-0.5 ~ 20	V	Voltage that can be applied between VB(U)-VS(U), VB(V)-VS(V), VB(W)-VS(W) terminals.
High-side Bias Offset Voltage	V_U V_V V_W	-5 ~ 650	V	Voltage that can be applied between U-COM, V-COM, W-COM terminals.[*4]
Input Signal Voltage	V_{IN}	-0.5 ~ V_{CCH}+0.5 -0.5 ~ V_{CCL}+0.5	V	Voltage that can be applied between IN(HU)-COM, IN(HV)-COM, IN(HW)-COM, IN(LU)-COM, IN(LV)-COM, IN(LW)-COM terminals.
Input Signal Current	I_{IN}	3	mA	Maximum current between IN(HU)-COM, IN(HV)-COM, IN(HW)-COM, IN(LU)-COM, IN(LV)-COM, IN(LW)-COM terminals.
Fault Signal Voltage	V_{FO}	-0.5 ~ V_{CCL}+0.5	V	Voltage that can be applied between VFO-COM terminals.
Fault Signal Current	I_{FO}	1	mA	Maximum sink current between VFO-COM terminals.
CFO Signal Voltage	V_{CFO}	-0.5 ~ 5.0	V	Voltage that can be applied between CFO-COM terminals.[*5]
CFO Signal Current	I_{CFO}	-0.05 / 3	mA	Maximum source / sink current between CFO-COM terminals.[*5]
Over Current Sensing Input Voltage	V_{IS}	-0.5 ~ V_{CCL}+0.5	V	Voltage that can be applied between IS-COM terminals.
TEMP Signal Voltage	V_{TEMP}	-0.5 ~ 5.0	V	Voltage that can be applied between TEMP-COM terminals.
TEMP Signal Current	I_{TEMP}	-0.05 / 3	mA	Maximum source / sink current between TEMP-COM terminals.
VSC Signal Voltage	V_{VSC}	-0.5 ~ V_{CCL}+0.5	V	Voltage that can be applied between VSC-COM terminals.[*6]
VSC Signal Current	I_{VSC}	-20	mA	Maximum source current between VSC-COM terminals.[*6]

Table 1-2 Control Circuit Block Absolute Maximum Ratings at T_{vj}=25℃, T_c=25℃,V_{CC} *1=15V, $V_{B(*)}$=15V (continued)

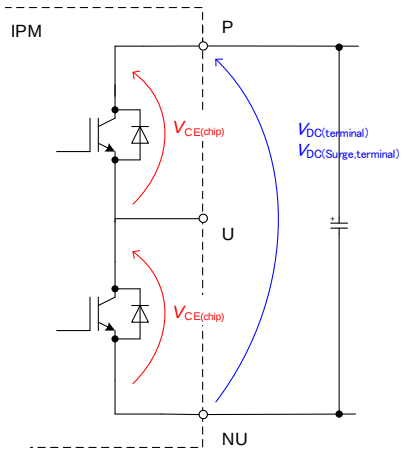
Item	Symbol	Rating	Unit	Description
Virtual Junction Temperature of Control Circuit Block	T_{vj}	150	℃	Average virtual junction temperature of the control circuit.
Operating Case Temperature	T_c	-40 ~ +125	℃	Operating case temperature (temperature of IMS directly under the IGBT or FWD chip).
Storage Temperature	T_{stg}	-40 ~ +125	℃	Ambient temperature range for storage and transportation (no load condition).
Isolation Voltage	V_{isol}	AC 2500	Vrms	Maximum voltage between IMS and all shorted terminals (Sine wave 60Hz, 1min)

*1 V_{CC} is applied between VCCH(U,V,W)-COM and VCCL-COM terminals.
*2 Pulse width and duty are limited by T_{vj}.
*3 The maximum virtual junction temperature during continuous operation is T_{vj}=150℃.
Continuous operation at over T_{vj}=150℃ may result in degradation of product lifetime such as power cycling capability with respect to the designed lifetime.
*4 Apply 13.0V or more between VB(U)-U, VB(V)-V, VB(W)-W terminals.
The IPM might malfunction if the high-side bias offset voltage is less than -5V.
*5 CFO is output terminal. Do not apply voltage or current.
Connect only the specified capacitor between CFO-COM terminals.
*6 VSC is output terminal. Do not apply voltage or current.
Connect only the specified resistor between VSC-COM terminals.

Absolute Maximum Rating of Collector-Emitter Voltage

The absolute maximum rating of collector-emitter voltage of the IGBT is specified below.
During operation, the voltage between P-N(*)[*1] is usually applied to high-side or low side of one phase.
Therefore, the voltage between P-N(*) must not exceed the absolute maximum rating of IGBT.
The collector-emitter voltage absolute maximum rating is described below.

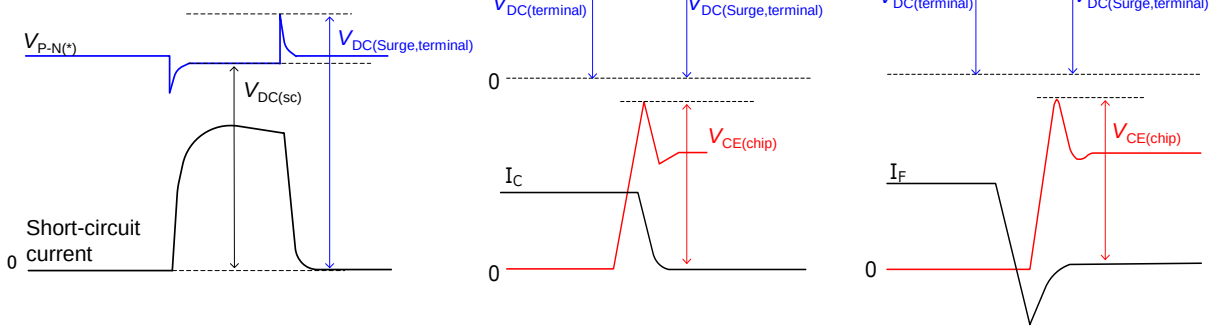
[*1] N(*) : N(U), N(V), N(W)



$V_{CE(chip)}$: Breakdown voltage of IGBT and FWD chip. Because it is difficult to measure directly, please use IPM with $V_{DC(terminal)}$, $V_{DC(Surge,terminal)}$ within the absolute maximum rating.

$V_{DC(terminal)}$: DC bus voltage (between P-N(*) terminals)

$V_{DC(Surge,terminal)}$: DC bus voltage at P-N(*) terminals including surge voltage generated during switching.



(a) During short-circuit (b) During IGBT turn-off (c) During FWD reverse recovery

Fig.1-5 Collector-emitter voltage

Fig.1-5 shows the waveforms during short-circuit, IGBT turn-off and FWD reverse recovery.
Since $V_{DC(Surge,terminal)}$ is different in each situation, it is necessary to set $V_{DC(terminal)}$ considering these situations.
$V_{CE(chip)}$ is the collector-emitter voltage absolute maximum rating of the IGBT chip. $V_{DC(Surge,terminal)}$ is specified considering the margin of surge voltage generated by the wiring inductance inside the IPM.
$V_{DC(terminal)}$ is specified considering the margin of surge voltage generated by the wiring inductance between P-N(*) terminals and electrolytic capacitor.