Chapter 5 Recommended Wiring and Layout

1. Examples of Application Circuit

This chapter describes the recommended wiring and layout.
Please refer to the following application circuit examples for tips and precautions when designing PCB.

Fig. 5-1, Fig. 5-2, and Fig. 5-3 show examples of application circuits using three types of current detection methods. The notes are common for all circuits.

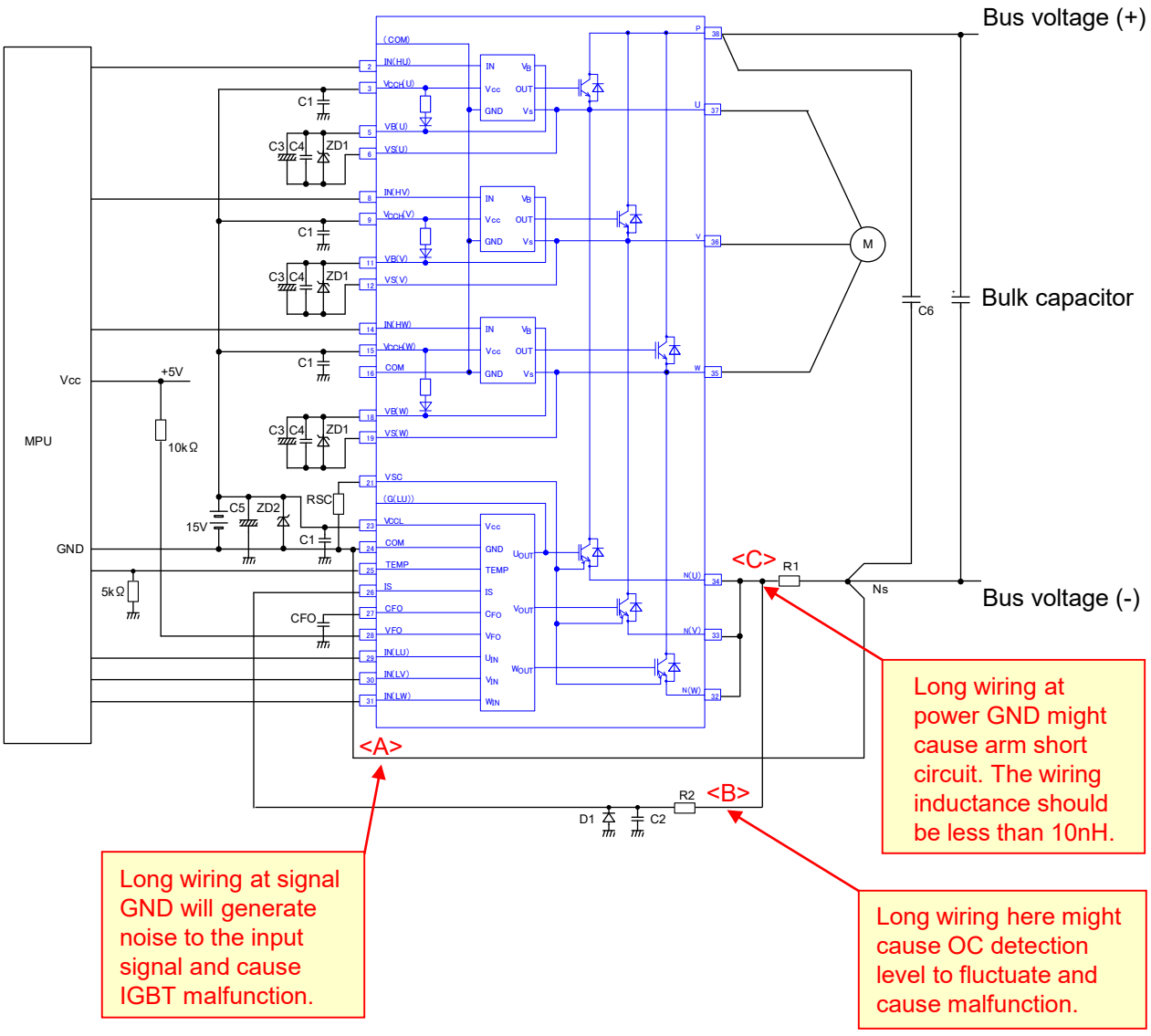


Fig. 5-1 Example of application circuit 1

(In the case of detecting all 3 phase current at once with a single shunt resistor)

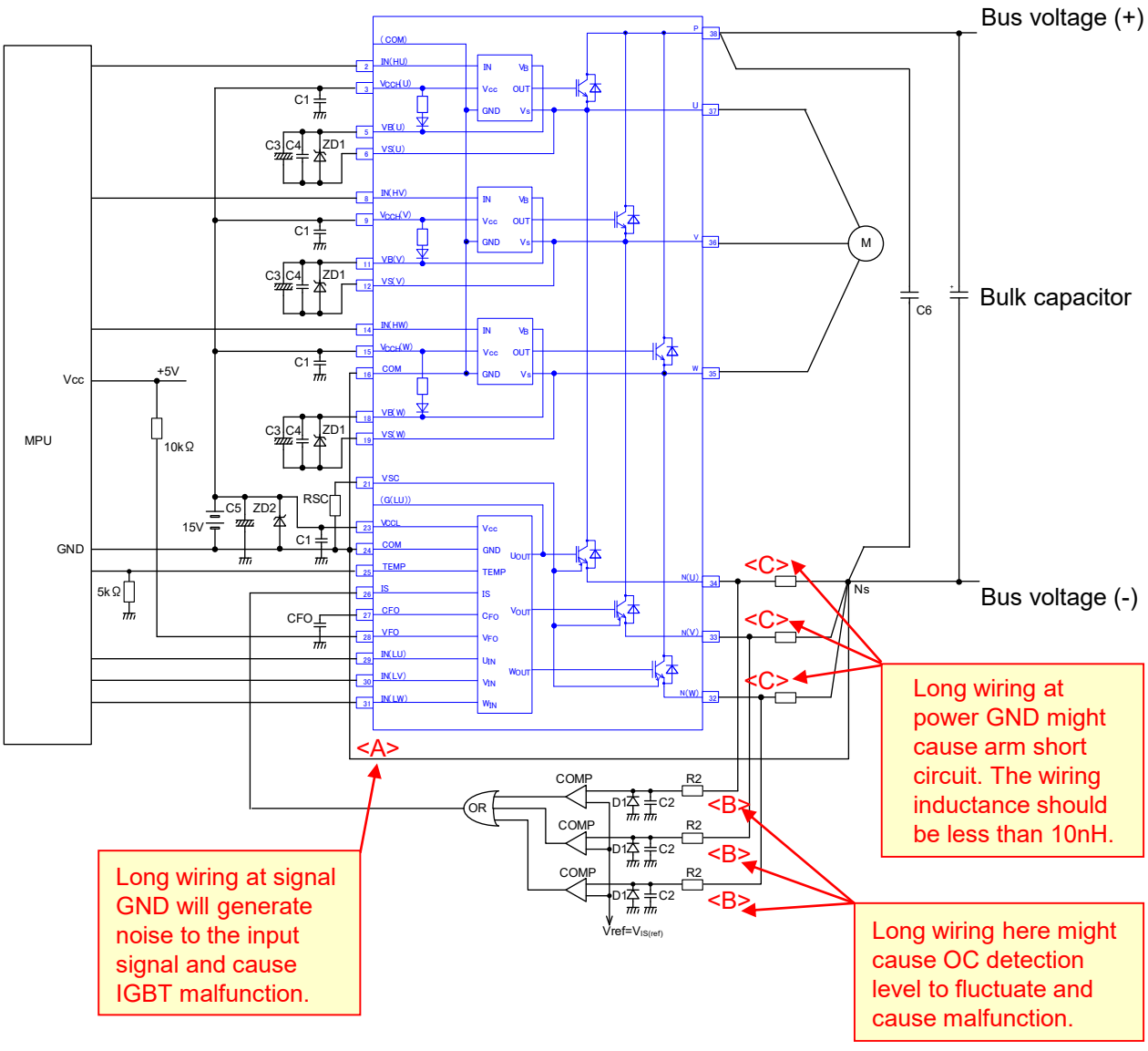


Fig. 5-2 Example of application circuit 2

(In the case of detecting each phase current with individual shunt resistor)

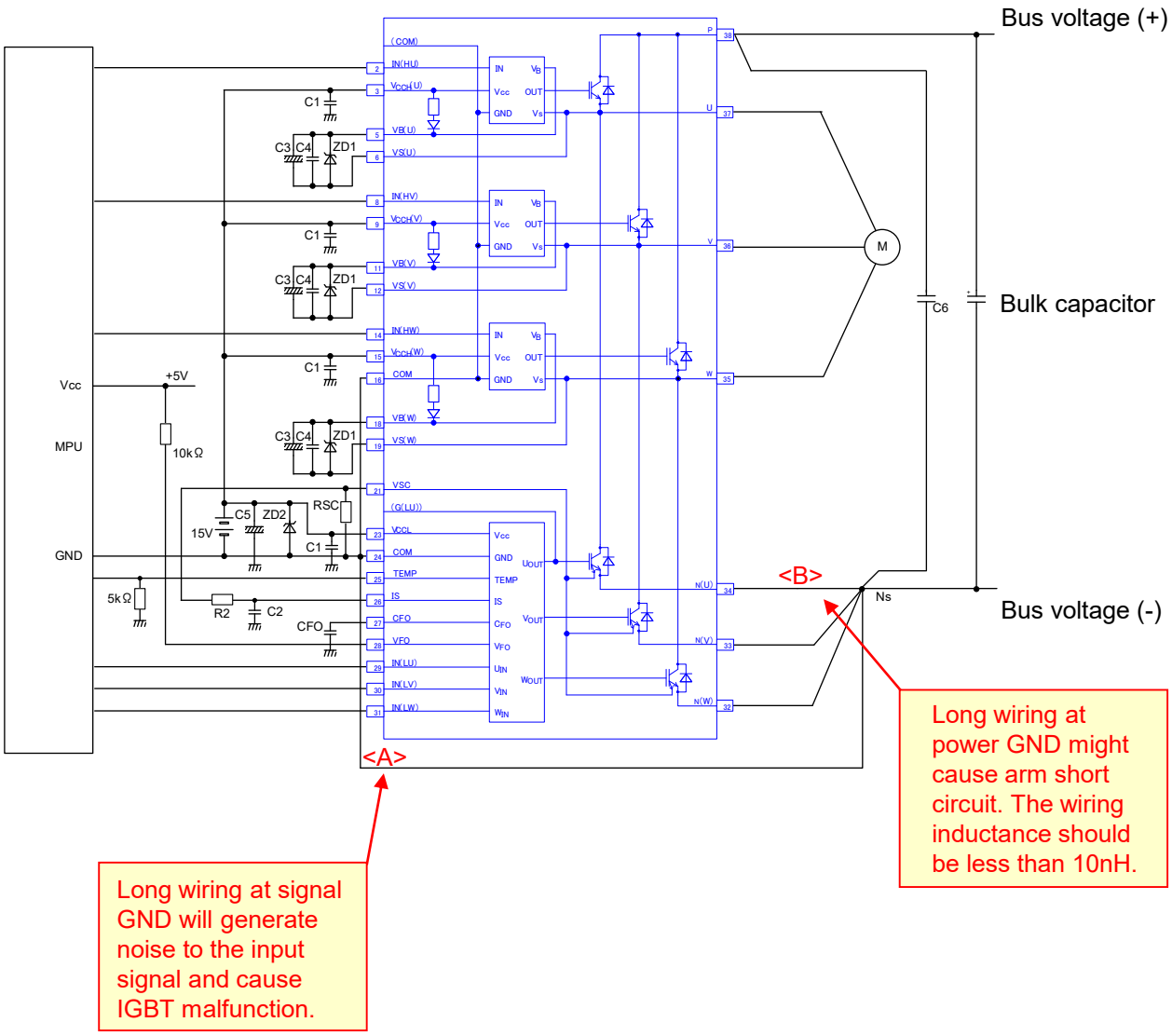


Fig. 5-3 Example of application circuit 3

(In the case of detecting sense current with sense resistor)

<Note>

1. The input signal of this product is high active. The input circuit of the control IC has built-in pull-down resistors. To prevent malfunction, the wiring of each input should be as short as possible. When using RC filter, set the input signal level to meet the turn-on and turn-off threshold voltages.
2. VFO output is open drain type. It should be pulled up to 5V power supply with resistor of about 10kΩ.
3. To prevent malfunction, the wiring of <A>, <B> and <C> should be as short as possible.
4. Set the time constant of R2-C2 of the OC protection circuit to about 1.1us. The OC shutdown time might vary depending on the wiring pattern. For R2 and C2, tight tolerance, temperature compensated type is recommended.
5. It is recommended to set the OC protection circuit comparator reference voltage to the same level as the IPM OC protection threshold voltage $V_{IS(ref)}$.
6. Use high speed comparator and logic IC to detect OC condition quickly.
7. It is recommended to connect a Schottky barrier diode D1 if negative voltage is generated at R1 during switching operation.
8. All capacitors should be connected as close as possible to the terminals. Ceramic capacitors with excellent temperature, frequency and DC bias characteristics for C1 and C4, and electrolytic capacitors with excellent temperature and frequency characteristics for C3 and C5 are recommended.
9. To prevent destruction caused by surge voltage, the wiring between snubber capacitor C6, P terminal and Ns node should be as short as possible. Generally, the recommended snubber capacitance is 0.1uF to 0.22uF.
10. The two COM terminals (terminal no.16 & 24) are not connected internally. Connect both terminals to the signal GND at single point.
11. To prevent the destruction caused by surge voltage, it is recommended to connect a 22V Zener diode to each control power supply and high-side bias voltage terminal.
12. It is recommended that the signal GND and the power GND be wired separately, and to connect the snubber capacitor GND : Ns at a single point to avoid the effect of voltage fluctuation due to current flowing in the power line.
13. For R_{sc}, it is recommended to use a resistor with small variation (1% or less) including temperature characteristics, low inductance, and wattage rating of 1/8W or more.
    Please evaluate it sufficiently in actual system.
14. When using external shunt resistors, it is recommended to use low inductance chip resistors. Do not use shunt resistors with large inductance, such as cement resistors.

2. Recommendations and Precautions in PCB Design

In this section, the recommended pattern layout and precautions in PCB design are described.
Fig. 5-4 to Fig. 5-8 show the images of recommended PCB layout in examples of application circuit (Fig. 5-1, Fig. 5-2, Fig. 5-3).
In these figures, the input signal from the system is represented by “IN(HU)”.

Recommended layouts and precautions are as follows.

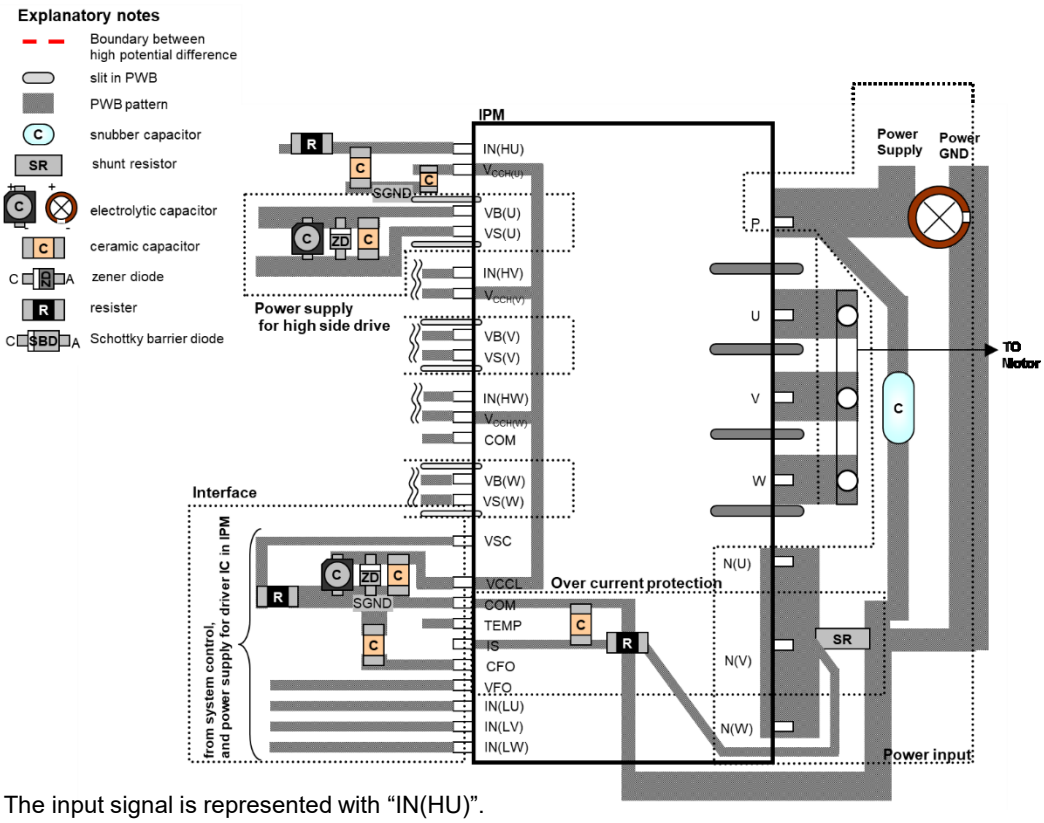
(1) Overall design around the IPM

(A) At boundary where the potential difference is high, secure an appropriate creepage distance. (Make a slit between there if necessary)

(B) Separate the pattern of power input (DC bus voltage) part and the high-side bias voltage part to prevent the increase of conduction noise. In the case of using a multilayer PCB and crossing these wirings on pattern, please take note of the stray capacitance between the wirings and the insulation performance of the PCB.

(C) Separate the high-side bias voltage and the input circuit pattern for each phase to prevent system malfunction. In the case of using a multilayer PCB, it is strongly recommended not to cross these wirings.

Details of each part are described in next page.



Note) The input signal is represented with “IN(HU)”.

Fig. 5-4 Image of recommended PCB layout (Overall design around the IPM)

(2) Power input part

(A) Connect the snubber capacitor between the P terminal and the GND of the shunt resistor as close as possible. To avoid the influence of pattern inductance, the pattern between snubber capacitor, P terminal and shunt resistor should be as short as possible.

(B) Separate the pattern of the bulk capacitor and the pattern of the snubber capacitor near to the P terminal and shunt resistor.

(C) The pattern from the power GND and COM terminal should be connected as close as possible to the shunt resistor at a single point ground.

(D) Please use low inductance type for shunt resistor.

(E) The pattern between the N(U), N(V), N(W) terminals and the shunt resistor should be as short as possible.

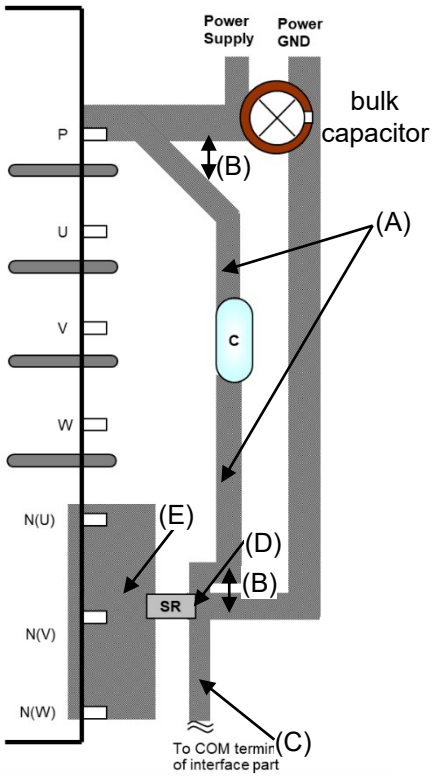


Fig. 5-5 Image of recommended PCB layout (Power input part)

(3) High-side bias voltage part

(A) The pattern between VB(U,V,W) terminal and the electronic components (ceramic capacitor, electrolytic capacitor, Zener diode) should be as short as possible.

(B) Use an appropriate capacitor according to the application. In particular, use a ceramic capacitor or a low ESR capacitor close to the VB(U,V,W) terminals.

(C) If the stray capacitance between VB(U) and the power GND (or equal potential) terminal is large, the voltage between VB(U) and VS(U) terminals might become overvoltage or negative voltage due to the high dV/dt during IGBT turn-on and turn-off. Therefore, it is recommended to connect a Zener diode between VB(U) and VS(U) terminals. It should be connected as close as possible to VB (U) terminal.
(The same applies to VB(V) and VB(W).)

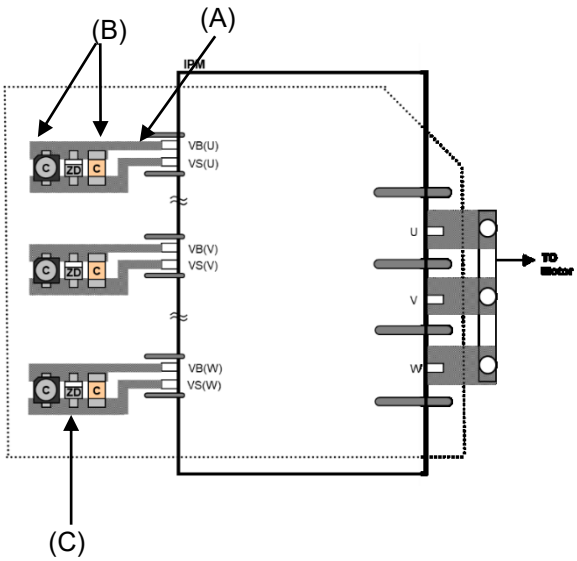


Fig. 5-6 Image of recommended PCB layout (High-side bias voltage part)

(4) Interface part

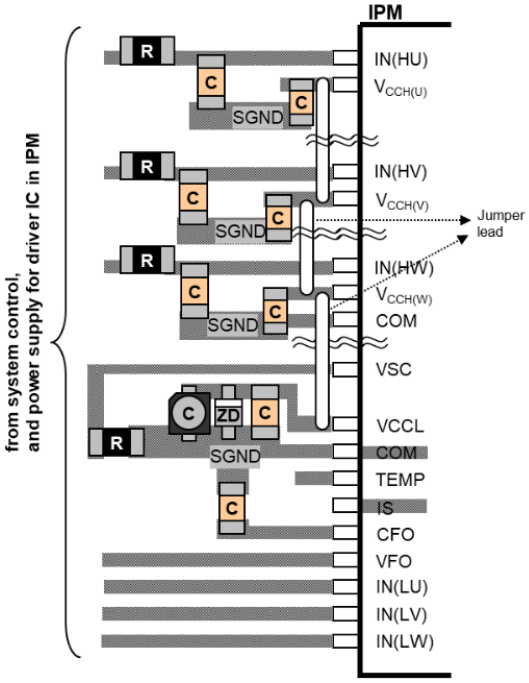
(A) If the influence of noise from the high-side bias voltage is not negligible, connect a capacitor between the input signal and the COM terminal. The negative pole of the capacitor should be connected to the signal GND as close as possible to the COM terminal.
In the case of connecting a filter resistor or capacitor, please take into account of the built-in pull-down resistor and confirm the the input signal level in the actual system.

(B) The two COM terminals (terminal no.16 & 24) are not connected internally. Connect both terminals to the signal GND at single point.

(C) Connect an electrolytic capacitor and a ceramic capacitor between VCCL and COM, and between VCCH(U,V,W) and COM. Connect these capacitors as close as possible to each terminal.

(D) The output signal from the TEMP terminal should be in parallel with the signal GND in order to minimize the effect of noise.

(E) The pattern of signal GND from the system and the pattern from the COM terminal should be connected at a single point ground. The single point ground should be as close as possible to the COM terminal.



Note) The input signal is represented with "IN(HU)".

Fig. 5-7 Image of recommended PCB layout (Interface part)

(5) Overcurrent protection part

As shown in Fig. 5-1, Fig. 5-2 and Fig. 5-3, there are three methods for OC detection and protection. They are “Detecting all 3 phase current at once with a single shunt resistor method” (Fig. 5-8(a)), “Detecting each phase current with individual shunt resistor method” (Fig. 5-8(b)), and “Detecting sense current with sense resistor method” (Fig. 5-8(c)).

In Fig. 5-8(a)

(A) The pattern between the negative pole of the shunt resistor and the COM terminal is very important. It is the reference potential for the control IC, and also the path for the high-side bootstrap capacitor charging current and the low-side IGBT gate drive current. Therefore, to minimize the effect of common impedance, this pattern should be as short as possible.

(B) The pattern of IS signal should be as short as possible to avoid OC level fluctuation.

(C) To prevent erroneous detection during switching operation, connect a RC filter to the IS terminal. The negative pole of the RC filter capacitor should be connected to the signal GND near the COM terminal.

(D) If negative voltage is applied to the IS terminal during switching operation, connect a Schottky barrier diode between the IS terminal and the COM terminal or in parallel with the shunt resistor.

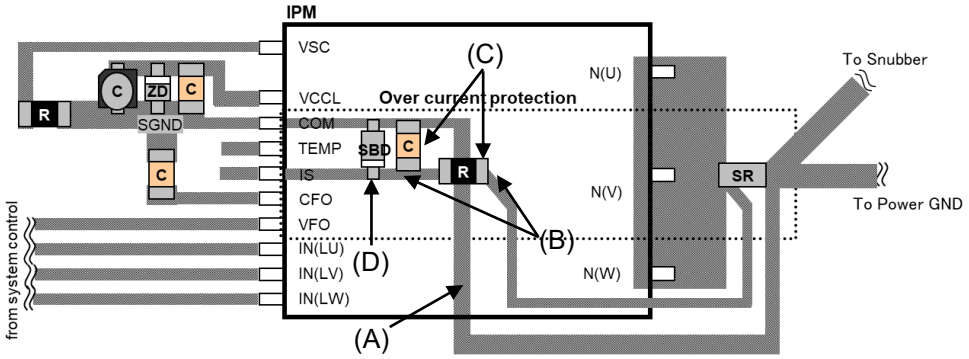


Fig. 5-8(a) Detecting all 3 phase current at once with a single shunt resistor method

In Fig. 5-8(b)

(A) Use high speed comparator and logic IC to detect OC condition quickly

(B) The reference voltage of OC which is input to the comparator should be coupled by a capacitor to signal GND. The capacitor should be connected as close as possible to the comparator.

(C) Separate the signal GND pattern of COM terminal and the signal GND pattern of comparator.

(D) The signal GND pattern of COM terminal and the signal GND pattern of comparator should be connected at a single point ground. The single point ground should be as close as possible to the shunt resistor.

(E) Other precautions and recommended patterns are same as Fig. 5-7(a). Refer to Chapter 4, Section 2 for details on circuit constant determination.

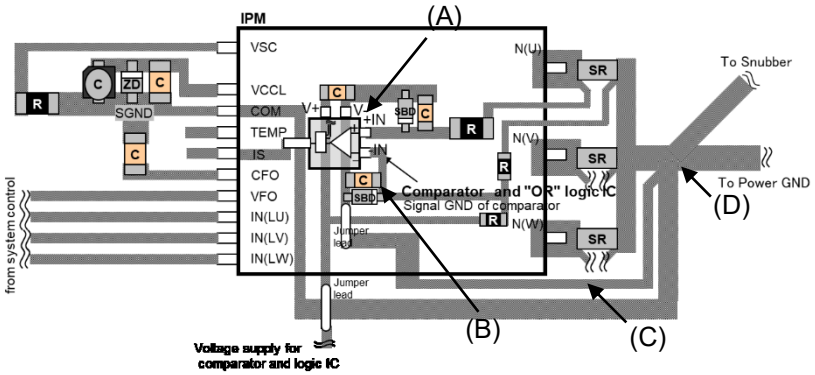


Fig. 5-8(b) Detecting each phase current with individual shunt resistor method

In Fig. 5-8(c)

(A) It is recommended that the signal GND and the power GND be wired separately, and to connect the snubber capacitor GND : Ns at a single point to avoid the effect of voltage fluctuation due to current flowing in the power line.

(B) To prevent fluctuations of the OC protection level and malfunction, the IS signal pattern should be as short as possible.

(C) To prevent erroneous detection during switching operation, connect a RC filter to the IS terminal. The negative pole of the RC filter capacitor should be connected to the signal GND near the COM terminal.

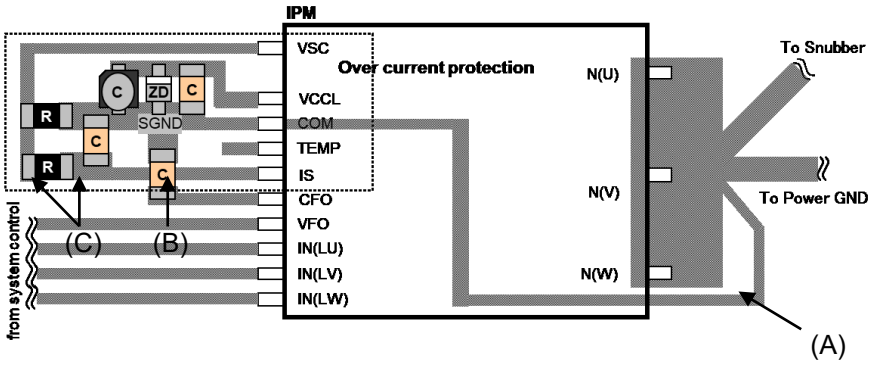


Fig. 5-8(c) Detecting sense current with sense resistor method