Chapter 3 Details of Control & Protection Functions

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1. Control Power Supply, VCCH(U,V,W), VCCL, COM

1. Voltage range of control power supply $V_{CCH(U,V,W)}$, V_{CCL}

Please connect 15V DC power supply between VCCH(U), VCCH(V), VCCH(W), VCCL and COM terminals for the control power supply of this IPM. The voltage should be regulated to 15V±10% for proper operation. Table 3-1 describes the operating state of the IPM for various control power supply voltages. A low impedance capacitor and a high frequency decoupling capacitor should be connected close to the terminals of the power supply.

High frequency noise on the power supply might cause malfunction of the internal control IC or output erroneous fault signal. To avoid these problems, the maximum amplitude of voltage ripple of the control power supply should be less than ±1V/μs.

When connecting external shunt resistor, the potential at the COM terminal is different from that at the N(*)*1 terminal. Please refer all control circuits and power supplies to the COM terminal and not to the N(*)*1 terminals. If circuits are improperly connected, current might flow through the shunt resistor and cause improper operation of the short-circuit protection function. In general, it is recommended to set the COM terminal as the ground potential in the PCB layout.

The main control power supply is also connected to the bootstrap circuit, which provide floating power supplies for gate driving of high-side IGBTs.

When high side control power supply voltage $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ falls below $V_{CCH(OFF)}$, only the IGBT which UV protection is triggered is turned-off regardless of input signal condition.

When low side control power supply voltage V_{CCL} falls below $V_{CCL(OFF)}$, all low-side IGBTs are turned-off regardless of input signal condition.

Table 3-1 $V_{CCH(U,V,W)}$, V_{CCL} voltage range versus operating state of IPM

Voltage range [V]	Operating state of IPM
0 ~ 4	The IPM does not operate. UV protection and alarm output do not function. dv/dt noise on P-N(*) power supply might cause malfunction to the IGBTs.
4 ~ 13	The IPM starts to operate. UV protection is activated. Input signals are blocked and fault output is generated.
13 ~ 13.5	UV protection is reset. Low-side IGBTs perform switching operation according to the input signal. Due to the driving voltage is below the recommended range, the conduction losses and switching losses of the IGBTs are larger than normal. The high-side IGBTs do not operate until $V_{B(*)}$*2 reach $V_{B(ON)}$ after initial charging.
13.5 ~ 16.5	The IPM operates under recommended operating conditions.
16.5 ~ 20	Due to the driving voltage is above the recommended range, IGBTs are switching faster, which increases the system noise. Even with proper overcurrent protection design, the peak short-circuit current might be too large and lead to destruction.
Over 20	The IPM might be destroyed. It is recommended to connect a Zener diode to each control power supply terminal if necessary.

*1 N(*) : N(U),N(V),N(W) *2 $V_{B(*)}$: $V_{B(U)}$, $V_{B(V)}$, $V_{B(W)}$

2. Under voltage (UV) protection of control power supply $V_{CCH(U,V,W)}$, V_{CCL}

Fig.3-1 shows the UV protection circuit of high-side and low-side control power supply ($V_{CCH(U,V,W)}$, V_{CCL}). Fig.3-2 and Fig.3-3 show the UV protection operation sequence.

As shown in Fig.3-1, diodes are electrically connected to the VCCH(U,V,W)-COM and VCCL-COM terminals. These diodes are built-in to protect the IPM from input surge voltage. Do not use these diodes for voltage clamp purpose as it might damage the IPM.

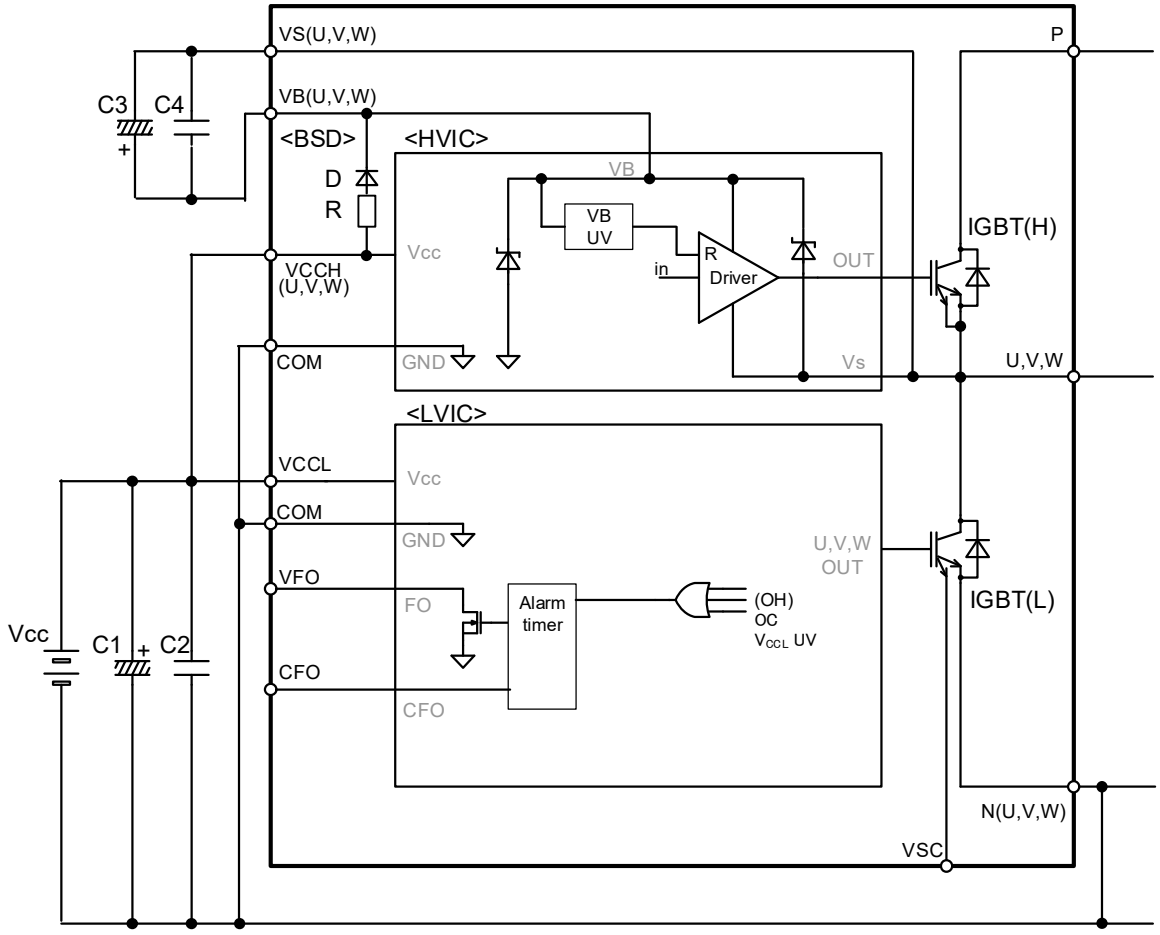

Fig. 3-1 UV protection circuit of high-side and low-side control power supply

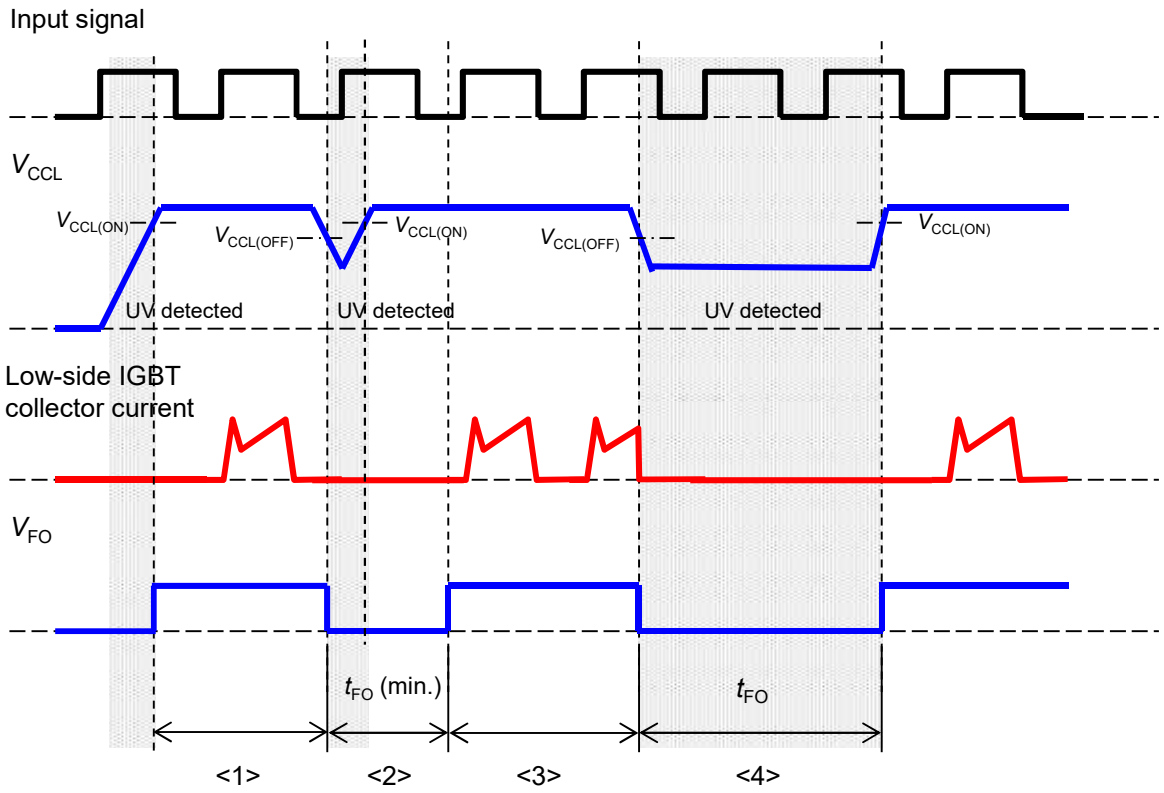

Fig. 3-2 UV protection operation sequence of V_{CCL}

When V_{CCL} is below 4V, UV and fault output are not activated.

<1> When V_{CCL} is below $V_{CCL(ON)}$, all low-side IGBTs are OFF.
When V_{CCL} exceeds $V_{CCL(ON)}$, the fault output voltage V_{FO} is reset from L level to H level.
LVIC starts switching operation from the next input signal.

<2> When V_{CCL} falls below $V_{CCL(OFF)}$, the fault output voltage V_{FO} becomes L level.
All low-side IGBTs are turned off.
If the voltage drop period is less than $t_{FO(min.)}$, the minimum fault output pulse width $t_{FO(min.)}$ is generated. During that period, all low-side IGBTs are turned off regardless of input signal condition.

<3> UV protection is reset after t_{FO} when V_{CCL} exceeds $V_{CCL(ON)}$.
Fault output voltage V_{FO} is also reset.
LVIC restarts switching operation from the next input signal.

<4> If the voltage drop period is longer than t_{FO}, fault output pulse width with the same duration is output. During that period, all low-side IGBTs are turned off regardless of input signal condition.

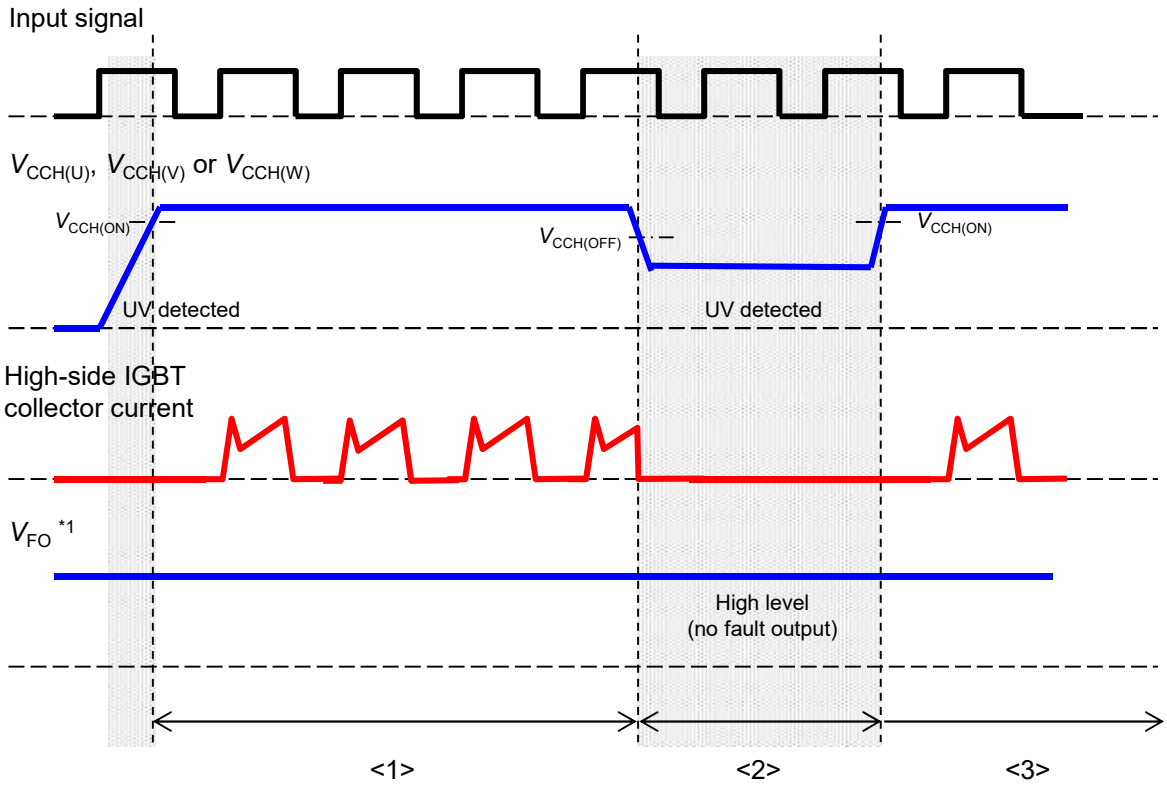

Fig. 3-3 UV protection operation sequence of $V_{CCH(U,V,W)}$

<1> When $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ is below $V_{CCH(ON)}$, the corresponding high-side IGBT is OFF. When $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ exceeds $V_{CCH(ON)}$, HVIC starts switching operation from the next input signal.
The fault output voltage V_{FO} is H level regardless of $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$. *1

<2> When $V_{CCH(U)}$, $V_{CCH(V)}$ or $V_{CCH(W)}$ falls below $V_{CCH(OFF)}$, the corresponding high-side IGBT is turned off.
The fault output voltage V_{FO} remains at H level.

<3> After UV protection is reset, HVIC restarts switching operation from the next input signal.

*1 : The fault output does not depend on the bias condition of the HVIC.

2. High-side Bias Voltage, VB(U,V,W), VS(U,V,W)

1. Voltage range of high-side bias voltage $V_{B(*)}$

The $V_{B(*)}$ voltage, which is the voltage difference between VB(U,V,W) and VS(U,V,W), is the high-side bias voltage for the built-in HVICs. HVIC can drive the high-side IGBTs if the voltage is in the range of 13.0~18.5V. The IPM has UV protection for $V_{B(*)}$ to ensure that the HVICs do not drive the high-side IGBTs when $V_{B(*)}$ voltage drops below a specified voltage. This function prevents the IGBT from operating in a high dissipation mode. Please note that the UV function turns-off only the IGBT of the triggered phase. There is no fault output.

In the case of using bootstrap circuit, the high-side IGBT bias voltage can be generated with the control power supply. Conventionally, high-side IGBT drive circuit requires three independent floating power supplies in addition to the control power supplies.

The high-side bias voltage is charged when the low-side IGBT is turned on or when freewheel current flows at the low-side FWD. Table 3-2 describes the operating state of the IPM for various high-side bias voltages. Connect a low impedance electrolytic capacitor and a smoothing capacitor with good frequency characteristics to the high-side bias voltage as close as possible to the terminals in order to prevent malfunction of this IPM caused by high frequency noise.

When high-side bias voltage $V_{B(U)}$, $V_{B(V)}$, or $V_{B(W)}$ falls below $V_{B(OFF)}$, only the high-side IGBT which UV protection is triggered is turned-off regardless of the input signal condition.

Table 3-2 $V_{B(*)}$ voltage range versus operating state of IPM

Voltage range [V]	Operating state of IPM
0 ~ 4	The IPM does not operate. UV protection does not function. dv/dt noise on P-N(*) power supply might cause malfunction to the IGBTs.
4 ~ 12.5	The IPM starts to operate. UV protection is activated. Input signals are blocked.
12.5 ~ 13	UV protection is reset. High-side IGBTs perform switching operation according to the input signal. Due to the driving voltage is below the recommended range, the conduction losses and switching losses of the IGBTs are larger than normal.
13 ~ 18.5	The IPM operates under recommended operating conditions.
18.5 ~ 20	Due to the driving voltage is above the recommended range, IGBTs are switching faster, which increases the system noise. Even with proper overcurrent protection design, the peak short-circuit current might be too large and lead to destruction.
Over 20	The IPM might be destroyed. It is recommended to connect a Zener diode to each control power supply terminal if necessary.

2. Under voltage (UV) protection of high-side bias voltage $V_{B(*)}$

Fig.3-4 shows the UV protection circuit of high-side bias voltage $V_{B(*)}$.
Fig.3-5 shows the UV protection operation sequence of $V_{B(*)}$.

As shown in Fig.3-4, diodes are electrically connected to the VB(U,V,W), VS(U,V,W) and VB(U,V,W)-COM terminals. These diodes are built-in to protect the IPM from input surge voltage. Do not use these diodes for voltage clamp purpose as it might damage the IPM.

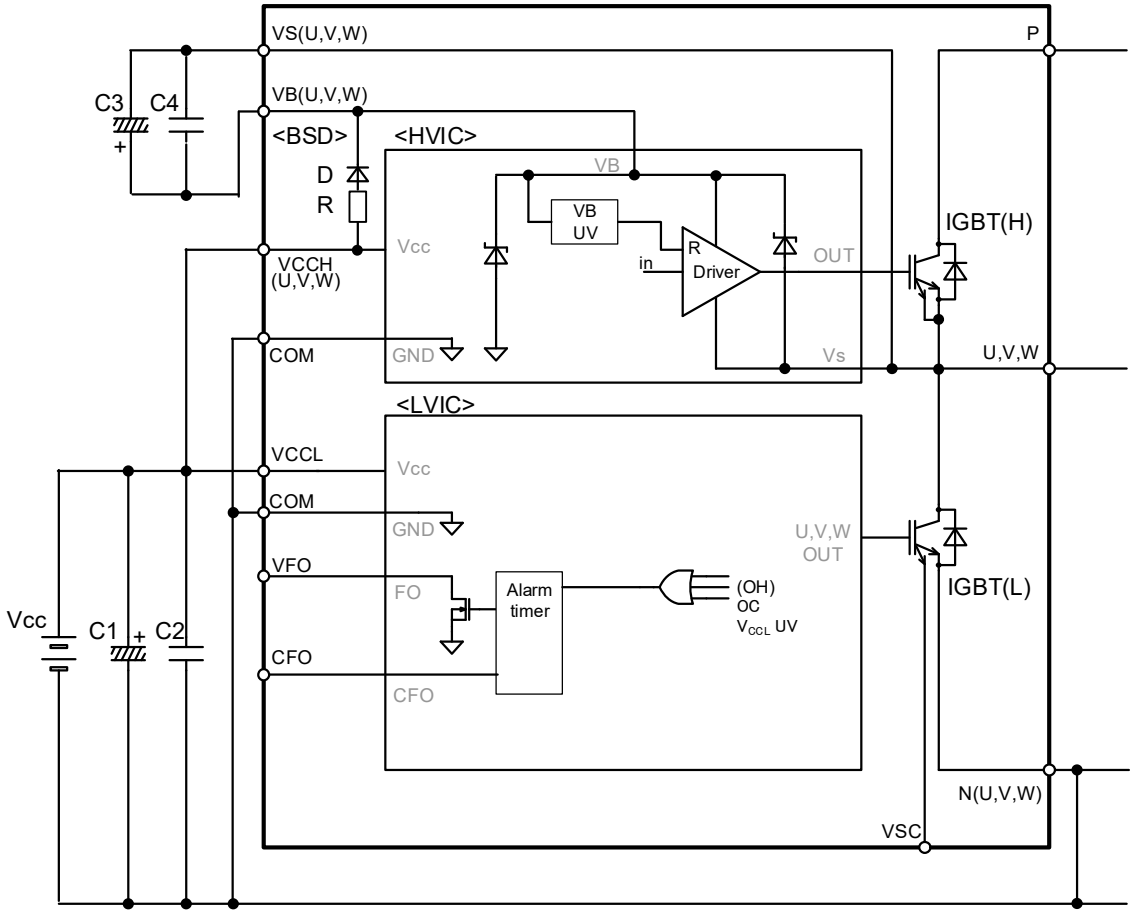

Fig. 3-4 UV protection circuit of high-side bias voltage

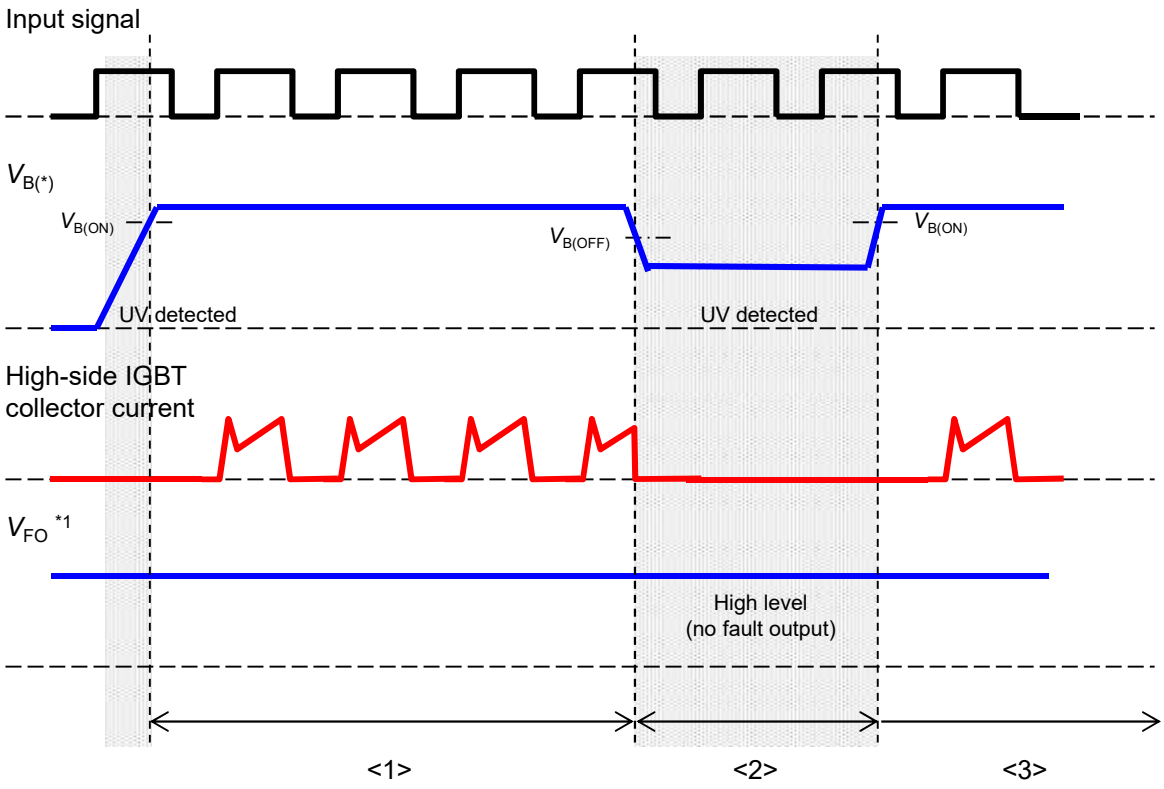

Fig. 3-5 UV protection operation sequence of $V_{B(*)}$

<1> When $V_{B(U)}$, $V_{B(V)}$ or $V_{B(W)}$ is below $V_{B(ON)}$, the corresponding high-side IGBT is OFF.
When $V_{B(*)}$ exceeds $V_{B(ON)}$, HVIC starts switching operation from the next input signal.
The fault output voltage V_{FO} is H level regardless of $V_{B(*)}$. *1

<2> When $V_{B(U)}$, $V_{B(V)}$ or $V_{B(W)}$ falls below $V_{B(OFF)}$, the corresponding high-side IGBT is turned off.
The fault output voltage V_{FO} remains at H level.

<3> After UV protection is reset, HVIC restarts switching operation from the next input signal.

*1 : The fault output does not depend on the bias condition of the HVIC.

3. Function of Built-in BSDs (Bootstrap Diodes)

There are several ways to generate high-side bias voltage $V_{B(*)}$ (VB(U)-VS(U), VB(V)-VS(V), VB(W)-VS(W) voltage). This IPM can configure a bootstrap circuit by using the built-in BSDs. When configuring the bootstrap circuit, it is necessary to set the duty ratio and on-time according to the bootstrap capacitor and the charging operation conditions.

1. Bootstrap circuit operation

<Low-side IGBT ON (Fig. 3-6) : timing chart (Fig. 3-7)>

When low-side IGBT is ON, the high-side bias voltage $V_{B(*)}(t1)$ from the charging operation of the bootstrap capacitor can be expressed by the following equations.

$V_{B(*)}(t1) = V_{CC}\text{-}V_F\text{-}V_{CE(sat)}\text{-}I_B\cdot R$ …… transient state
$V_{B(*)}(t1) \approx V_{CC}$ …….. steady state

V_F : Forward voltage of BSD (D)
$V_{CE(sat)}$: Saturation voltage of low-side IGBT
R : Bootstrap circuit resistance (R)
I_B : Charging current of bootstrap circuit

When low-side IGBT is turned off, the motor current flows to the high-side FWD. When the V_S potential rises above V_{CC}, the charging of C stops, and $V_{B(*)}$ gradually decreases due to current consumption by the high-side control power supply.

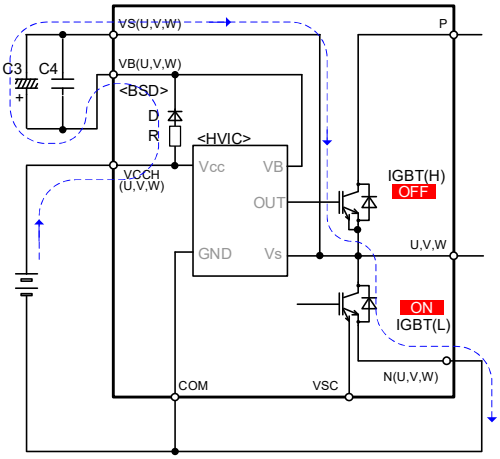

Fig. 3-6 Circuit diagram of charging operation when low-side IGBT is ON

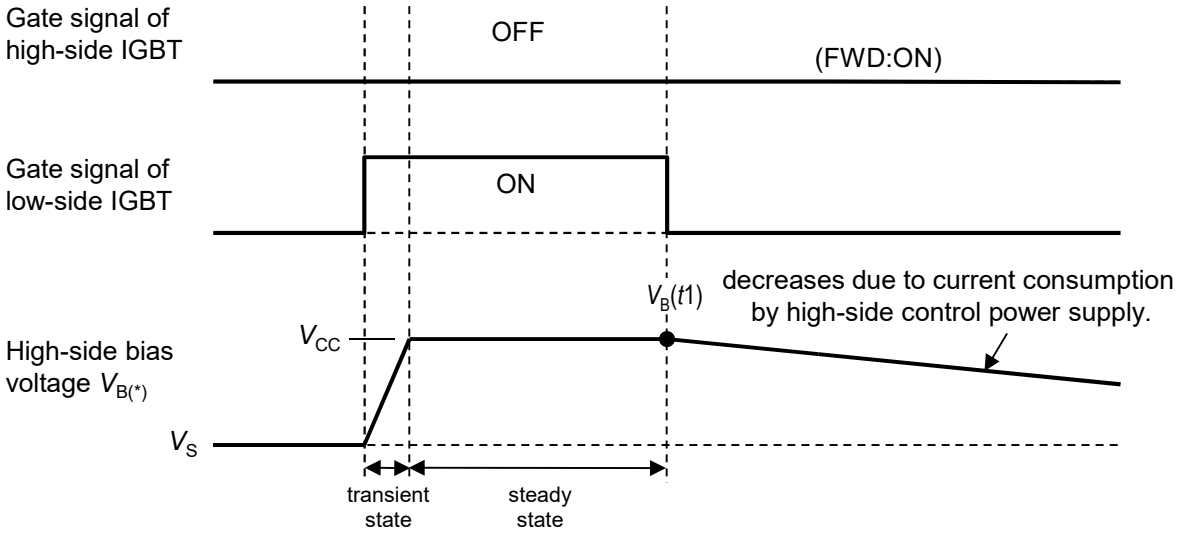

Fig. 3-7 Timing chart of charging operation when low-side IGBT is ON

<Low-side IGBT OFF, low-side FWD ON (freewheeling) (Fig. 3-8) : sequence (Fig. 3-9)>

When low-side IGBT is OFF and low-side FWD is ON, freewheel current flows through the low-side FWD. The high-side bias voltage $V_{B(*)}(t2)$ from the charging operation of the bootstrap capacitor can be expressed by the following equations.

$V_{B(*)}(t2) = V_{CC}-V_F+V_{F(FWD)}-I_B \cdot R$ …… transient state
$V_{B(*)}(t2) \approx V_{CC}$ …… steady state

V_F : Forward voltage of BSD (D)
$V_{F(FWD)}$: Forward voltage of low-side FWD
R : Bootstrap circuit resistance (R)
I_B : Charging current of bootstrap circuit

When both the low-side and high-side IGBTs are OFF, the regenerative current flows through the low-side FWD. Therefore, the V_S potential drops to $-V_F$ of FWD, and the bootstrap capacitor is recharged. When the high-side IGBT is turned on and the V_S potential rises above V_{CC}, the charging of C stops, and $V_{B(*)}$ gradually decreases due to current consumption by the high-side control power supply.

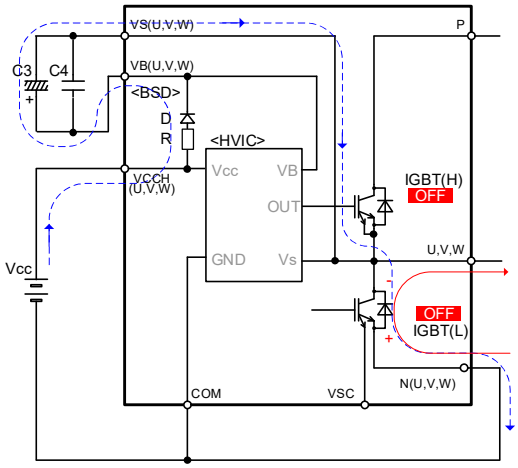

Fig. 3-8 Circuit diagram of charging operation when low-side FWD is ON

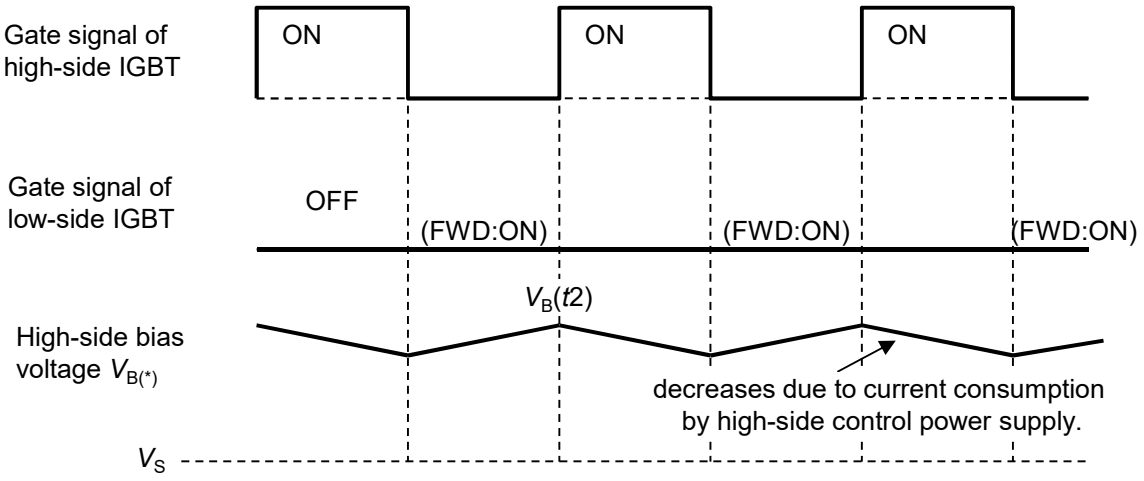

Fig. 3-9 Timing chart of charging operation when low-side FWD is ON

2. Setting of bootstrap operating conditions

2.1 Setting the bootstrap capacitance and minimum ON/OFF pulse width

The bootstrap capacitance can be determined by the following equation:

$$C = I_{CCHB} \cdot \frac{t1}{dV}$$

* $t1$: the maximum ON pulse width of the high-side IGBT
* I_{CCHB} : consumption current of high-side drive power supply (temperature and frequency dependent)
* dV : allowable discharge voltage of $V_{B(*)}$ (refer to Fig.3-10)

Certain margin should be added to the calculated capacitance.
In general, select a capacitor that is two to three times of the calculated result.
The recommended minimum ON pulse width ($t2$) of the low-side IGBT should be determined such that the time constant $R \cdot C$ will enable the discharged voltage (dV) to be fully recharged again during the ON period.
In the case of the control mode which only the high-side IGBT performs switching operation (Fig. 3-10), the time constant should be set so that the discharged voltage can be fully recharged again during the high-side IGBT OFF (low-side FWD ON) period.
The minimum pulse width is decided by the minimum ON pulse width of the low-side IGBT, or the minimum OFF pulse width of the high-side IGBT, whichever is longer.

$$t2 \geq \frac{R \cdot C \cdot dV}{V_{CC} - V_B(\min)}$$

* $t2$: Minimum ON pulse width of low-side IGBT
* R : Bootstrap circuit resistance $R_{(BSD)}$ (refer to Fig. 3-11, Fig. 3-12)
* C : Bootstrap capacitance
* dV : Allowable discharge voltage of $V_{B(*)}$
* V_{CC} : Voltage of high-side, low-side control power supply (ex.15V)
* $V_B(\min)$: Minimum voltage of high-side bias voltage (add margin to $V_{B(ON)}$, ex.14V)

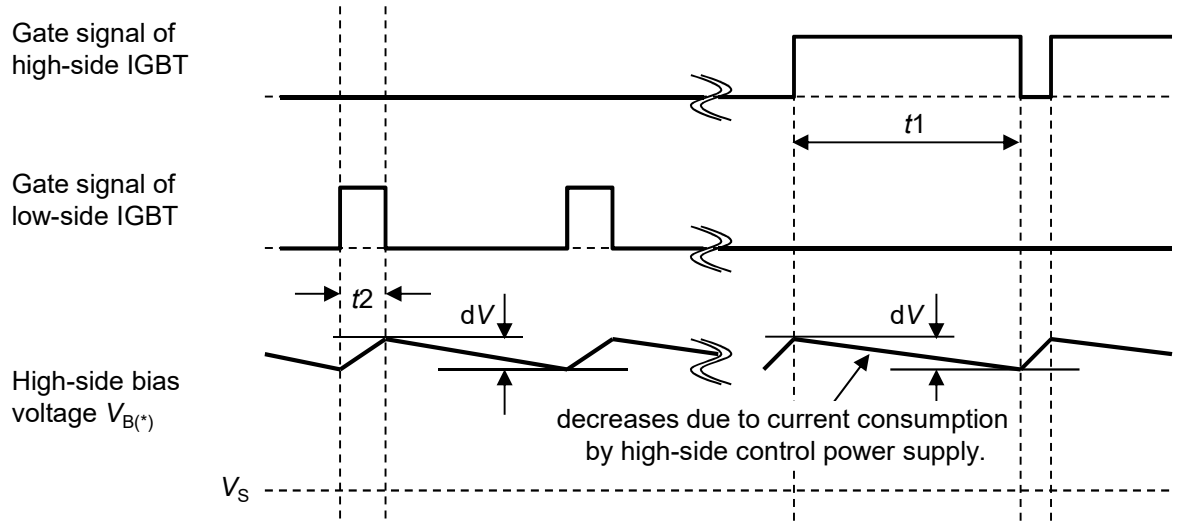

Fig. 3-10 Timing chart of charging and discharging operation

The bootstrap diode has built-in current limiting resistor of 20Ω (typ.). Fig. 3-11 and Fig. 3-12 show the V_F-I_F characteristics of the bootstrap diode.

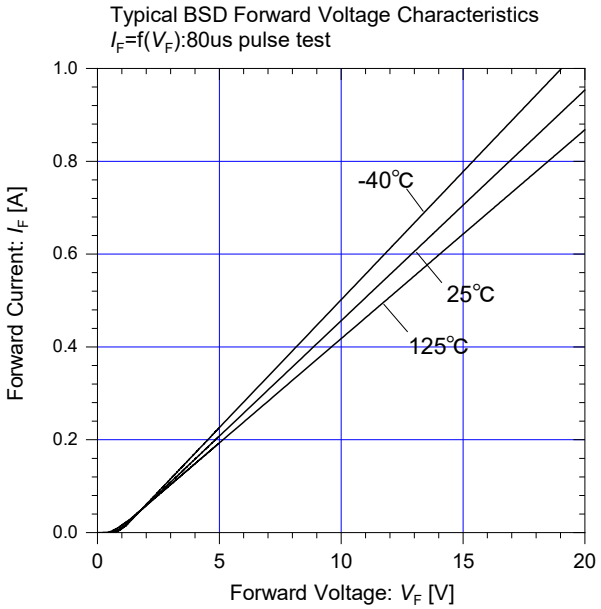

Fig. 3-11 V_F-I_F characteristic of BSD

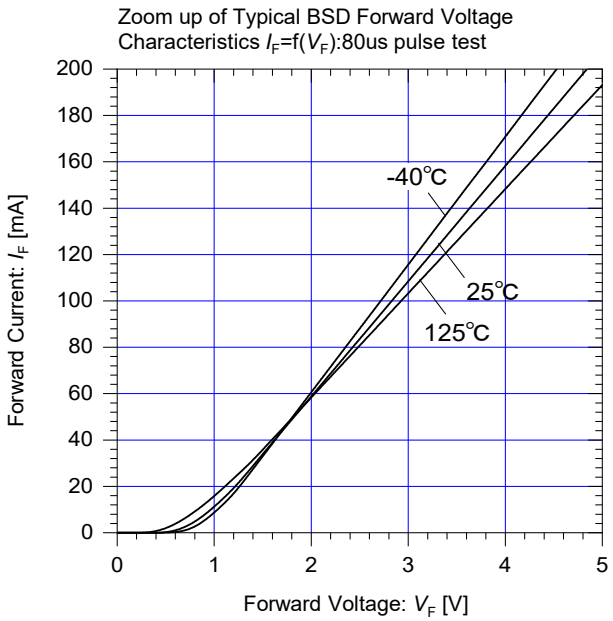

Fig. 3-12 V_F-I_F characteristic of BSD (zoom at low current range)

2.2 Setting the initial charging of bootstrap capacitor

Initial charging of the bootstrap capacitor is required to start the inverter.

The pulse width or the number of pulses should be long enough to fully charge the bootstrap capacitor.

For reference, it takes about 10ms to charge a 47uF capacitor through the built-in bootstrap diode.

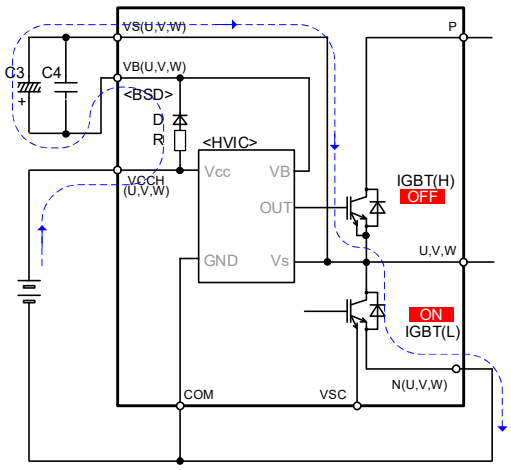

Fig. 3-13 Circuit diagram of initial charging operation

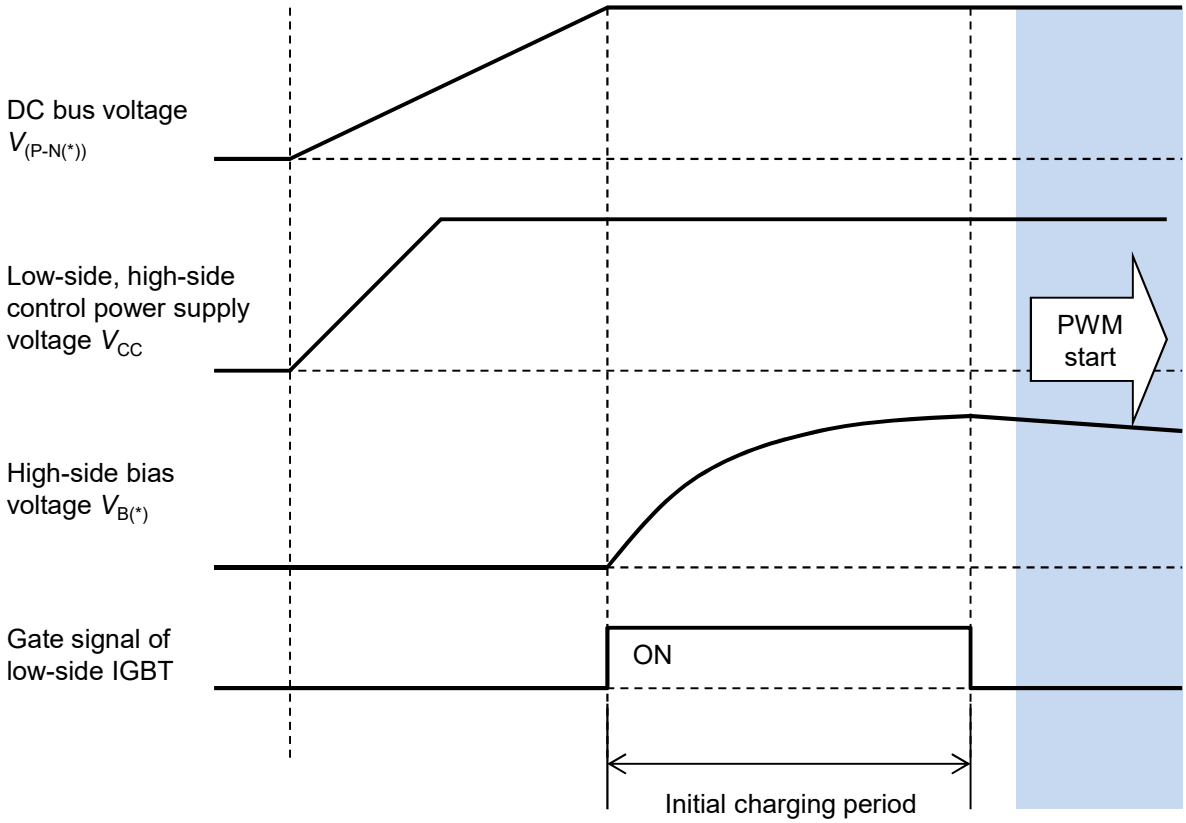

Fig. 3-14 Timing chart of initial charging operation

4. Signal Input, IN(HU,HV,HW), IN(LU,LV,LW)

1. Input terminals connection

Fig. 3-15 shows an example of interface circuit between MPU and the IPM. The input terminals can be connected directly to the MPU. The input terminals have built-in pull-down resistors, so there is no need for external pull-down resistors. Also, the input logic is high active, thus there is no need for external pull-up resistors.

Insert RC filter circuit as shown by the dotted line in Fig. 3-15 if noise is superimposed on long signal wire. Adjust the RC constant according to the PWM control method and the wiring pattern of the printed circuit board.

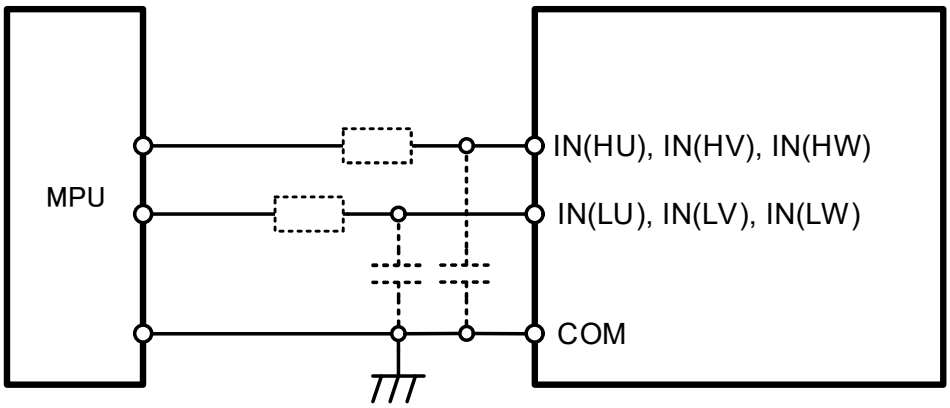

Fig. 3-15 Recommended MPU I/O interface circuit of IN(HU,HV,HW), IN(LU,LV,LW) terminals

2. Input terminals circuit

The input logic of this IPM is high active. Thus, the input signal has no restriction on the power supply startup and shutdown sequence, so the system is fail safe. In addition, as shown in Fig. 3-16, the input terminals have built-in pull-down resistors, thus there is no need for external pull-down resistors, reducing the number of system components. Furthermore, a 3.3V-class MPU can be connected directly since the input signal threshold voltage is low.

In the case of connecting an external filter resistor between the MPU and the input terminal of the IPM, make sure that the input terminal voltage is above the input signal threshold voltage in consideration of the built-in pull-down resistor.

As shown in Fig.3-16, diodes are electrically connected to the VCCL-IN(HU,HV,HW,LU,LV,LW) and IN(HU,HV,HW,LU,LV,LW)-COM terminals. These diodes are built-in to protect the IPM from input surge voltage. Do not use these diodes for voltage clamp purpose as it might damage the IPM.

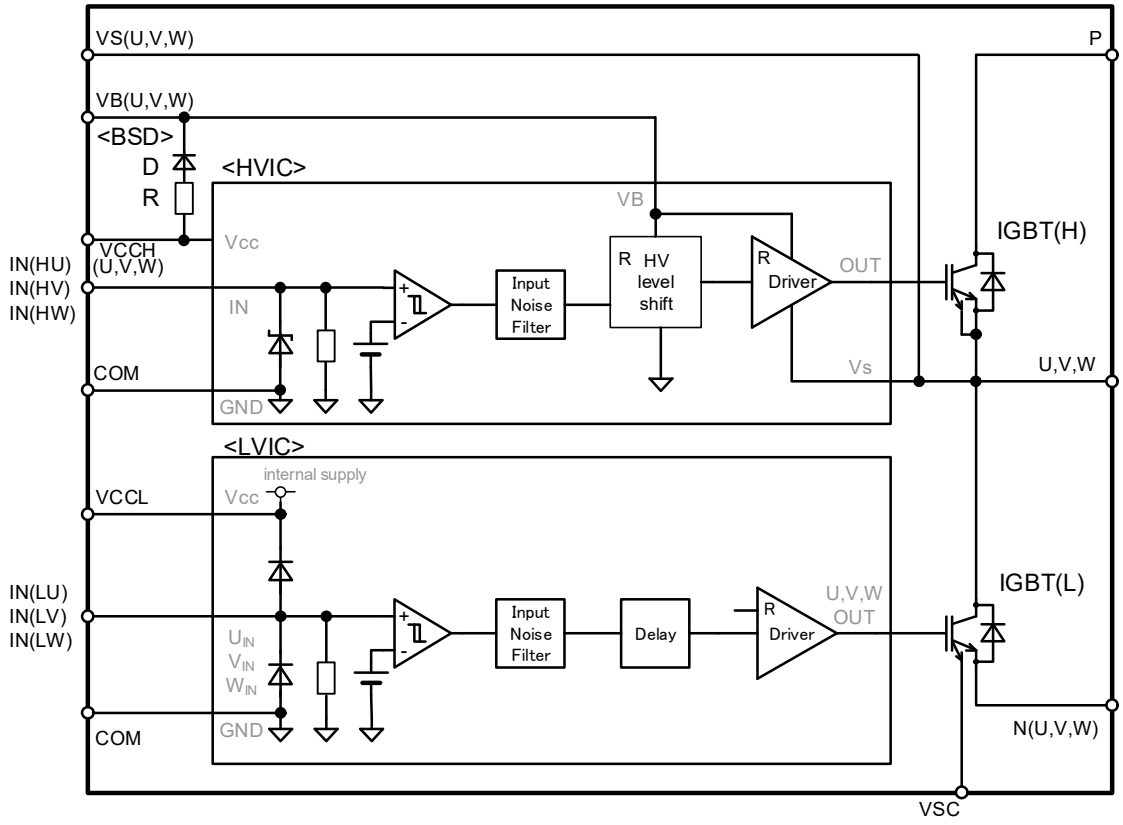

Fig.3-16 Circuit of IN(HU,HV,HW), IN(LU,LV,LW) terminals

3. IGBT drive state and input signal pulse width

$t_{IN(on)}$ is the recommended minimum ON pulse width required to turn-on the IGBT without malfunction, and $t_{IN(off)}$ is the recommended minimum OFF pulse width required to turn-off the IGBT without malfunction. Fig. 3-17 and Fig. 3-18 show the IGBT drive state at various input signal pulse width.

A : IGBT might turn-on even when the input signal ON pulse width is less than minimum $t_{IN(on)}$.
In the case of input signal ON pulse width is less than minimum $t_{IN(on)}$ and a voltage below -5V is applied between U-COM, V-COM, W-COM terminals, not only the IPM might be broken but also the IGBT might not turn-off due to malfunction of the control circuit.

B : In steady state operation. IGBT operates in the linear region.

C : IGBT might turn-off even when the input signal OFF pulse width is less than minimum $t_{IN(off)}$.
In the case of input signal OFF pulse width is less than minimum $t_{IN(off)}$ and a voltage below -5V is applied between U-COM, V-COM, W-COM terminals, not only the IPM might be broken but also the IGBT might not turn-on due to malfunction of the control circuit.

D : In steady state operation. IGBT is completely turned off.

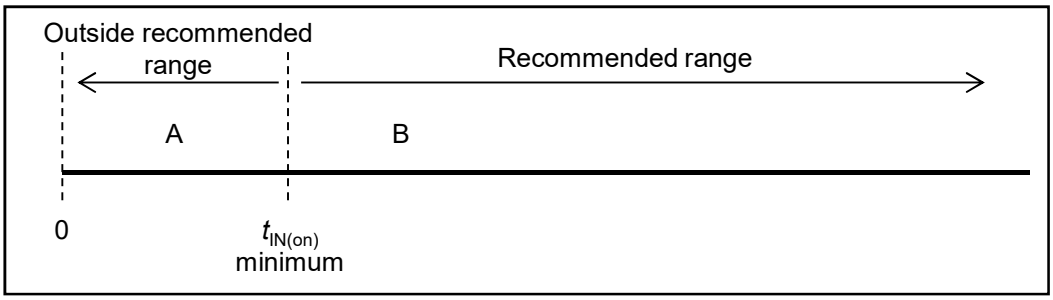

Fig. 3-17 IGBT drive state versus input signal ON pulse width

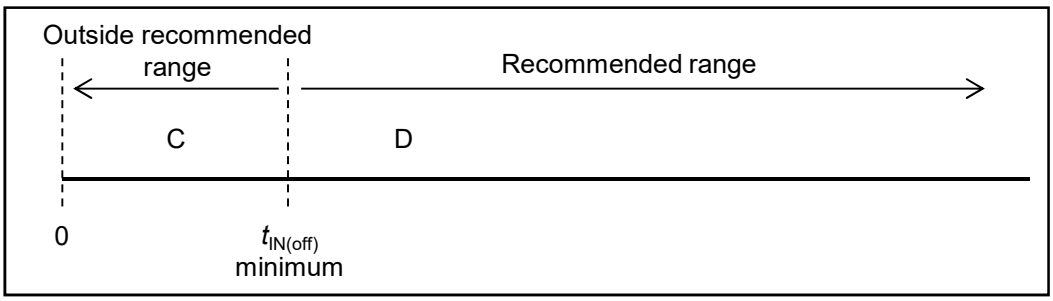

Fig. 3-18 IGBT drive state versus input signal OFF pulse width

5. Overcurrent Protection Function, IS

1. Input terminals connection

The overcurrent (OC) protection works by detecting the voltage generated at the external shunt resistor connected between N(*) *1 and COM terminal, or the voltage generated at the sense resistor connected between VSC and COM terminal, and input to IS terminal. When this voltage exceeds $V_{IS(ref)}$, all low-side IGBTs are turned-off and fault output is generated.

Fig. 3-19 shows the OC protection detection circuit of IS terminal. Fig. 3-20 shows the OC protection operation sequence.

To prevent the IPM from unnecessary operations due to switching noise or recovery current during normal operation, it is recommended to insert an external RC filter (time constant is approximately 1.5μs) to the IS terminal. Keep the wiring between the IPM and the shunt resistor as short as possible too.

As shown in Fig. 3-19, diodes are electrically connected between VCCL-IS and IS-COM terminals. These diodes are built-in to protect the IPM from input surge voltage. Do not use these diodes for voltage clamp purpose as it might damage the IPM.

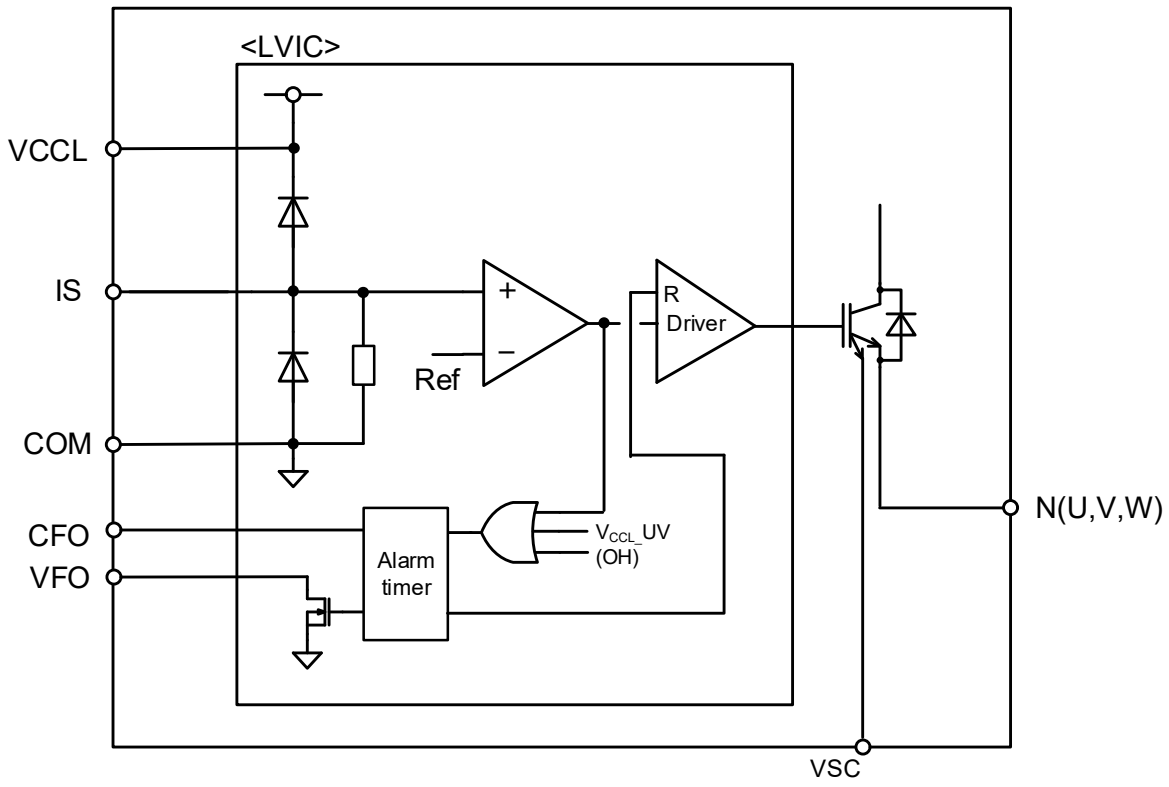

Fig. 3-19 OC protection detection circuit of IS terminal

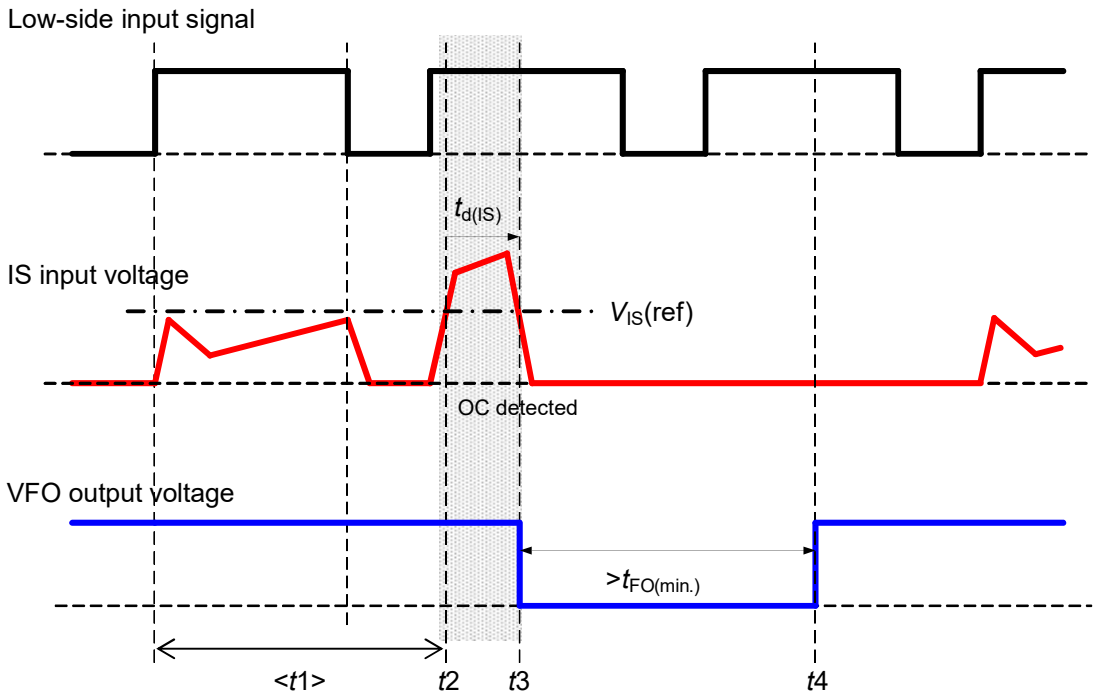

Fig. 3-20 OC protection operation sequence

<*t*1> : The IS input voltage is less than $V_{IS(ref)}$. All low-side IGBTs perform normal switching operation.

*t*2 : When IS input voltage exceeds $V_{IS(ref)}$, OC is detected.

*t*3 : Fault output voltage is generated and all low-side IGBTs are turned off after the overcurrent protection delay time $t_{d(IS)}$. Propagation delay of LVIC is included in $t_{d(IS)}$.

*t*4 : OC protection is reset after t_{FO}. LVIC restarts switching operation from the next input signal.

6. Fault Status Output Function, VFO, CFO

As shown in Fig. 3-21, it is possible to connect the fault status output terminal VFO directly to the MPU. The VFO terminal is open drain configured, thus this terminal should be pulled up to 5V or 3.3V DC logic power supply with a resistor of about 10kΩ. It is also recommended to connect a bypass capacitor C1 and inrush current limiting resistor R1 of 5kΩ or more between the MPU and the VFO terminal. These signal lines should be as short as possible.

VFO terminal outputs fault status alarm during UV protection of V_{CCL}, OC protection, and OH protection. (OH protection is built into “6MBP ** XTC065-50”)

The pulse width of the fault status output (t_{FO}) can be adjusted by the capacitance of the capacitor between CFO and COM terminal. The fault status output pulse width is 2.4ms when the capacitor capacitance is 22nF. C_{FO} is given by C_{FO} (typ.) = t_{FO} x (9.1 x 10-6) (F).

As shown in Fig. 3-21, diodes are electrically connected between VCCL-VFO and VFO-COM terminals. These diodes are built-in to protect the IPM from input surge voltage. Do not use these diodes for voltage clamp purpose as it might damage the IPM.

Fig. 3-22 shows the voltage-current characteristics of VFO terminal during fault status output. I_{FO} is the sink current of VFO terminal.

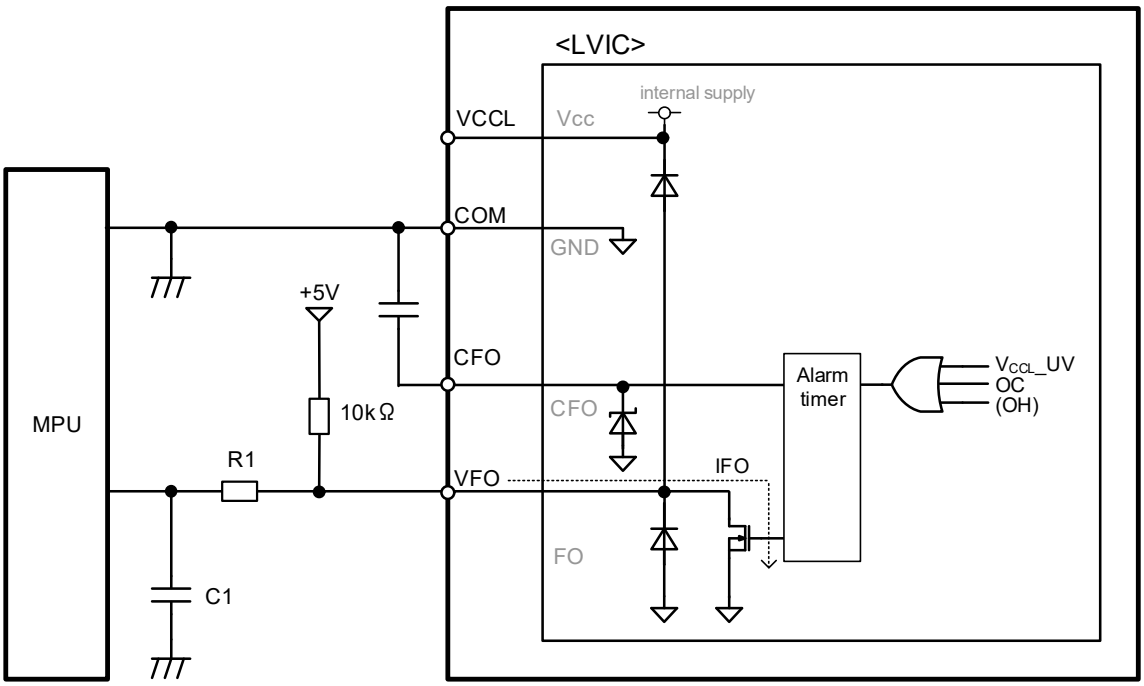

Fig. 3-21 Recommended MPU I/O interface circuit of VFO terminal

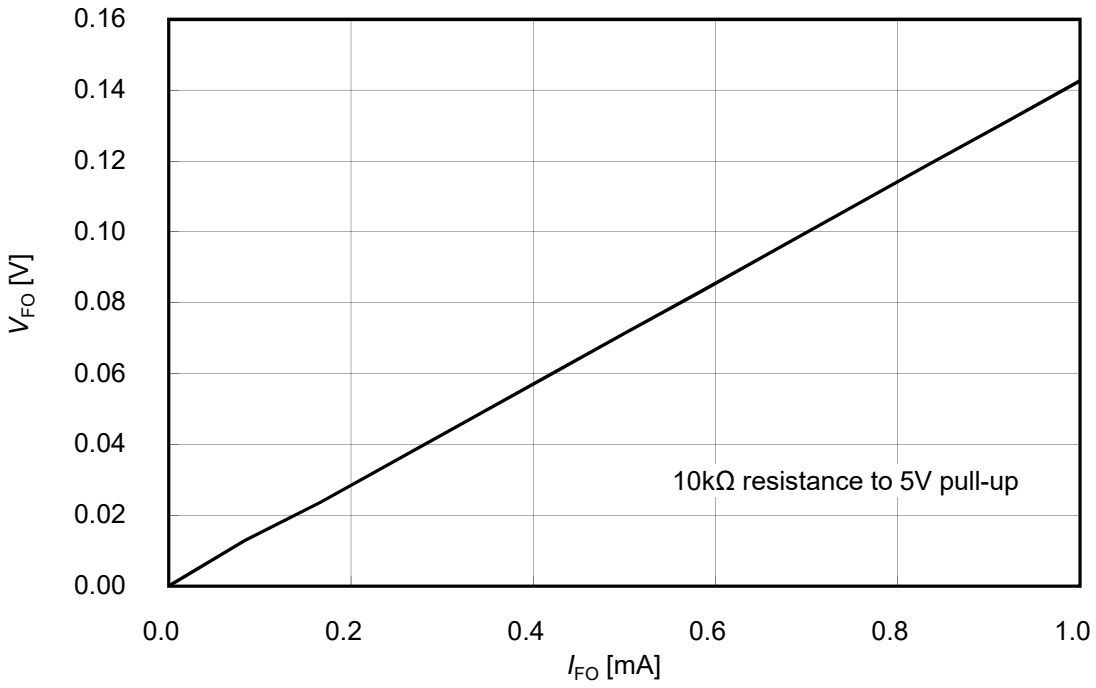

Fig. 3-22 Voltage-current characteristics of VFO terminal during fault status output

7. Temperature Output Function, TEMP

As shown in Fig. 3-23, the temperature output terminal TEMP can be connected directly to the MPU. It is recommended to connect a bypass capacitor and an inrush current limiting resistor of 10kΩ or more between the MPU and the TEMP terminal. These signal lines should be as short as possible.

This IPM has a built-in temperature sensor in LVIC that outputs analog voltage according to the LVIC virtual junction temperature. This function has no fault status output because it is not intended to protect the IPM. "6MBP ** XTC065-50" has built-in overheating (OH) protection. Fault status output is generated when the temperature exceeds T_{OH}.

As shown in Fig. 3-23, a diode is electrically connected between the TEMP-COM terminals. This diode is built-in to protect the IPM from input surge voltage. Do not use this diode for voltage clamp purpose as it might damage the IPM.

Fig. 3-24 shows the LVIC virtual junction temperature versus TEMP output voltage characteristics. In the case of the MPU power supply voltage is 3.3V, connect a Zener diode to the TEMP terminal. The output voltage shows clamp characteristic at below room temperature. Connect a 5kΩ±10% pull-down resistor to the TEMP terminal if linear characteristic is required. Fig. 3-25 shows the LVIC virtual junction temperature versus TEMP output voltage characteristics with 5kΩ pull-down resistor.

Fig. 3-26 shows the operation sequence of the TEMP terminal during startup and shutdown of IPM.

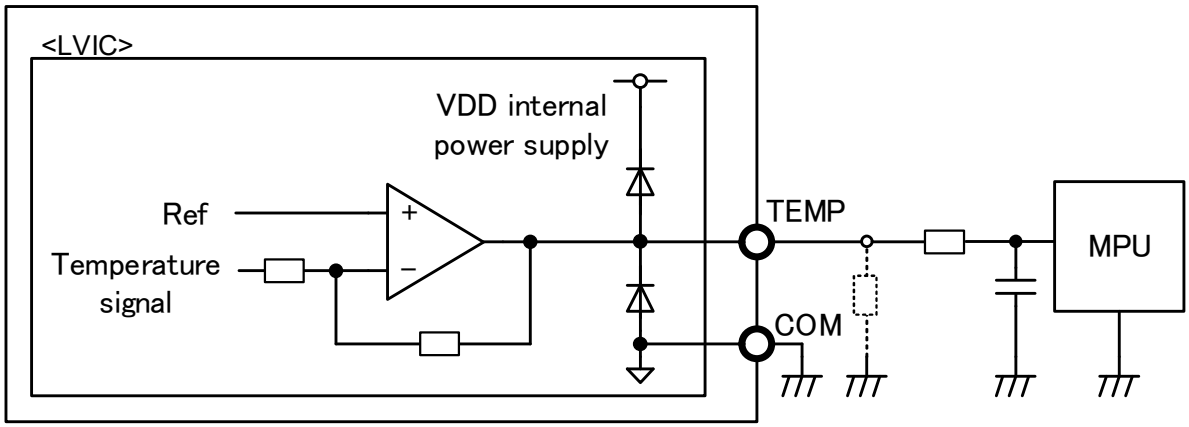

Fig. 3-23 Recommended MPU I/O interface circuit of TEMP terminal

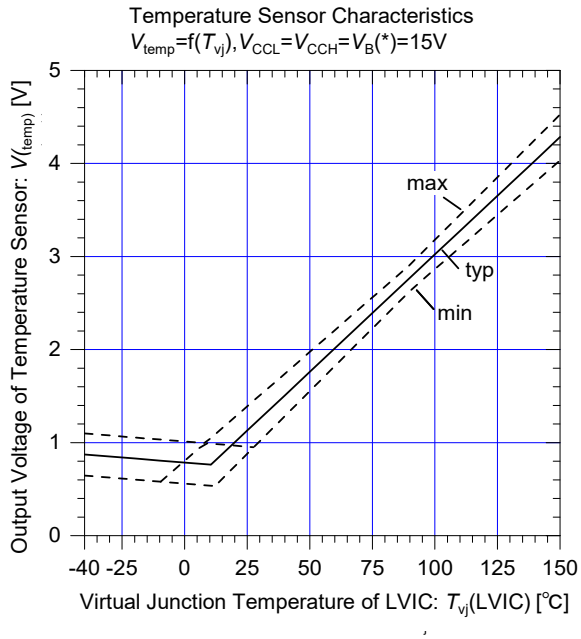

Fig. 3-24 LVIC virtual junction temperature vs. TEMP output voltage characteristic (without pull-down resistor)

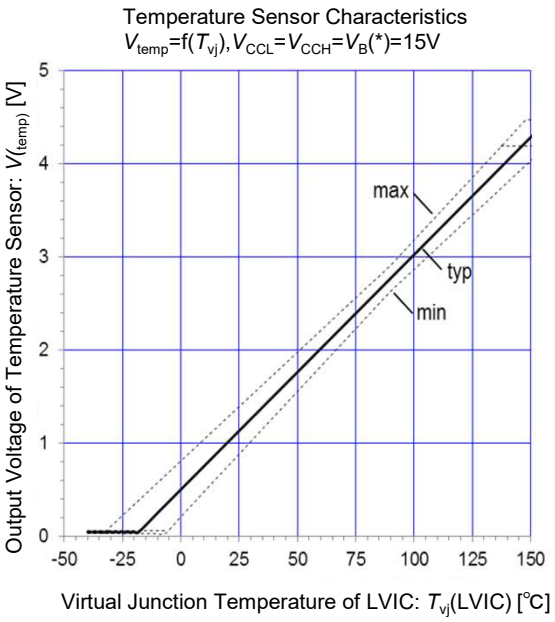

Fig. 3-25 LVIC virtual junction temperature vs. TEMP output voltage characteristic (with 5kΩ pull-down resistor)

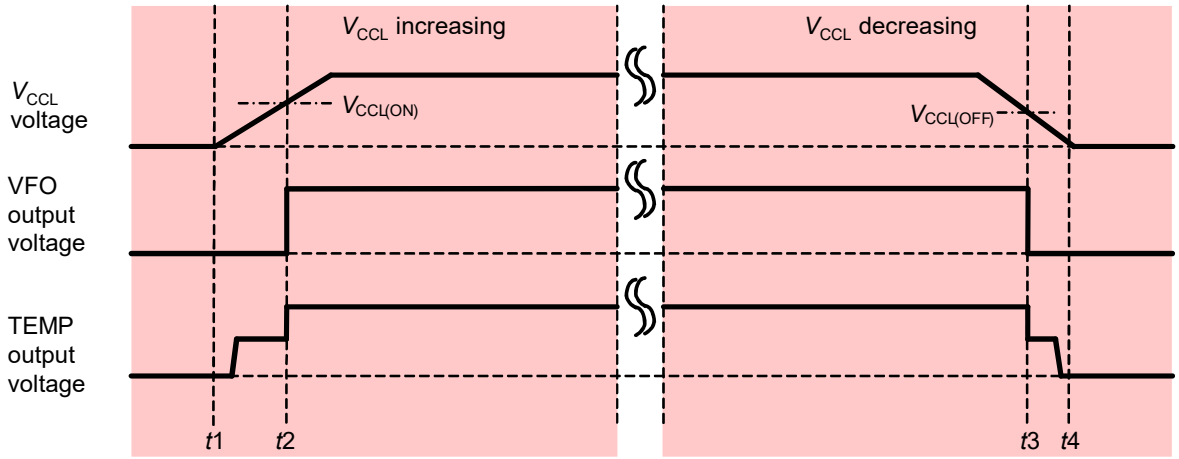

Fig. 3-26 Operation sequence of TEMP terminal during startup and shutdown of IPM

*t*1-*t*2 : TEMP output function is activated when V_{CCL} exceeds $V_{CCL(ON)}$. When V_{CCL} is lower than $V_{CCL\ (ON)}$, TEMP output voltage is the same as clamp voltage.

*t*2-*t*3 : TEMP output voltage rises to the voltage determined by LVIC virtual junction temperature. Under temperature condition that cause clamp operation, TEMP output voltage is the same as clamp voltage even if V_{CCL} exceeds $V_{CCL\ (ON)}$.

*t*3-*t*4 : TEMP output function is reset when V_{CCL} falls below $V_{CCL(OFF)}$. TEMP output voltage is the same as clamp voltage.

8. Overheating Protection Function

The overheating (OH) protection function is built in “6MBP ** XTC065-50”.

The OH function monitors the LVIC virtual junction temperature.

Fig. 2-3 shows the position of the T_{OH} sensor.

As shown in Fig. 3-27, when LVIC virtual junction temperature exceeds T_{OH}, all low-side IGBTs are turned-off. If LVIC virtual junction temperature falls below T_{OH}–$T_{OH(hys)}$, OH function is reset.

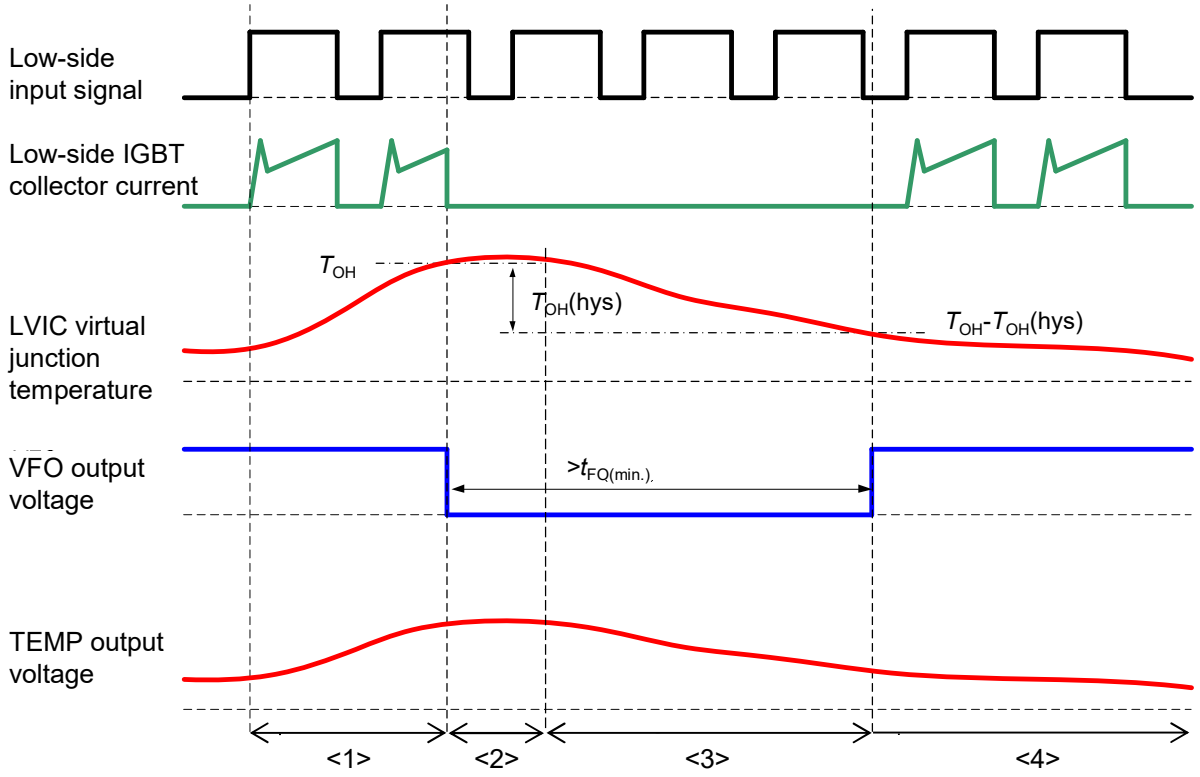

Fig. 3-27 OH protection operation sequence

<1> : When LVIC virtual junction temperature is below T_{OH}, all low-side IGBTs operate normally.

<2> : While LVIC virtual junction temperature is above T_{OH}, all low-side IGBTs are turned off.

<3> : During OH protection status, TEMP terminal continues to output voltage corresponding to LVIC virtual junction temperature.

<4> : Fault status and OH protection status are reset after LVIC virtual junction temperature falls below T_{OH}-$T_{OH(hys)}$ and t_{FO} has elapsed. The low-side IGBTs restart operation from the next input signal. $T_{OH(hys)}$ is the hysteresis temperature of overheating protection.