
Chapter 5

Recommended wiring and layout

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1. Examples of Application Circuits

In this chapter, recommended wiring and layout are explained
In this section, tips and precautions in PCB design are described with example of application circuit.

Fig. 5-1 and Fig.5-2 show examples of application circuits and their notes.
In these figures, although two types of current detection method are shown, the notes are common.

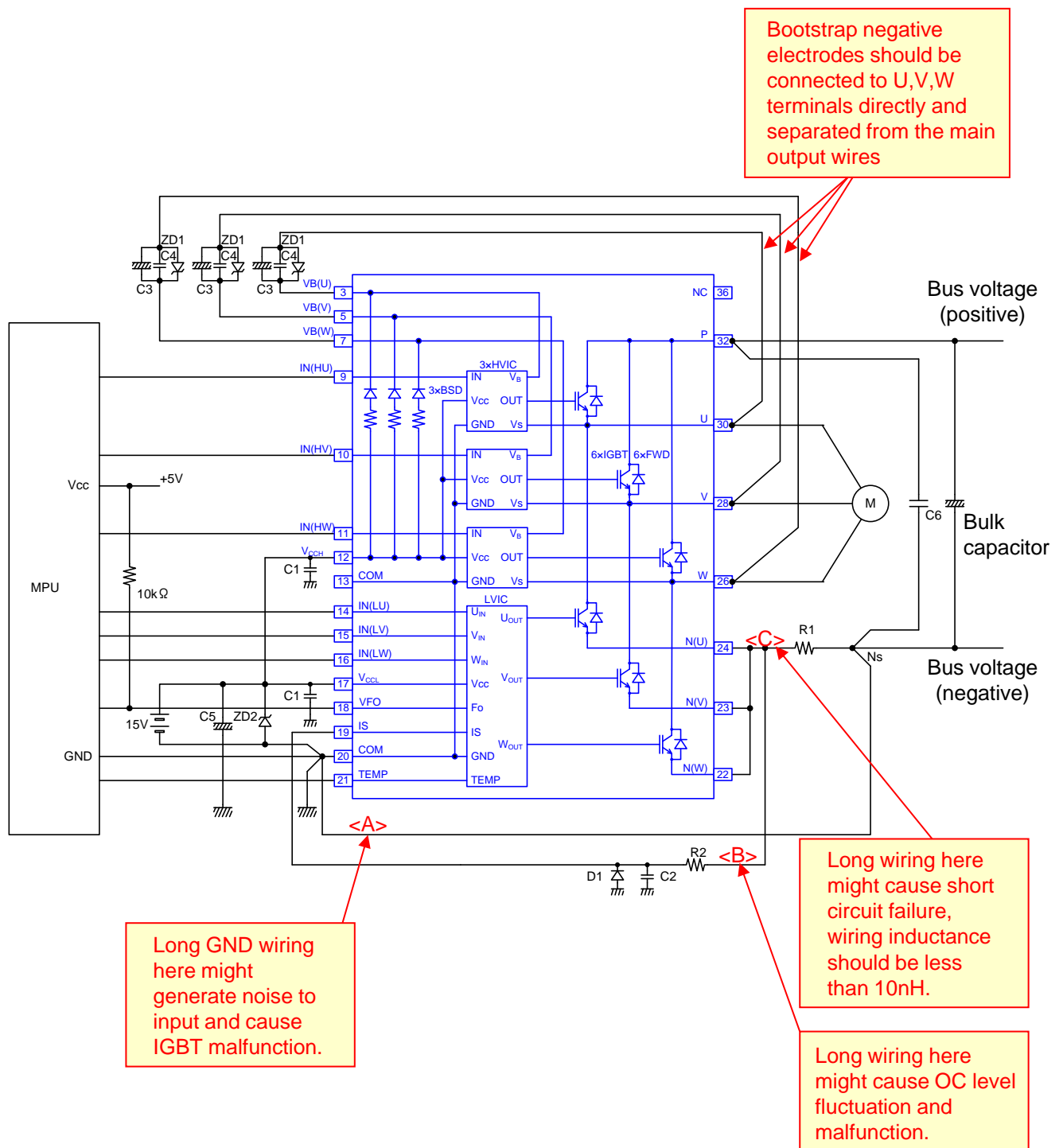


Fig. 5-1 Example of application circuit 1
(In case of sensing all 3 phase currents at once with a single shunt resistor)

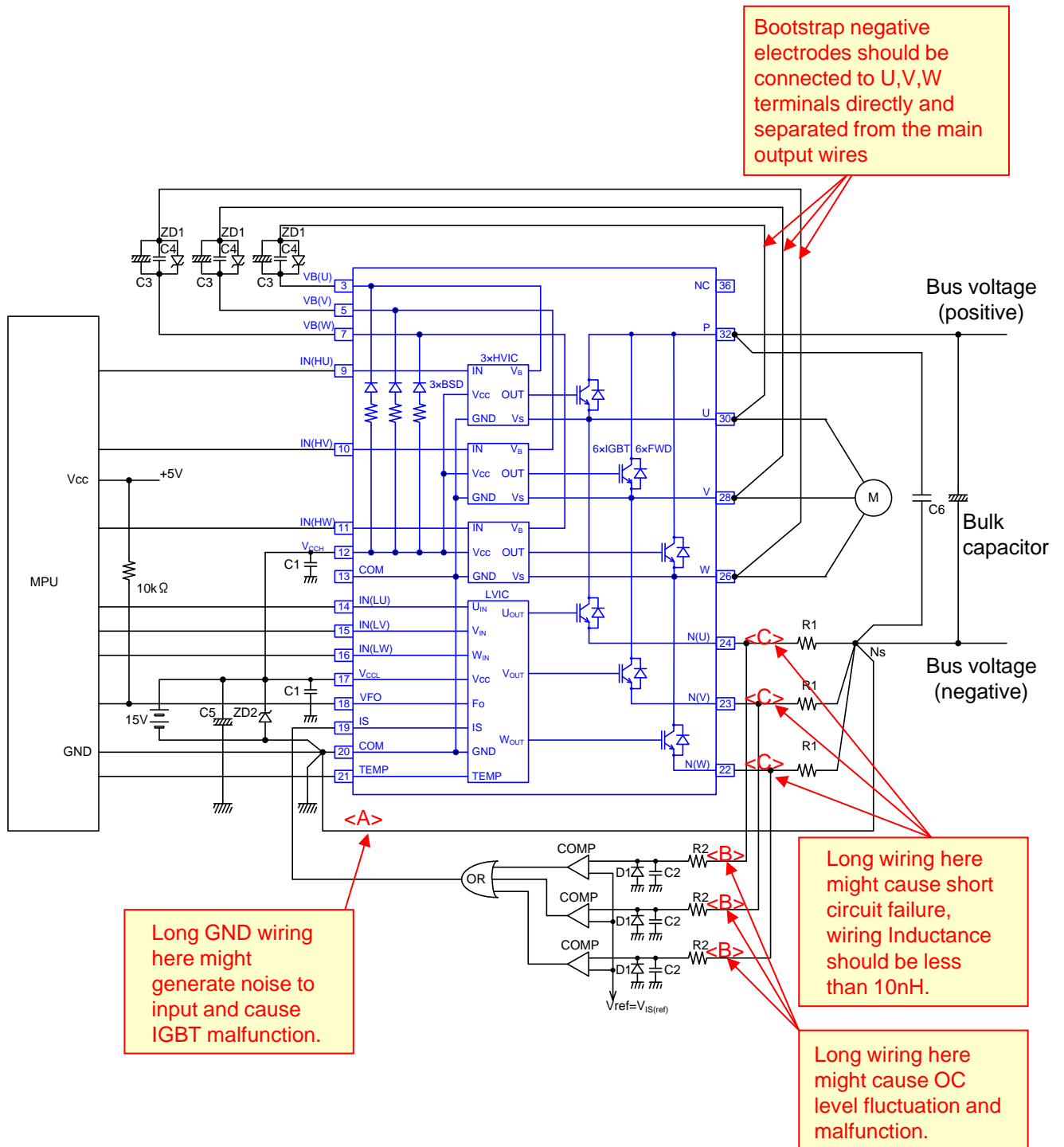


Fig. 5-2 Example of application circuit 2
(In case of sensing each phase current individually)

<Note>

1. Input signal for IGBT driving is High-Active. The input circuit of the IC has a built-in pull-down resistor. To prevent malfunction, the wiring of each input should be as short as possible. When using RC filter, please make sure that the input signal level meets the turn-on and turn-off threshold voltage.
2. The IPM has built-in HVICs and thus it is possible to be connected to a microprocessor (MPU) directly without any photocoupler or pulse transformer.
3. VFO output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10k Ω .
4. To prevent erroneous protection, the wiring of (A), (B), (C) should be as short as possible.
5. The time constant R2-C2 of the protection circuit should be selected approximately 1.5 μ s. Over current (OC) shut down time might vary due to the wiring pattern. Tight tolerance, temp-compensated type is recommended for R2, C2.
6. It is recommended to set the threshold voltage of the comparator reference input to be same level as the IPM OC trip reference voltage $V_{IS(ref)}$.
7. Please use high speed type comparator and logic IC to detect OC condition quickly.
8. If negative voltage is applied to R1 during switching operation, connecting a Schottky barrier diode D1 is recommended.
9. All capacitors should be connected as close to the terminals of the IPM as possible. (C1, C4: ceramic capacitors with excellent temperature, frequency and DC bias characteristics are recommended; C3, C5: electrolytic capacitors with excellent temperature and frequency characteristics are recommended.)
10. To prevent destruction caused by surge voltage, the wiring between the snubber capacitor C6 and P terminal, Ns node should be as short as possible. Generally, snubber capacity of 0.1 μ F~0.22 μ F is recommended.
11. Two COM terminals (9 & 16 pin) are connected internally. Please connect either of the terminal to the signal GND and leave the other terminal open.
12. It is recommended to connect a Zener diode (22V) between each pair of control power supply terminals to prevent destruction caused by surge voltage.
13. If signal GND is connected to power GND by board pattern, there is possibility of malfunction due to fluctuations at the power GND. It is recommended to connect signal GND and power GND at a single point.

2. Recommendations and Precautions in PCB design

In this section, the recommended pattern layout and precautions in PCB design are described.

Fig.5-3 to Fig.5-7 show the images of recommended PCB layout (referring to example application circuit in Fig.5-1 and Fig.5-2).

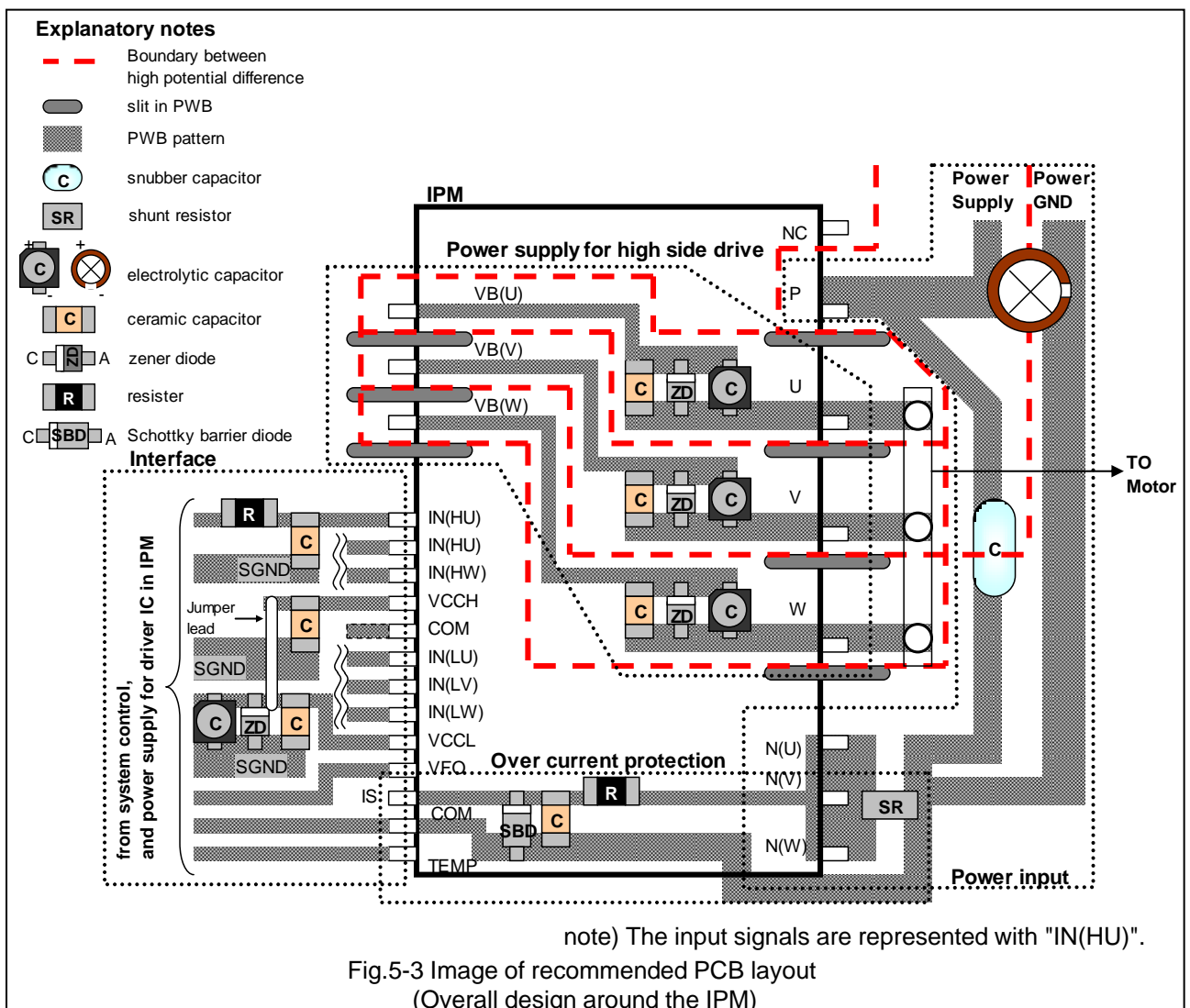
In these figures, the input signals from system control are represented with "IN(HU)".

The recommendations and precautions are as follows,

(1) Overall design around the IPM

- (A) Keep a relevant creepage distance at the boundary.
(Place a slit between there if needed.)
- (B) The pattern of the power input (DC bus voltage) part and the power supply for high side drive parts should be separated in order to prevent the increase of conduction noise.
In case of crossing these wirings on pattern in multi-layer PCB, please take note of stray capacitance between wires and insulation performance of the PCB.
- (C) The pattern of the power supply for high side drive part and the input circuit of each phase part should be separated to avoid malfunction of the system. In case of using multi-layer PCB, it is strongly recommended not to cross these wirings.

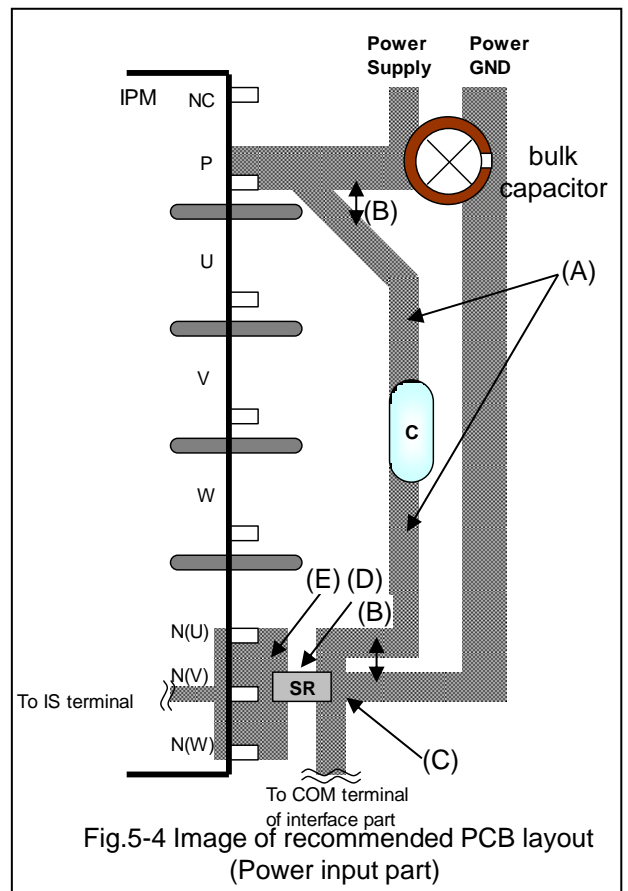
Details of each part are described in next page.



2. Recommendation and Precautions in PCB design

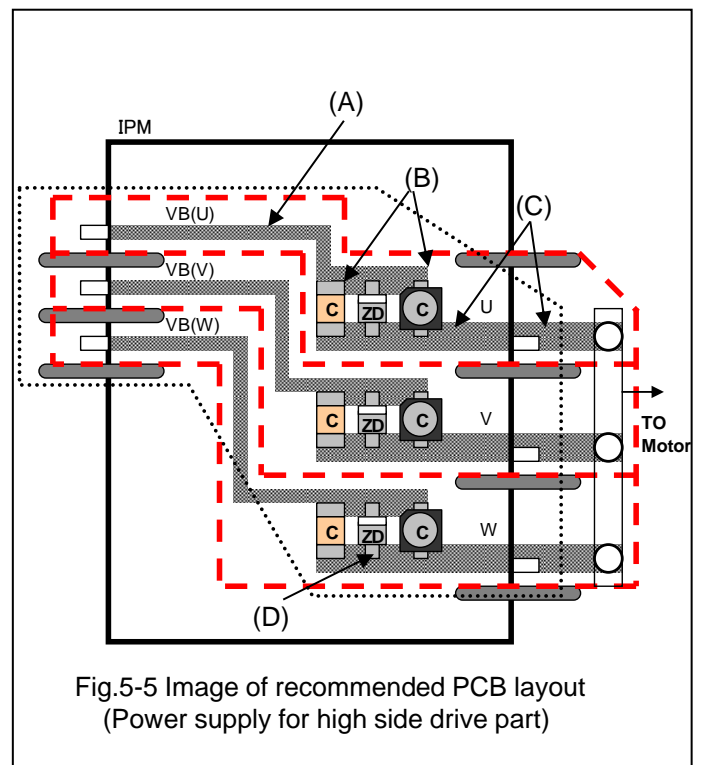
(2) Power input part

- (A) Connect the snubber capacitor between P terminal and the negative node of the shunt resistor as close as possible.
The pattern between the snubber capacitor and P terminal, and shunt resistor should be as short as possible to avoid the influence of pattern inductance.
- (B) Pattern of the bulk capacitor and snubber capacitor should be separated near the P terminal and shunt resistor.
- (C) The pattern from power GND and COM terminal should be connected as close as possible to the shunt resistor with single-point-grounding.
- (D) Please use low inductance shunt resistor.
- (E) The pattern between N(U),N(V),N(W) terminals and the shunt resistor should be as short as possible.



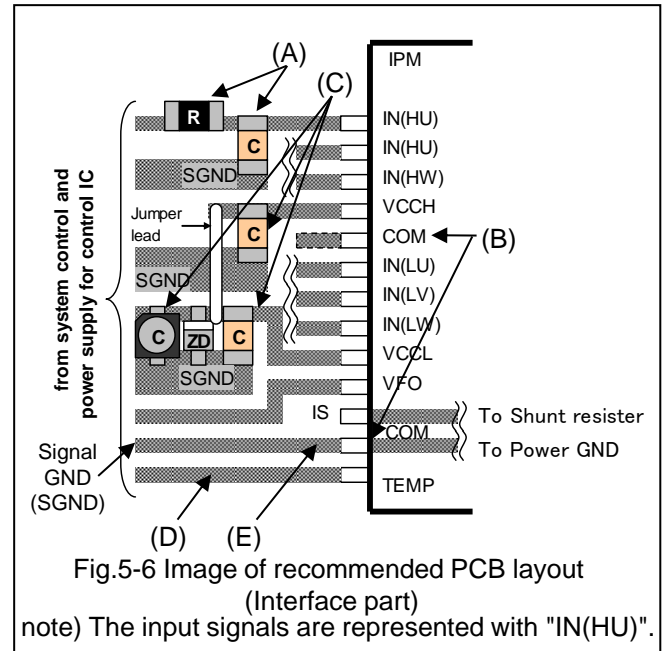
(3) Power supply for high side drive part.

- (A) The pattern between VB(U), VB(V), VB(W) and the electronic components (ceramic capacitor, electrolytic capacitor and Zener diode) should be as short as possible to avoid the influence of pattern inductance.
- (B) Please use appropriate capacitor according to applications. Especially, please use ceramic capacitor or low-ESR capacitor close to VB(U), VB(V), VB(W) terminals.
- (C) The pattern to Motor output and negative pole of the capacitor connected to VB(U), VB(V), VB(W) should be separated close to U, V and W terminals in order to avoid malfunction due to common impedance.
- (D) If the stray capacitance between VB(U) and power GND (or equal potential) is large, the voltage between VB(U) and U terminals might become overvoltage or negative voltage when IGBT turns on and off with high dV/dt. Therefore, connecting a Zener diode between VB(U) and U are recommended. It should be connected close to VB(U) terminal.
(The same applies to VB(V) and VB(W).)



(4) Interface part

- (A) Please connect a capacitor between the input signal and COM terminal if the influence of noise from the power supply for high side drive part (and so forth) are not negligible. The negative pole of the capacitor should be connected as close as possible to the pattern of signal GND near the COM terminal.
If filter resistor or capacitor is used, please take into account the internal pull down resistors in this IPM and confirm the signal level in the actual system.
- (B) This IPM has two COM terminals that are connected internally. Please use either one.
- (C) Electrolytic capacitor and ceramic capacitor should be connected between V_{CCL} and COM, V_{CCH} and COM. These capacitors should be connected as close to each terminal as possible.
- (D) The output signal from TEMP terminal should be parallel with Signal GND in order to minimize the effects of noise.
- (E) The pattern of Signal GND from system control and the pattern from COM terminal should be connected at single point ground. The single point ground should be as close to the COM terminal as possible.



(5) Over Current Protection part

As shown in Fig.5-1 and Fig. 5-2, there are 2 methods to sense over current. One is "One-shunt type" (Fig.5-7 (a)) and the other is "3-shunt type" (Fig.5-7 (b)).

In Fig.5-7 (a)

- (A) The pattern between the negative pole of the shunt resistor and the COM terminal is very important. It is not only the reference zero level of the control IC, but also the current path of bootstrap capacitor charging current and gate driving current of low side IGBTs. Therefore, in order to minimize the impact of common impedance, this pattern should be as short as possible.
- (B) The pattern of IS signal should be as short as possible to avoid OC level fluctuation and malfunction.
- (C) In order to prevent false detection during switching operation, it is recommended to connect a RC filter to the IS terminal. The negative pole of this capacitor should be connected to the pattern of signal GND near the COM terminal.
- (D) If negative voltage is applied to IS terminal during switching operation, please connect a Schottky barrier diode between the IS and COM terminals or in parallel with the shunt resistor.

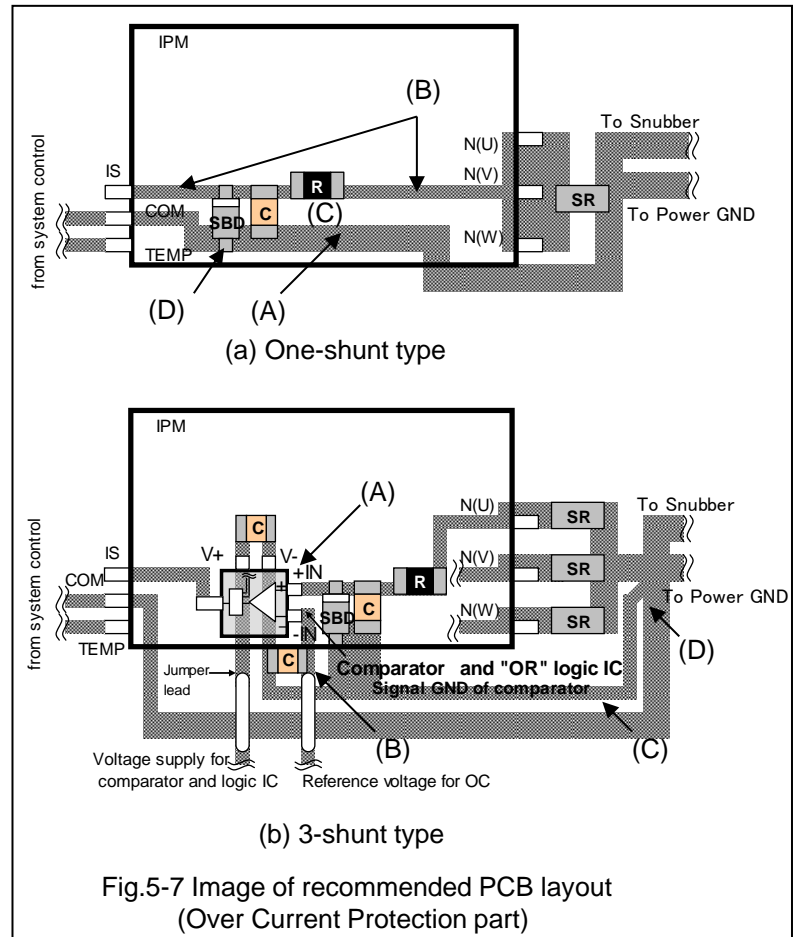


Fig.5-7 Image of recommended PCB layout
(Over Current Protection part)

In Fig.5-7 (b)

- (A) Please use high speed type comparator and logic IC to detect OC condition quickly.
- (B) The reference voltage level of OC which is inputted to the comparator should be coupled by a capacitor to signal GND. The capacitor should be as close to the comparator as possible.
- (C) The pattern of signal GND for COM terminal and the pattern of signal GND for the comparator should be separated.
- (D) The pattern of signal GND from COM and the pattern of signal GND of the comparator should be connected at single point ground. The single point ground should be as close to the shunt resistors as possible.
- (E) The other precautions and recommendations are same as Fig.5-7 (a).

Please refer to Chapter 4, Section 2 for more information on the circuit constant determination.