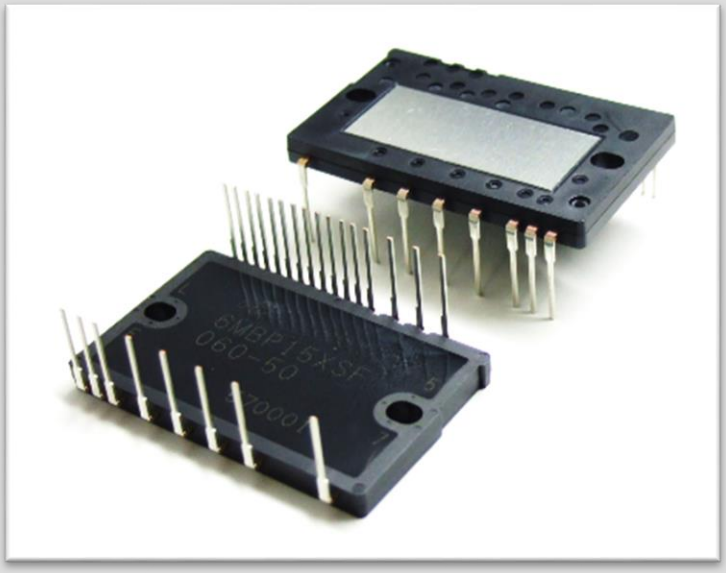
Fuji Electric
Innovating Energy Technology



Fuji Small IPM (Intelligent Power Module)
P633A Series
6MBP**XS*060-50
Chapter 3 Detail of Signal Input/Output Terminals

Application Manual

October 2021

Fuji Electric Co., Ltd.

MT6M08855 a

Cautions

This Instruction contains the product specifications, characteristics, data, materials, and structures as of June 2021. The contents are subject to change without notice for specification changes or other reason. When using a product listed in this Instruction be sure to obtain the latest specifications.

The application examples in this note show the typical examples of using Fuji products and this note shall neither assure to enforce the industrial property including some other rights nor grant the license.

Although Fuji Electric Co., Ltd. continually strives to enhance product quality and reliability, a small percentage of semiconductor products may become faulty. When using Fuji Electric semiconductor products in your equipment, be sure to take adequate safety measures such as redundant, flame-retardant and fail-safe design in order to prevent a semiconductor product failure from leading to a physical injury, property damage or other problems.

The products described in this application manual are manufactured with the intention of being used in the following industrial electronic and electrical devices that require normal reliability.

- Compressor motor inverter
- Fan motor inverter for room air conditioner
- Compressor motor inverter for heat pump applications, etc.

If you need to use a semiconductor product in this application note for equipment requiring higher reliability than normal, such as listed below, be sure to contact Fuji Electric Co., Ltd. to obtain prior approval. When using these products, take adequate safety measures such as a backup system to prevent the equipment from malfunctioning when a Fuji Electric's product incorporated in the equipment becomes faulty.

- Transportation equipment (mounted on vehicles and ships)
- Trunk communications equipment
- Traffic-signal control equipment
- Gas leakage detectors with an auto-shutoff function
- Disaster prevention / security equipment
- Safety devices, etc.

Do not use a product in this application note for equipment requiring extremely high reliability such as:

- Space equipment
- Airborne equipment
- Atomic control equipment
- Submarine repeater equipment
- Medical equipment

If you have any question about any portion of this application note, ask Fuji Electric Co., Ltd. or its sales agencies. Neither Fuji Electric Co., Ltd. nor its agencies shall be liable for any injury or damage caused by any use of the products not in accordance with instructions set forth herein.

Chapter 3 Detail of Signal Input/Output Terminals

1. Control Power Supply Terminals VCCH, VCCL, COM

<Voltage Range of control power supply terminals VCCH, VCCL>

- For control supply voltage, please connect a 15V±10% DC power supply between VCCH, VCCL and COM terminals. Table 3-1 describes the operation of the product for various control supply voltages.
- A low impedance capacitor and a high frequency decoupling capacitor should be connected close to the terminals of the power supply.
- High frequency noise on the power supply might cause malfunction of the internal control IC or erroneous fault signal output. To avoid these problems, the maximum amplitude of voltage ripple on the power supply should be less than ±1V/μs.
- The potential at the COM terminal is different from that at the N(U, V, W) power terminal. It is very important that all control circuits and power supplies are referred to the COM terminal and not to the N(U, V, W) terminals. If circuits are improperly connected, current might flow through the shunt resistor and cause improper operation of the short-circuit protection function. In general, it is recommended to make the COM terminal as the ground potential in the PCB layout.
- The main control power supply is also connected to the bootstrap circuit which provide a power to floating supplies for the high side gate drivers.
- When high side control supply voltage V_{CCH} falls below $V_{CCH(OFF)}$, only the IGBT which occurred the under voltage condition becomes off-state even though input signal is ON condition.
- When low side control supply voltage V_{CCL} falls below $V_{CCL(OFF)}$, all lower side IGBTs become off-state even though the input signal is ON condition.

Table 3-1 Functions versus supply voltage V_{CCH}, V_{CCL}

Control Voltage Range [V]	Operations and functions
0 ~ 4	The product doesn't operate. UV and fault output are not activated. *d*V/*d*t noise on the main P-N supply might cause malfunction of the IGBTs.
4 ~ 13	The product starts to operate. UV is activated, control input signals are blocked and fault output VFO is generated.
13 ~ 13.5	UV is reset. IGBTs perform switching in accordance to input signal. Drive voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition. High side IGBTs do not switch until V_B(*)*1 reaches $V_{B(ON)}$ after initial charging.
13.5 ~ 16.5	Normal operation. This is the recommended operating condition.
16.5 ~ 20	IGBTs perform switching. Because drive voltage is above the recommended range, IGBT's switching is faster and causes an increase in system noise. Even with proper overcurrent protection design, the short-circuit peak current can become very large and might lead to failure.
Over 20	Control circuit in the product might be damaged. It is recommended to insert a Zener diode between each pair of control supply terminals if necessary.

*1 : V_B(*) is applied between VB(U)-U, VB(V)-V, VB(W)-W.

<Under Voltage (UV) protection of control power supply terminals VCCH, VCCL>

- Fig.3-1 shows the UV protection circuit of VCCH and VCCL. Fig.3-2 and Fig.3-3 shows the operation sequence of UV operation of V_{CCH} and V_{CCL}.
- As shown in Fig.3-1, a diode is electrically connected between VCCH-COM and VCCL-COM terminals. The diode is connected to protect the Small IPM from the input surge voltage. Do not use the diode for voltage clamp purpose otherwise the product might be damaged.

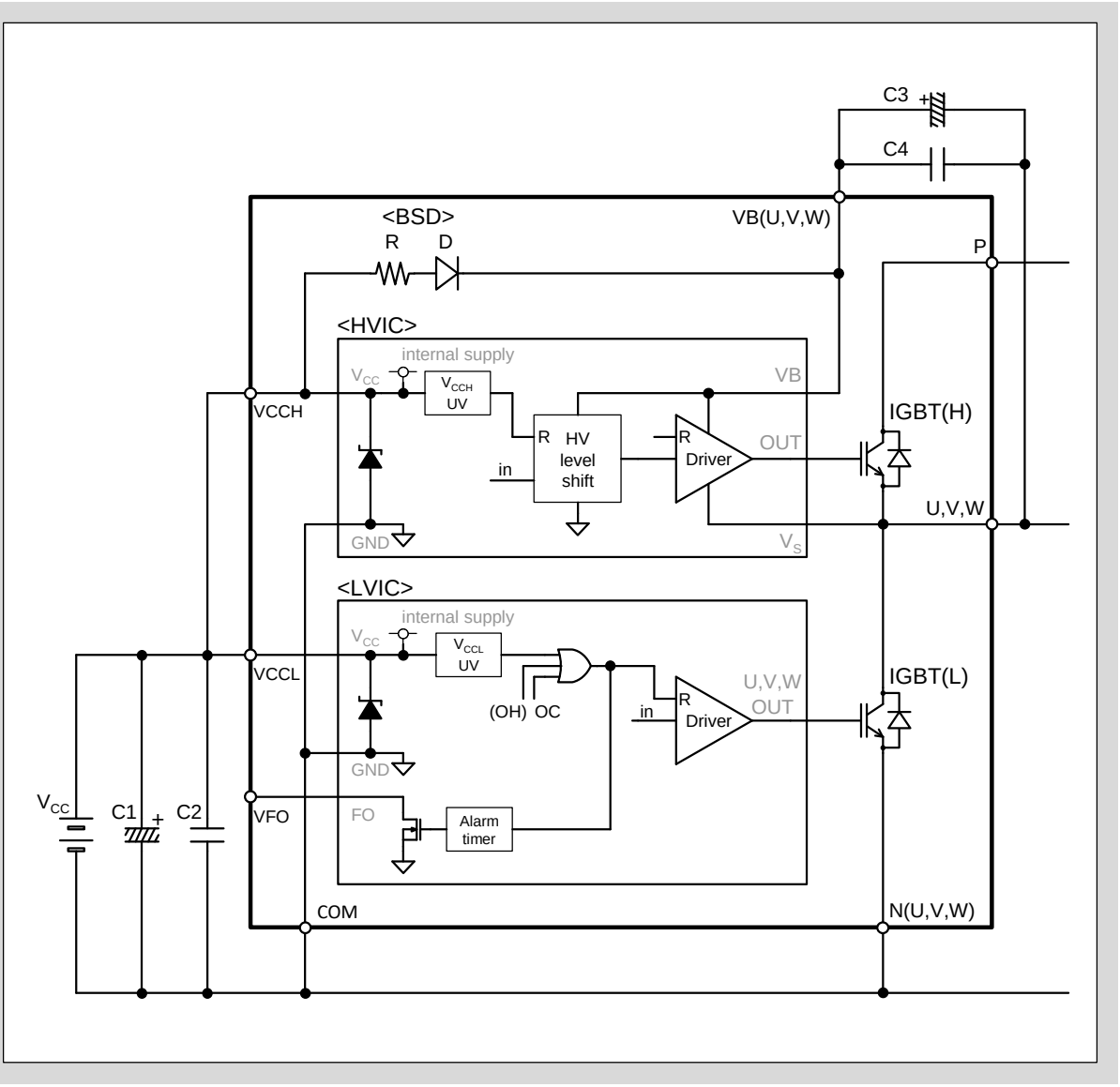


Fig.3-1 UV protection circuit of VCCH, VCCL

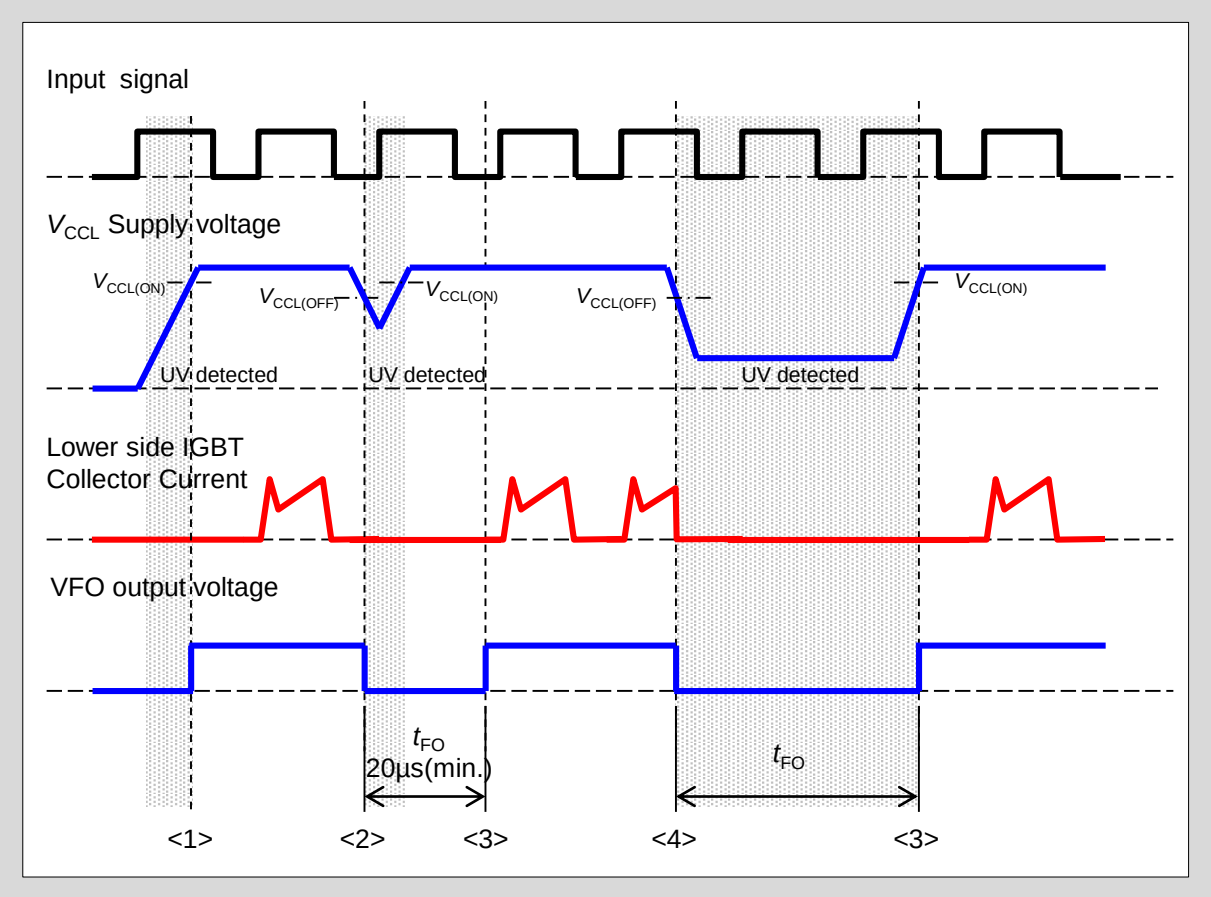


Fig.3-2 Operation sequence of V_{CCL} Under Voltage protection (lower side arm)

<1> When V_{CCL} is lower than $V_{CCL(ON)}$, all lower side IGBTs are OFF state.
After V_{CCL} exceeding $V_{CCL(ON)}$, the fault output VFO is released (high level).
And the LVIC starts to operate, then next input is activated.

<2> The fault output VFO is activated when V_{CCL} falls below $V_{CCL(OFF)}$, and all lower side IGBT remains OFF state.
If the voltage drop time is less than 20µs, the minimum pulse width of the fault output signal is 20µs and all lower side IGBTs are OFF state regardless of the input signal condition.

<3> UV is reset after t_{FO} and V_{CCL} exceeding $V_{CCL(ON)}$, then the fault output VFO is reset simultaneously.
After that the LVIC starts to operate from the next input signal.

<4> When the voltage drop time is more than t_{FO}, the fault output pulse width is generated and all lower side IGBTs are OFF state regardless of the input signal condition during the same time.

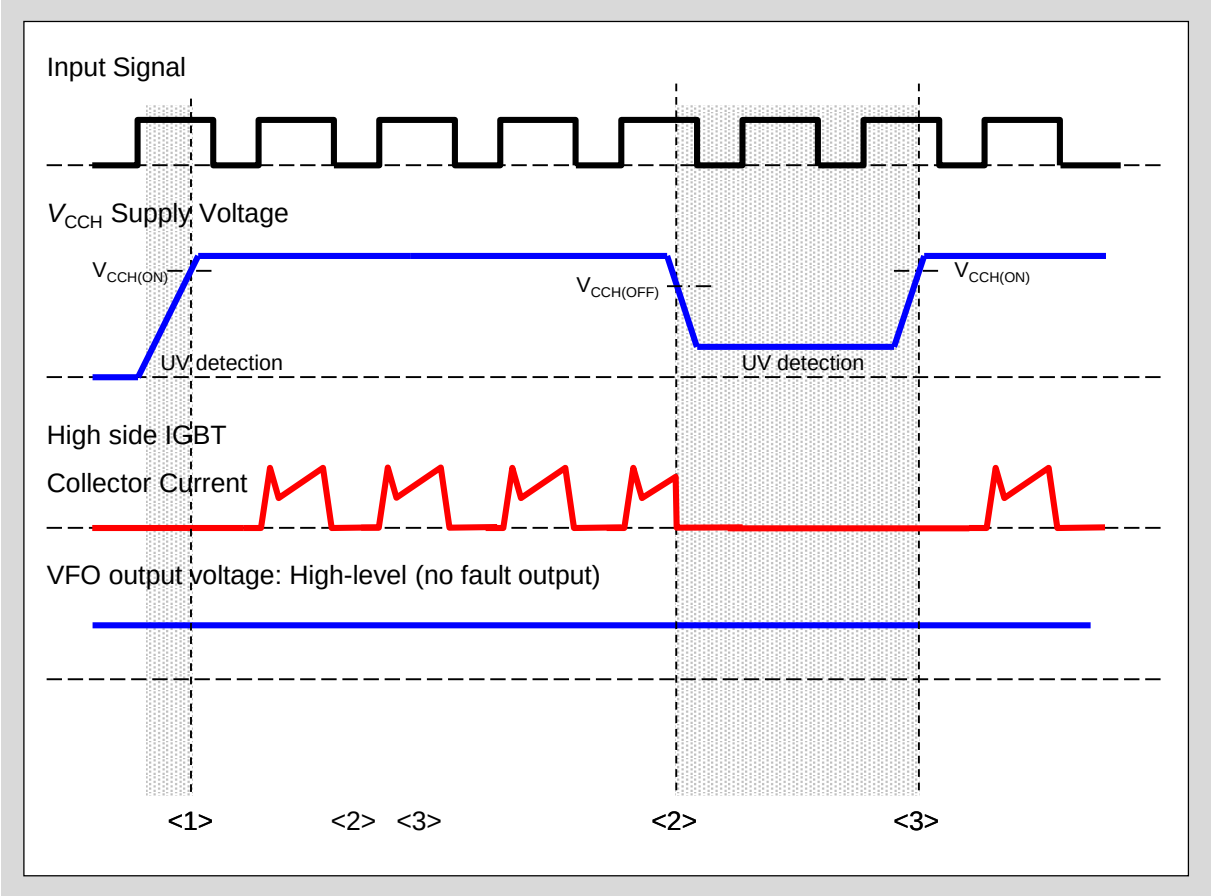


Fig.3-3 Operation sequence of V_{CCH} Under Voltage protection (high side)

<1> When V_{CCH} is lower than $V_{CCH(ON)}$, the upper side IGBT is OFF state.
After V_{CCH} exceeds $V_{CCH(ON)}$, the HVIC starts to operate from the next input signals.
The fault output VFO is constant (high level) regardless of V_{CCH}.
<2> After V_{CCH} falls below $V_{CCH(OFF)}$, the upper side IGBT remains OFF state.
But the fault output VFO keeps high level.
<3> The HVIC starts to operate from the next input signal after UV is reset.

2. Power Supply Terminals of High Side VB(U, V, W)

<Voltage range of high side bias voltage for IGBT driving terminals VB(U, V, W)>

- The V_B(*) voltage, which is the voltage difference between VB(U,V,W) and U,V,W, provides the power supply to the HVICs within the product.
- This power supply must be in the range of 13.0~18.5V to ensure that the HVICs can fully drive the high side IGBTs. The product includes UV protection for V_B(*) to ensure that the HVICs do not drive the high side IGBTs when V_B(*) drops below a specified voltage (refer to the datasheet). This function prevents the IGBT from operating in a high dissipation mode. Please note that the UV protection only works on the triggered phase and doesn't generate fault output.
- Conventionally, three isolated power supplies are necessary for IGBT drive at the high side. In case of using bootstrap circuit, the IGBT drive power supply for high side can be generated from the high side/low side control power supply.
- The power supply of the high side is charged when the low side IGBT is turned on or when freewheel current flows the low side FWD. Table 3-2 describes the operation of the product for various control supply voltages. The control supply should be well filtered with a low impedance capacitor and a high frequency decoupling capacitor connected close to the terminals in order to prevent malfunction of the internal control IC caused by a high frequency noise on the power supply.
- When V_B(*) falls below $V_{B(OFF)}$, only the triggered phase IGBT is off-state even though input signal is ON condition.

Table 3-2 Functions versus high side bias voltage for IGBT driving V_B(*)

Control Voltage Range [V]	Operations and functions
0 ~ 4	HVICs are not activated. UV does not operate. d*V*/d*t* noise on the main P-N supply might trigger the IGBTs.
4 ~ 12.5	HVICs start to operate. As the UV is activated, control input signals are blocked.
12.5 ~ 13	UV is reset. The high side IGBTs perform switching in accordance to input signal. Driving voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition.
13 ~ 18.5	Normal operation. This is the recommended operating condition.
18.5 ~ 20	The high side IGBTs perform switching. Because drive voltage is above the recommended range, IGBT's switching is faster and causes an increase in system noise. Even with proper overcurrent protection design, the short-circuit peak current can become very large and might lead to failure.
Over 20	Control circuit in the product might be damaged. It is recommended to insert a Zener diode between each pair of high side power supply terminals.

<Under Voltage (UV) protection of high side power supply terminals VB(U,V,W)>

- Fig.3-4 shows the UV protection circuit of high side power supply VB(U, V, W).
- Fig.3-5 shows the operation sequence of UV operation of V_B(U), V_B(V), V_B(W).
- As shown in Fig.3-4, diodes are electrically connected to the VB(U,V,W)-(U,V,W) and VB(U,V,W)-COM terminals. These diodes protect the product from input surge voltage. Do not use these diodes for voltage clamp purpose otherwise the product might be damaged.

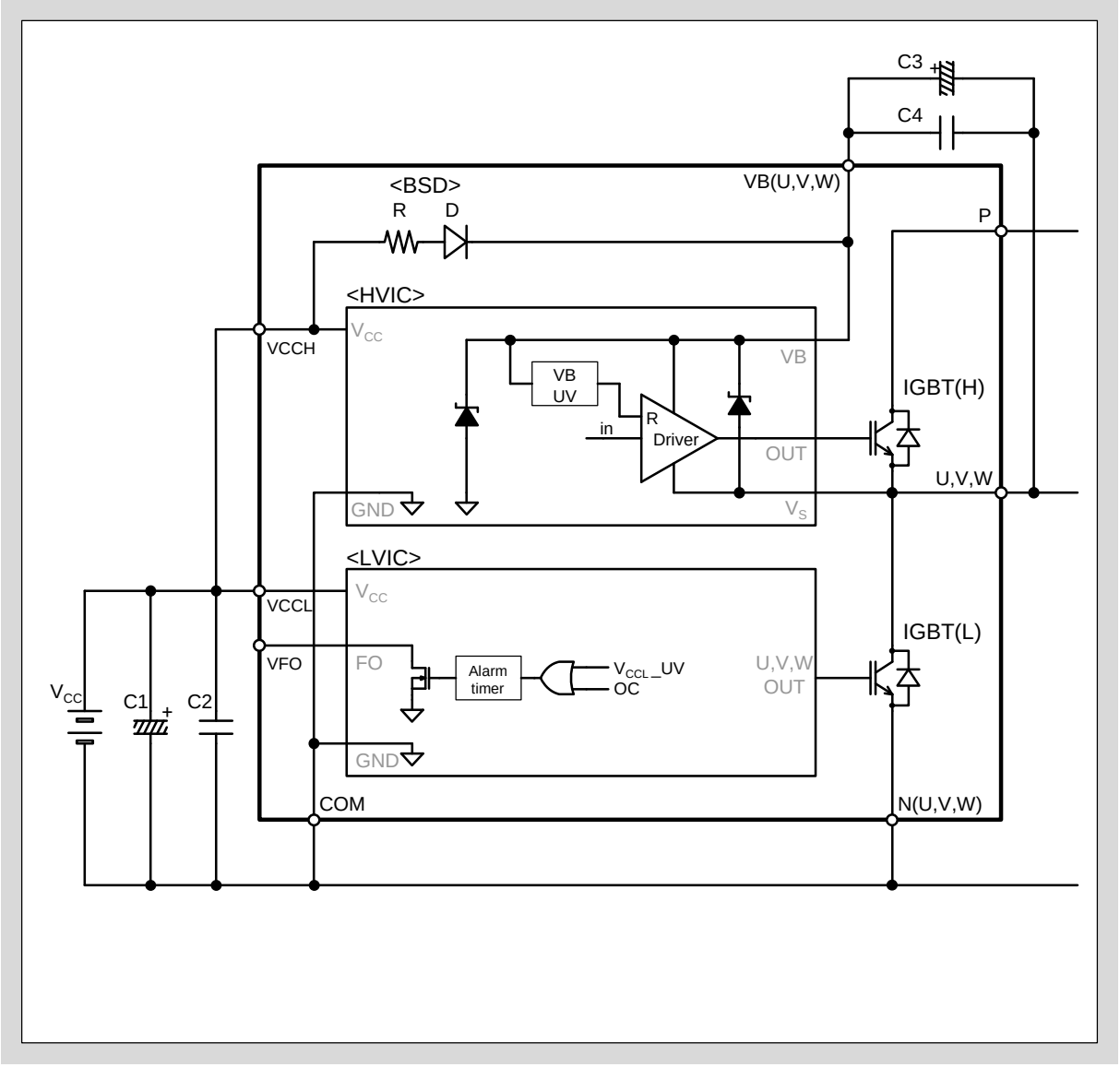


Fig.3-4 UV protection circuit of V_B(U, V, W)

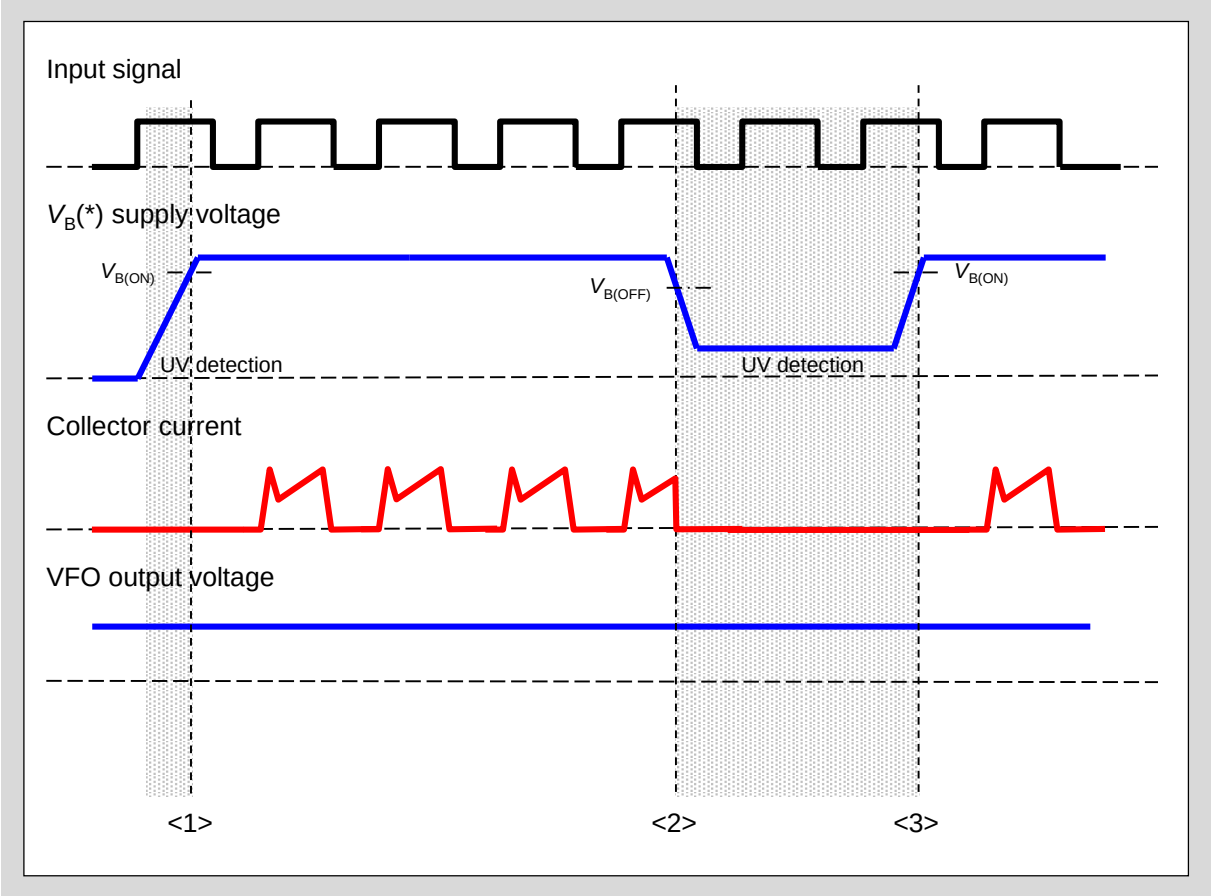


Fig.3-5 Operation sequence of V_B(*) Under voltage protection (high side)

<1> When V_B(*) is lower than $V_{B(ON)}$, the upper side IGBT is OFF state.
After V_B(*) exceeds $V_{B(ON)}$, the HVIC starts to operate from the next input signal.
The fault output VFO is constant (high level) regardless of V_B(*).
<2> After V_B(*) falls below $V_{B(OFF)}$, the high side IGBT remains OFF state.
But the fault output VFO keeps high level.
<3> The HVIC starts to operate from the next input signal after UV is reset.

*1 : V_B(*) is applied between VB(U)-U, VB(V)-V, VB(W)-W.

3. Function of Internal BSDs (bootstrap Diodes)

There are several ways in which the VB(U, V, W)-(U, V, W) floating supply can be generated. Bootstrap method is described here. The boot strap method is a simple and cheap solution. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. As shown in Fig. 3-6, Fig. 3-8 and Fig. 3-11, the boot strap circuit consists of bootstrap diode and resistor which are integrated in the Small IPM and an external capacitor.

<Charging and Discharging of Bootstrap Capacitor During Inverter Operation>

When low side IGBT is ON state, the charging voltage on the bootstrap capacitance $V_{C(t1)}$ is calculated by the following equations. Fig.3-6 shows the circuit diagram of charging operation, and Fig.3-7 shows the timing chart.

$V_{C(t1)} = V_{CC} - V_{F(D)} - V_{CE(sat)} - I_b \cdot R$.....Transient state

$V_{C(t1)} \approx V_{CC}$.....Steady state

$V_{F(D)}$: Forward voltage of Boost strap diode D
$V_{CE(sat)}$: Saturation voltage of low side IGBT
R : Bootstrap resistance
I_b : Bootstrap charging current

When low side IGBT is turned off, the motor current flows through the free-wheel path of the high side FWD. Once V_S rises above V_{CC}, the charging of C stops, and the voltage of C gradually declines due to current consumed by the drive circuit.

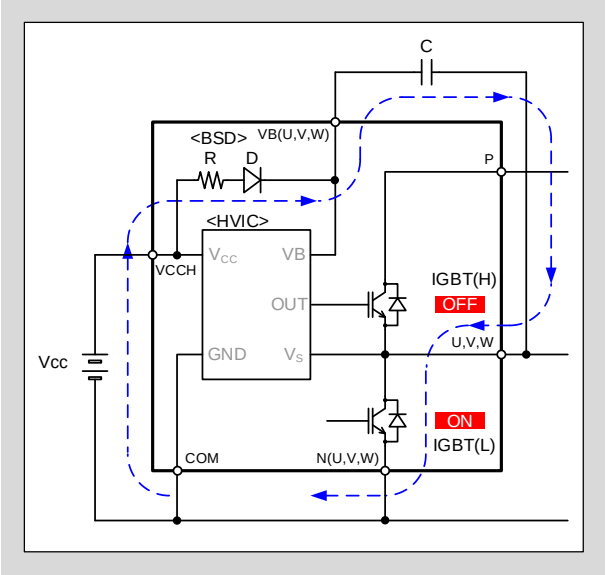


Fig.3-6 Circuit diagram of charging operation

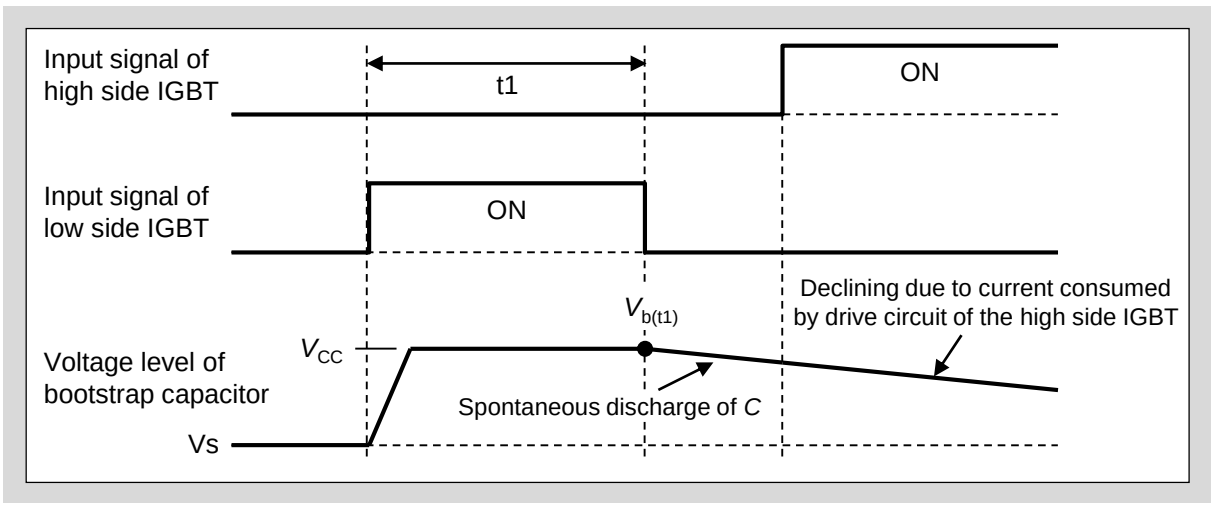


Fig.3-7 Timing chart of charging operation

When the low side IGBT is OFF and the low side FWD is ON, freewheeling current flows through the low side FWD. The voltage on the bootstrap capacitance $V_{C(t2)}$ is calculated by the following equations. Fig.3-8 shows the circuit diagram of charging operation, and Fig.3-9 shows the timing chart.

$V_{C(t2)} = V_{CC} - V_F + V_{F(FWD)} - I_b \cdot R$.....Transient state
$V_{C(t2)} \approx V_{CC}$.....Steady state

$V_{F(D)}$: Forward voltage of Boost strap diode D
$V_{F(FWD)}$: Forward voltage of lower side FWD
R : Bootstrap resistance
I_b : Bootstrap charging current

When both the low side and high side IGBTs are OFF, a regenerative current flows continuously through the low side FWD. Therefore V_s drops to $-V_F$ of FWD, then the bootstrap capacitor is re-charged to restore the declined potential. When the high side IGBT is turned ON and V_s exceeds V_{CC}, the charging of the C stops, and the voltage of the C gradually declines due to current consumed by the drive circuit.

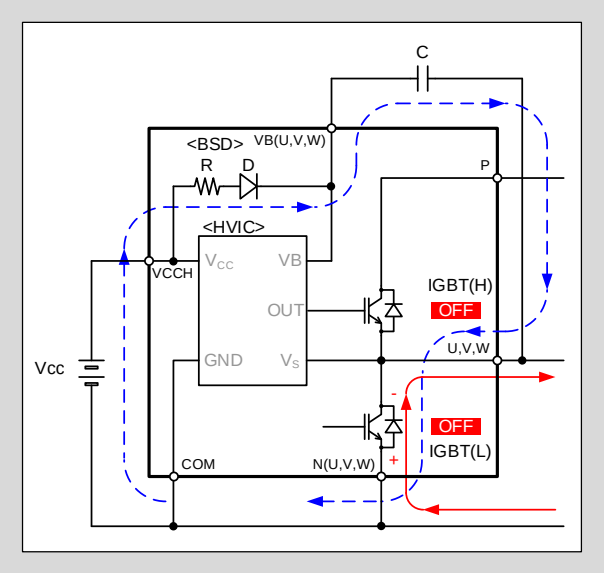


Fig.3-8 Circuit diagram of charging operation when the low side FWD is ON

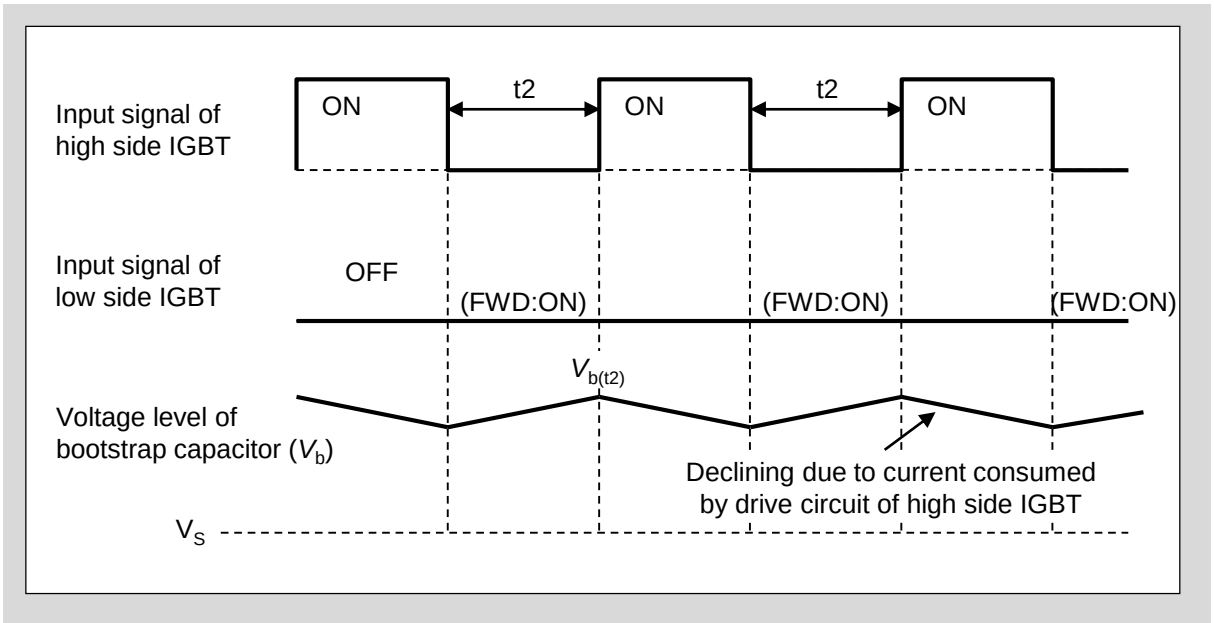


Fig.3-9 Timing chart of charging operation when the low side FWD is ON

<Setting the bootstrap capacitance and minimum ON/OFF pulse width>

The parameter of bootstrap capacitor can be calculated by the following equation:

$$C = I_b \cdot \frac{t_1}{dV_b}$$

t_1: the maximum ON pulse width of the high side IGBT

I_b: the drive current of the HVIC (depends on temperature and frequency characteristics)

dV_b: the allowable discharge voltage. (see Fig.3-10)

- A certain margin should be added to the calculated capacitance.
- The bootstrap capacitance is generally selected 2~3 times the value of the calculated result.
- The recommended minimum ON pulse width (t_2) of the low side IGBT should be basically determined such that the time constant $C \cdot R$ will enable the discharged voltage (dV) to be fully charged again during the ON period.
- However, if the control mode only has the high side IGBT switching (Sequence Fig.3-10), the time constant should be set so that the consumed energy during the ON period can be charged during the OFF period.
- The minimum pulse width is decided by the minimum ON pulse width of the low side IGBT or the minimum OFF pulse width of the high side IGBT, whichever is shorter.

$$t_2 \geq \frac{R \cdot C \cdot dV_b}{V_{CC} - V_{b(min)}}$$

R: Series resistance of Bootstrap diode ΔRF(BSD)

C: Bootstrap capacitance

dV: the allowable discharge voltage.

V_{CC}: Voltage of HVICs and LVIC power supply (ex.15V)

$V_{b(min)}$: the minimum voltage of the high side IGBT drive (Added margin to UV. ex. 14V)

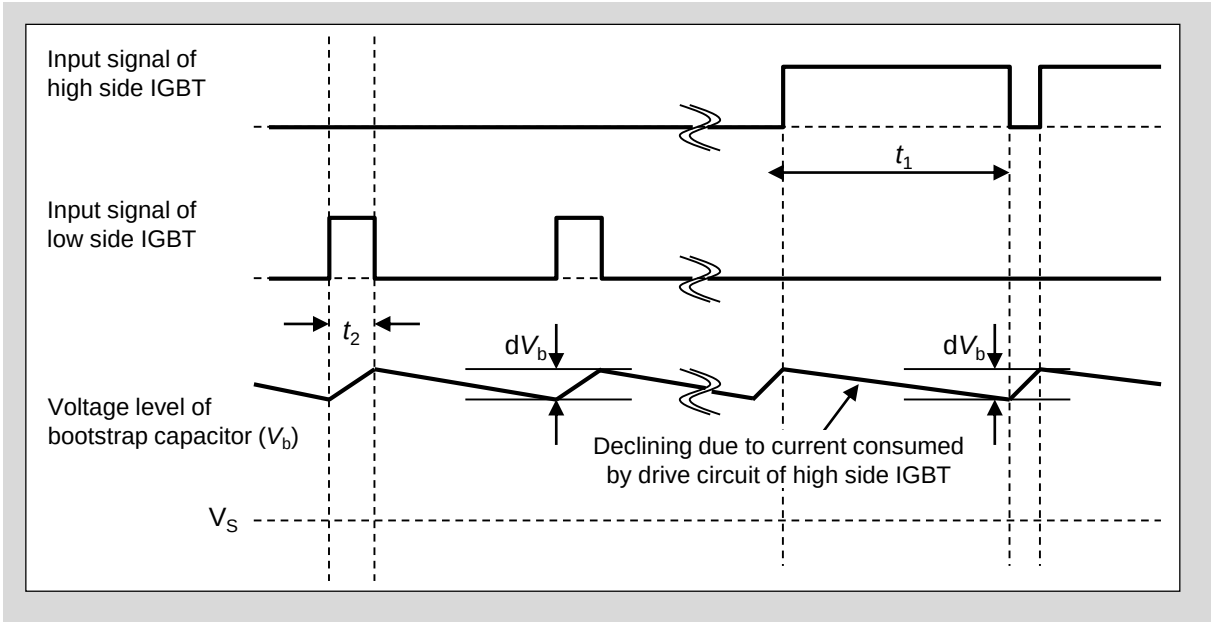


Fig.3-10 Timing chart of charging and discharging operation

<Setting the bootstrap capacitance for Initial charging>

- The initial charge of the bootstrap capacitor is required to start-up the inverter.
- The pulse width or pulse number should be large enough to make a full charge of the bootstrap capacitor.
- For reference, the charging time of 10μF capacitor through the internal bootstrap diode is about 2ms.

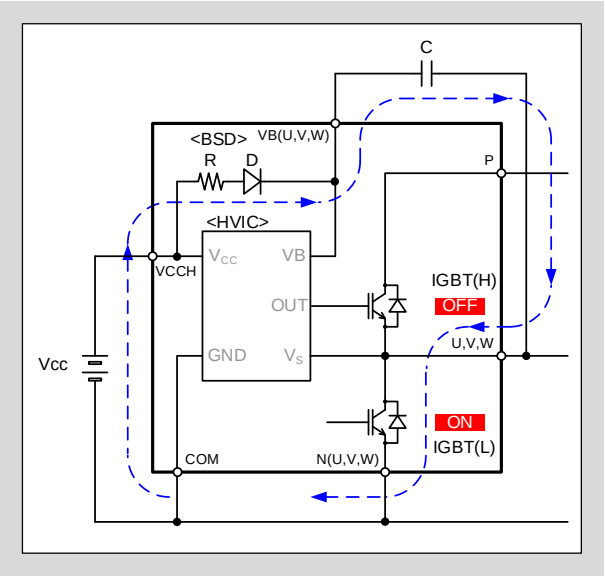


Fig.3-11 Circuit diagram of initial charging operation

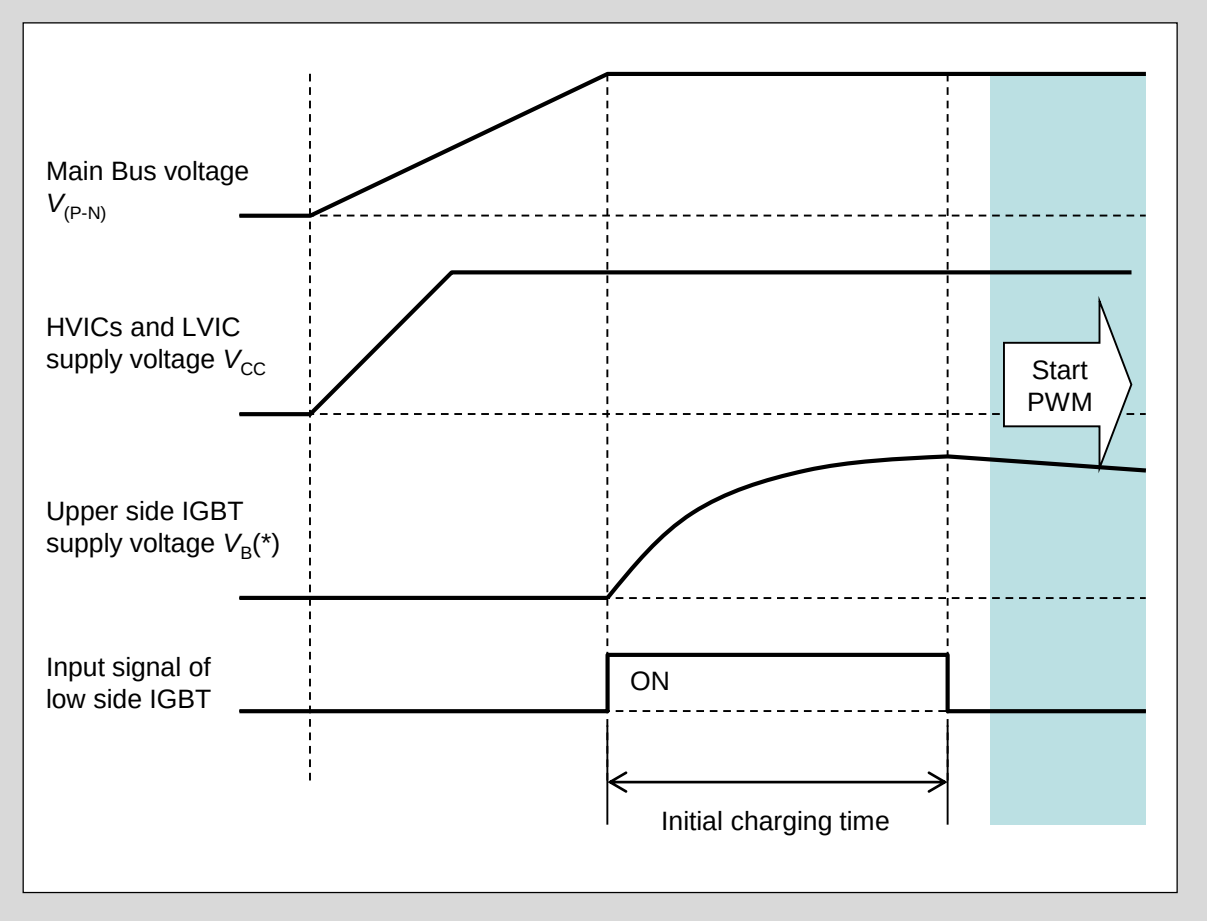


Fig.3-12 Timing chart of initial charging operation

<BSD built-in limiting resistance characteristic>

The BSD has non-linear V_F-I_F characteristic as shown in Fig. 3-13 because the diode forms a built-in current limiting resistor in the silicon. The equivalent dc-resistance against the charging voltage is shown in Fig.3-14.

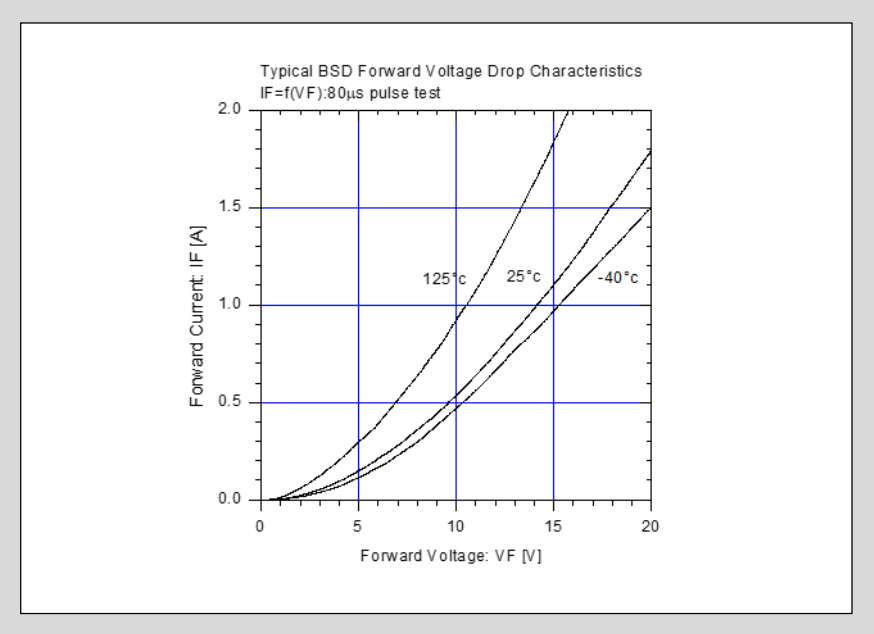


Fig.3-13 V_F-I_F curve of boot strap diode

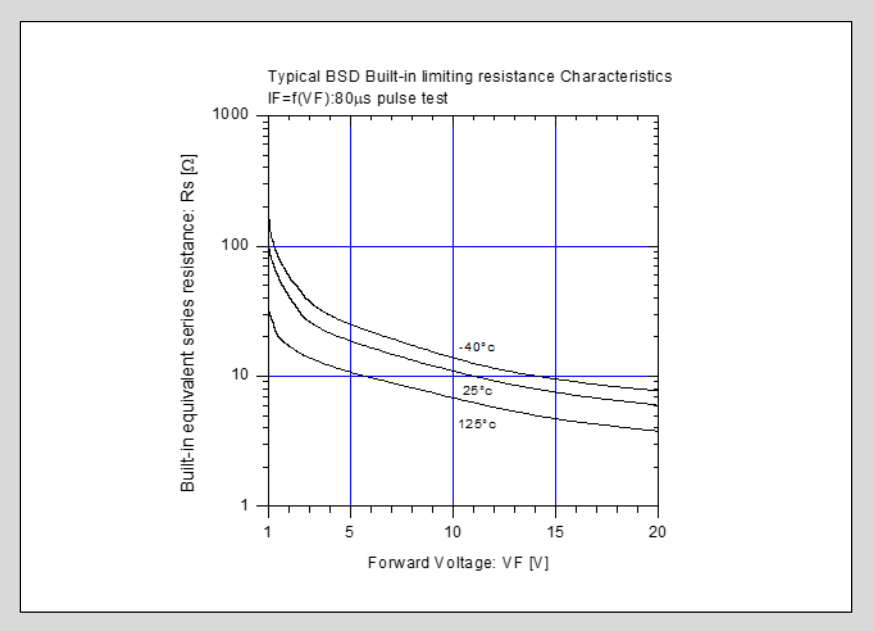


Fig.3-14 Equivalent series resistance of boot strap diode

4. Input Terminals IN(HU,HV,HW), IN(LU,LV,LW)

<Input terminals Connection>

- Fig.3-15 shows the input interface circuit between the MPU and the product. It is possible that the input terminals connect directly to the MPU. It should not need the external pull up and down resistors connected to the input terminals, input logic is active high and the pull down resistors are built in.
- The RC coupling at each input (parts shown dotted in Fig.3-15) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's PCB layout.

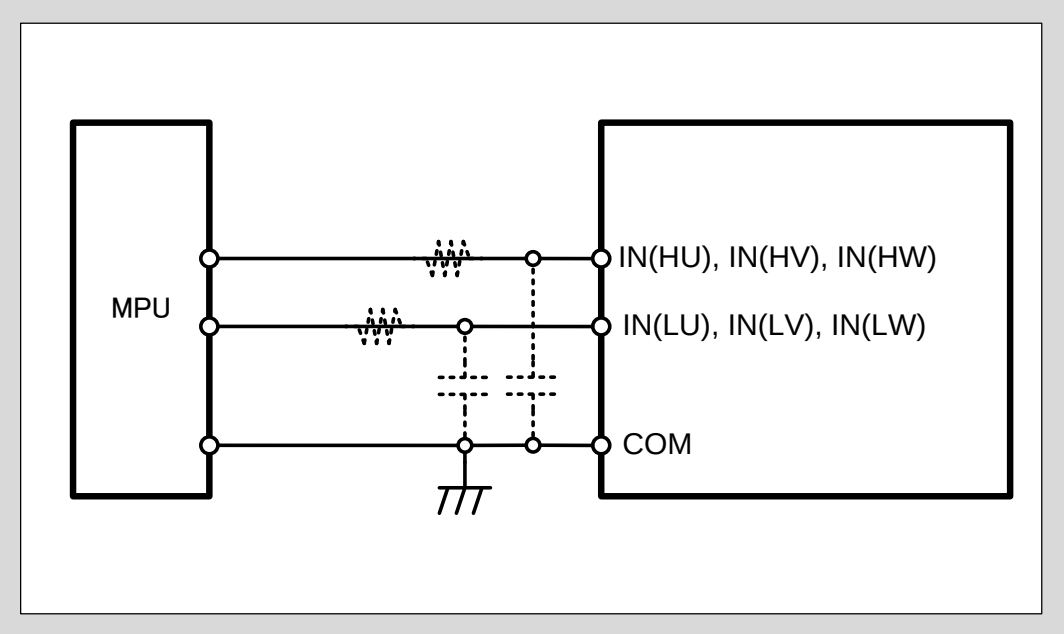


Fig.3-15 Recommended MPU I/O Interface Circuit of IN(HU,HV,HW), IN(LU,LV,LW) terminals

<Input terminal circuit>

- The input logic of this product is active high. This logic has removed the sequence restriction between the control supply and the input signal during startup or shut down operation. Therefore it makes the system failsafe. In addition, the pull down resistors are built in to each input terminals in Fig.3-16. Thus, external pull-down resistors are not needed reducing the required external component. Furthermore, a 3.3V-class MPU can be connected directly since the low input signal threshold voltage.
- As shown in Fig.3-16, the input circuit integrates a pull-down resistor. Therefore, when using an external filtering resistor between the MPU output and input of the product, please consider the signal voltage drop at the input terminals to satisfy the turn-on threshold voltage requirement. For instance, *R*=100Ω and *C*=1000pF for the parts shown dotted in Fig.3-15.
- Fig.3-16 shows that the internal diodes are electrically connected to the VCCL-IN(LU, LV, LW) and IN(HU, HV, HW, LU, LV, LW)-COM terminals. Do not use these diodes for voltage clamp purpose otherwise the product might be damaged.

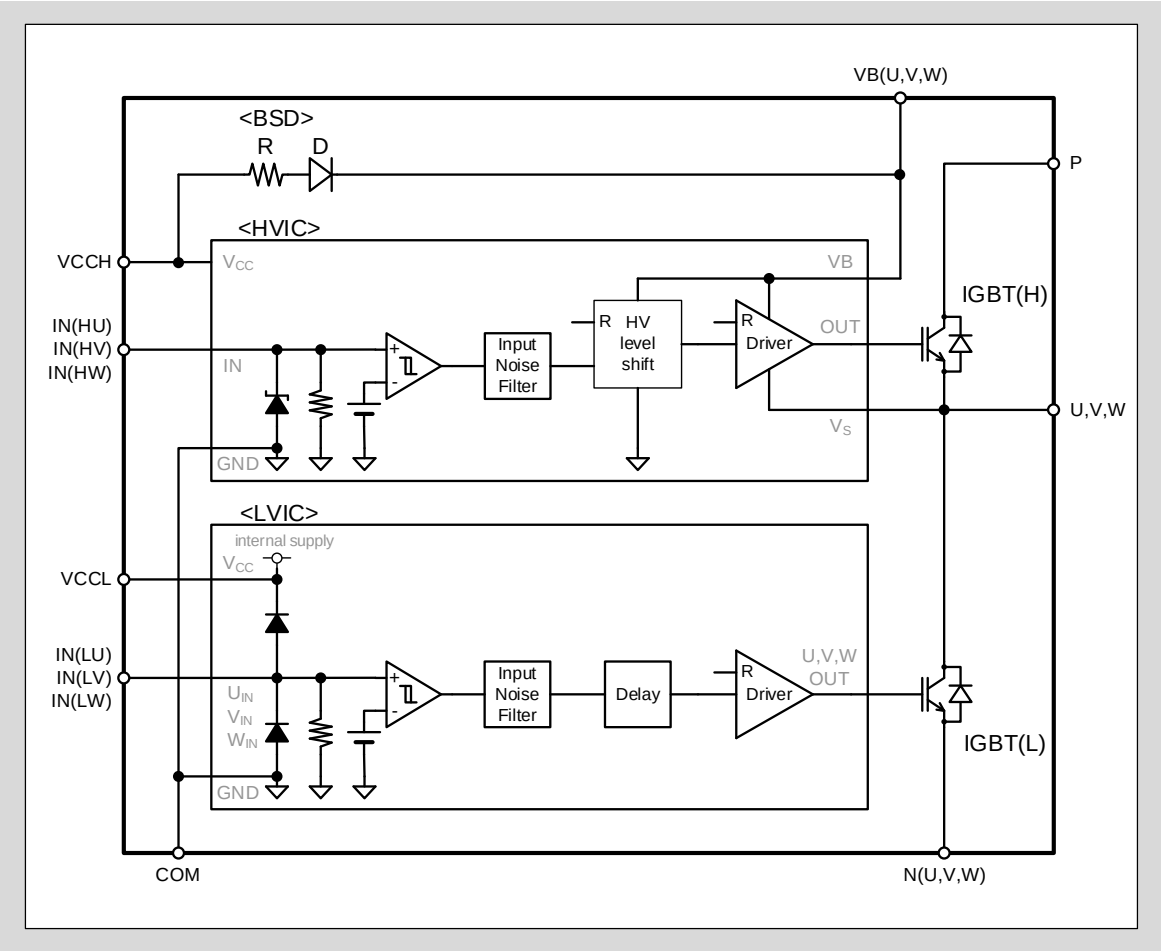


Fig.3-16 Input terminals IN(HU, HV, HW), IN(LU, LV, LW) circuit

<IGBT drive state versus Control signal pulse width>

$t_{IN(ON)}$ is a recommended minimum turn-on pulse width for changing the IGBT state from OFF to ON, and $t_{IN(OFF)}$ is a recommended minimum turn-off pulse width for changing the IGBT state from ON to OFF. Fig.3-17 and Fig.3-18 show IGBT drive state for various control signal pulse width.

A: IGBT may turn on occasionally, even when the ON pulse width of control signal is less than minimum tIN(ON). Also if the ON pulse width of control signal is less than minimum tIN(ON) and voltage below -5V is applied between U-COM,V-COM,W-COM , it may not turn off due to smalfunction of the control circuit.
B: IGBT can turn on and is saturated under normal condition.
C: IGBT may turn off occasionally, even when the OFF pulse width of control signal is less than minimum $t_{IN(OFF)}$. Also if the OFF pulse width of control signal is less than minimum $t_{IN(OFF)}$ and voltage below -5V is applied between U-COM, V-COM, W-COM , it may not turn on due to malfunction of the control circuit.
D: IGBT can turn fully off under normal condition.

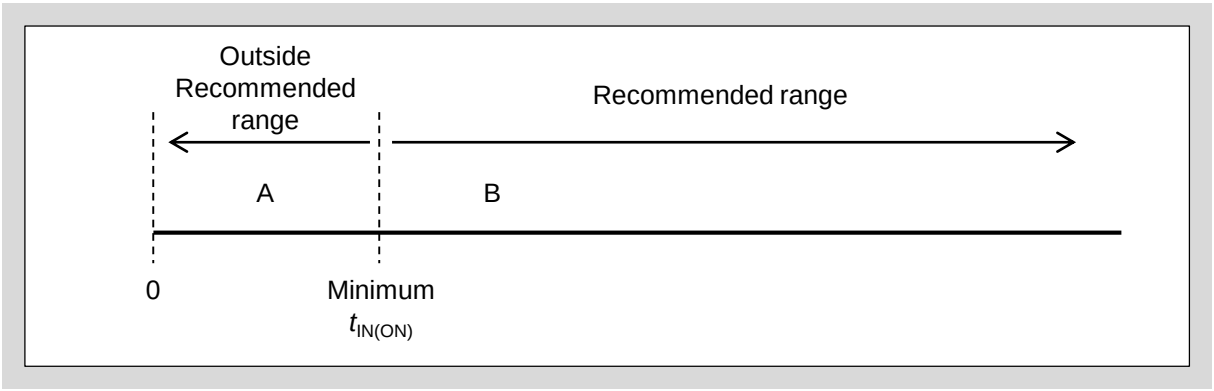


Fig.3-17 IGBT drive state versus ON pulse width of input signal

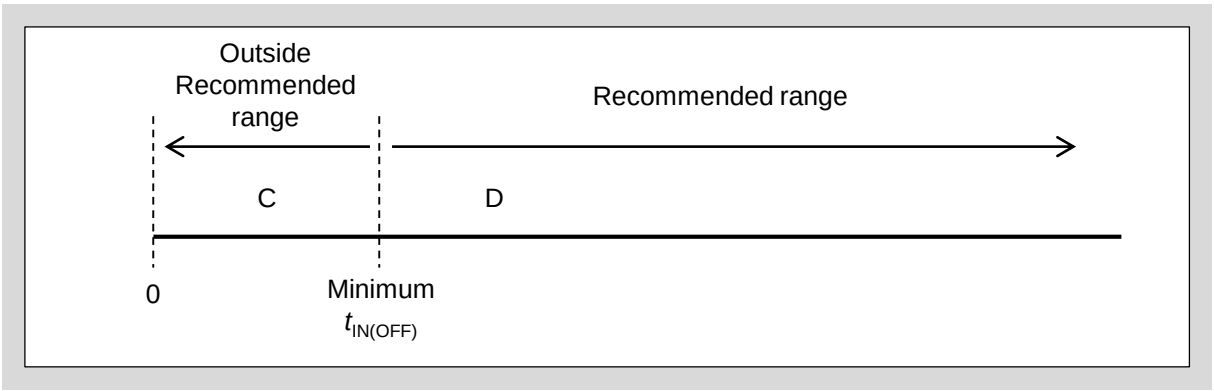


Fig.3-18 IGBT drive state versus OFF pulse width of input signal

5. Over Current Protection Input Terminal IS

- Over current (OC) protection is a function of detecting the IS voltage determined with the external shunt resistor, connected to N(U, V, W) and COM.
- Fig.3-19 shows the over current sensing voltage input IS circuit block, and Fig.3-20 shows the OC operation sequence.
- To prevent the product from unnecessary operations due to normal switching noise or recovery current, it is necessary to apply an external R-C filter (time constant is approximately 0.7µs) to the IS terminal. The shunt resistor should be connected to the product as close as possible.
- Fig.3-19 shows that the diodes in the product are electrically connected to the VCCL-IS and IS-COM terminals. Do not use these diodes for voltage clamp purpose otherwise the product might be damaged.

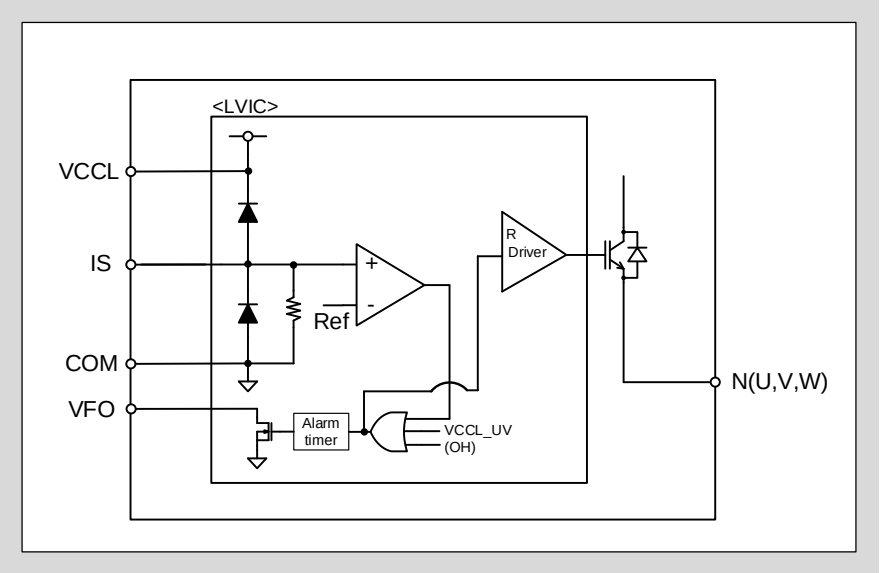


Fig.3-19 Over current sensing voltage input IS circuit

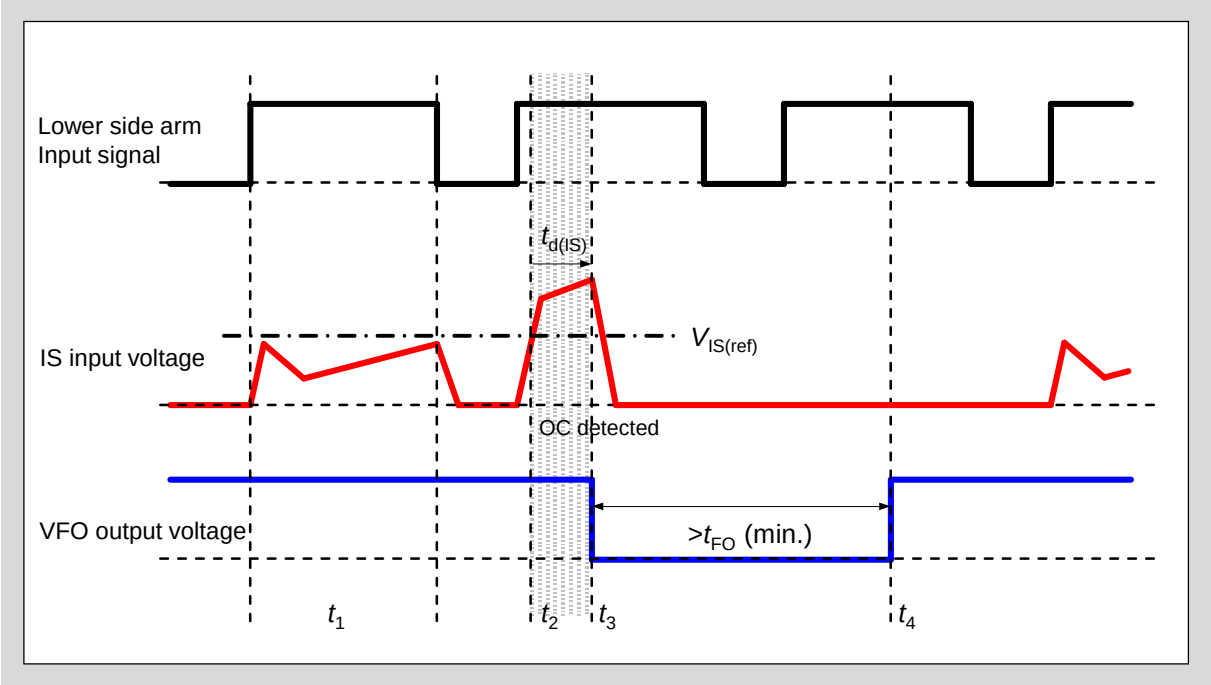


Fig.3-20 Operation sequence of Over Current protection

t1 : IS input voltage does not exceed $V_{IS(ref)}$, while the collector current of the lower side IGBT is under the normal operation.

t2 : When IS input voltage exceeds $V_{IS(ref)}$, the OC is detected.

t3 : The fault output V_{FO} is activated and all lower side IGBT shut down simultaneously after the over current protection delay time $t_{d(IS)}$. Inherently there is dead time of LVIC in $t_{d(IS)}$.

t4 : After the fault output pulse width t_{FO}, the OC is reset. Then next input signal is activated.

6. Fault Status Output Terminal VFO

- As shown in Fig.3-21, it is possible to connect the fault status output VFO terminal directly to the MPU. VFO terminal is open drain configured, thus this terminal should be pulled up by a resistor of approximate 10kΩ to the positive side of the 5V or 3.3V external logic power supply, which is the same as the input signals. It is also recommended that the by-pass capacitor C1 should be connected at the MPU, and the inrush current limitation resistance R1, which is more than 5kΩ, should be connected between the MPU and the VFO terminal. These signal lines should be wired as short as possible.
- Fault status output VFO function is activated by the UV of V_{CCL}, OC and OH.
  (OH protection function is applied to “6MBP**XSF060-50”.)
- Fig.3-21 shows that the diodes in the IPM are electrically connected to the VCCL-VFO and VCCL-COM terminals. Do not use these diodes for voltage clamp purpose otherwise the product might be damaged.
- Fig.3-22 shows the Voltage-current characteristics of VFO terminal at fault state condition. The I_{FO} is the sink current of the VFO terminal as shown in Fig.3-21.

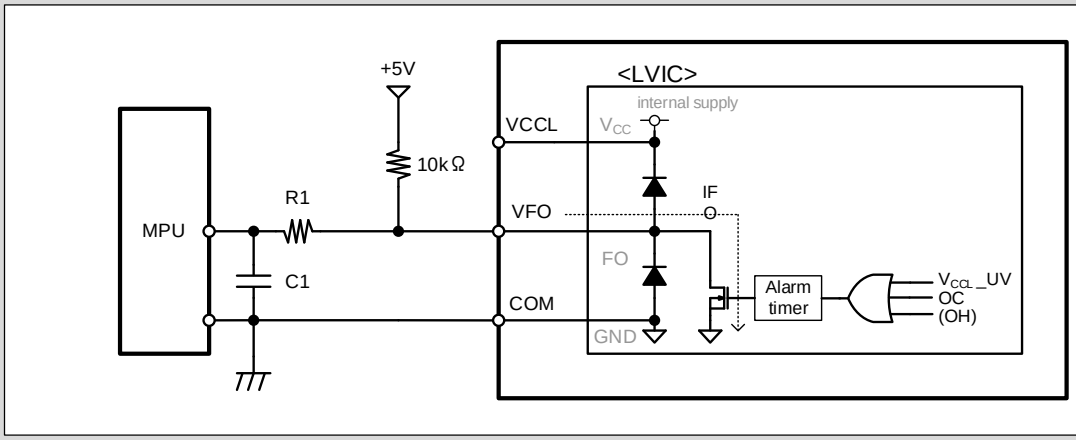


Fig.3-21 Recommended MPU I/O Interface Circuit of VFO terminal

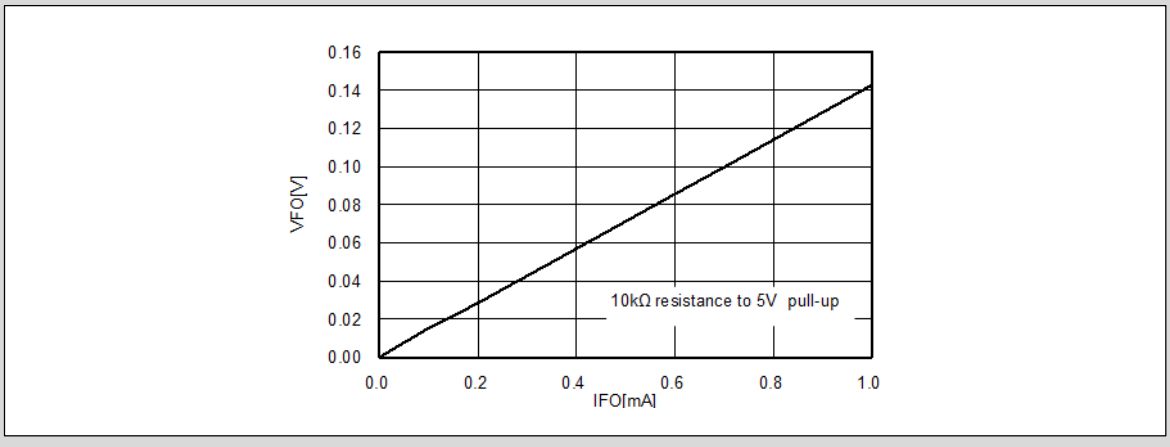


Fig.3-22 Voltage-current Characteristics of VFO terminal at the fault state condition

7. Temperature Sensor Output Terminal TEMP

- As shown in Fig. 3-23, the temperature sensor output TEMP can be connected to MPU directly.
- It is recommended that a by-pass capacitor and >10kΩ of inrush current limiting resistor are connected between the TEMP terminal and the MPU. These signal lines should be wired as short as possible to each device.
- The product has a built-in temperature sensor, and it can output an analog voltage according to the LVIC temperature. This function doesn't protect the product, and there is no fault signal output.
- "6MBP**XSF060-50" has built-in overheating protection. If the temperature exceeds T_{OH}, fault signal will output due to the overheating protection function.
- Since the position of the IGBT chip and the position of the temperature sensor are different, it is not possible to respond to sudden rise in Tvj such as during motor lock and short circuit (see Fig. 2-2).
- A diode is electrically connected between TEMP-COM terminal as shown in Fig. 3-12. The diode protect the product from input surge voltage. Do not use the diode for voltage clamp purpose otherwise the product might be damaged.
- Fig.3-24 shows the LVIC temperature versus TEMP output voltage characteristics. A Zener diode should be connected to the TEMP terminal when the power supply of MPU is 3.3V. Fig. 3-25 shows the LVIC temperature versus TEMP output voltage characteristics with 22kΩ pull-down resistor.
- Fig.3-26 shows the operation sequence of TEMP terminal at during the LVIC startup and shut down conditions.

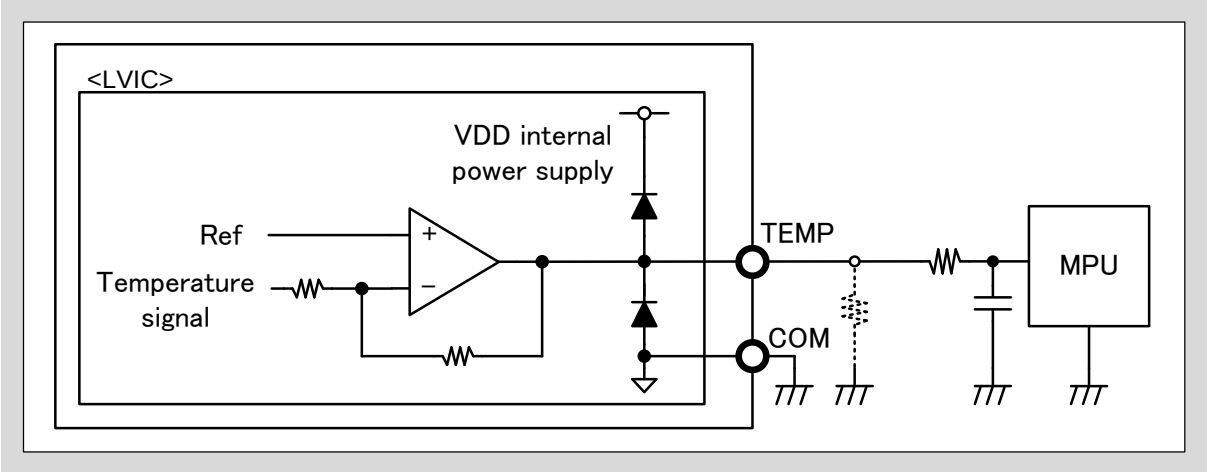


Fig.3-23 Recommended MPU I/O Interface Circuit of TEMP terminal

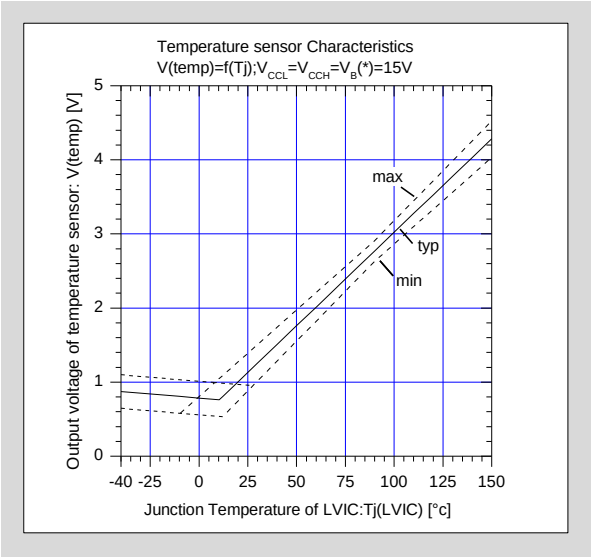


Fig.3-24 LVIC temperature vs. TEMP output voltage characteristics without pull-down resistor

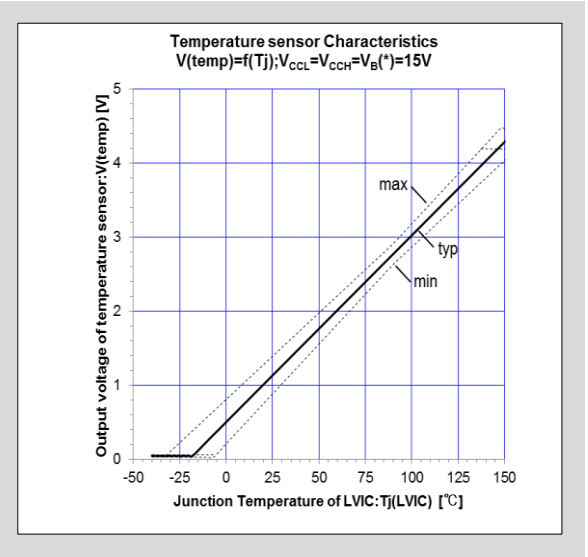


Fig.3-25 LVIC temperature vs. TEMP output voltage characteristics with 22kΩ pull-down resistor

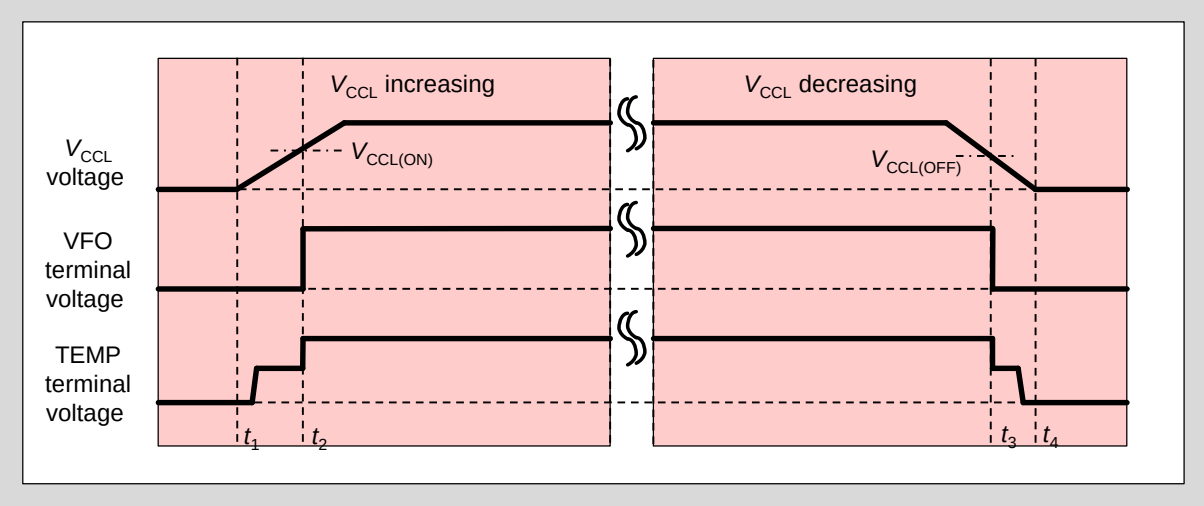


Fig.3-26 Operation sequence of TEMP terminal during LVIC startup and shut down conditions

t_1-t_2 : TEMP function is activated when V_{CCL} exceeds $V_{CCL(ON)}$. If V_{CCL} is lower than $V_{CCL(ON)}$, the TEMP terminal voltage is the same as the clamp voltage.

t_2-t_3 : TEMP terminal voltage rises to the voltage determined by LVIC temperature. In the case that the temperature is under clamping condition, the TEMP terminal voltage is the clamp voltage even though V_{CCL} is above $V_{CCL(ON)}$.

t_3-t_4 : TEMP function is reset when V_{CCL} falls below $V_{CCL(OFF)}$. TEMP terminal voltage is the same as the clamp voltage.

8. Over Heating Protection

- The over heating (OH) protection functions is integrated into "6MBP**XSF060-50".
- The OH function monitors the LVIC junction temperature. Since the position of the IGBT chip and the position of the temperature sensor are different, it is not possible to respond to sudden rise in Tvj such as during motor lock and short circuit (see Fig. 2-2).
- The T_{OH} sensor position is shown in Fig.2-2.
- As shown in Fig.3-27, the product shuts down all low side IGBTs when the LVIC temperature exceeds T_{OH}. The fault status is reset when the LVIC temperature drops below $T_{OH} - T_{OH(hys)}$.

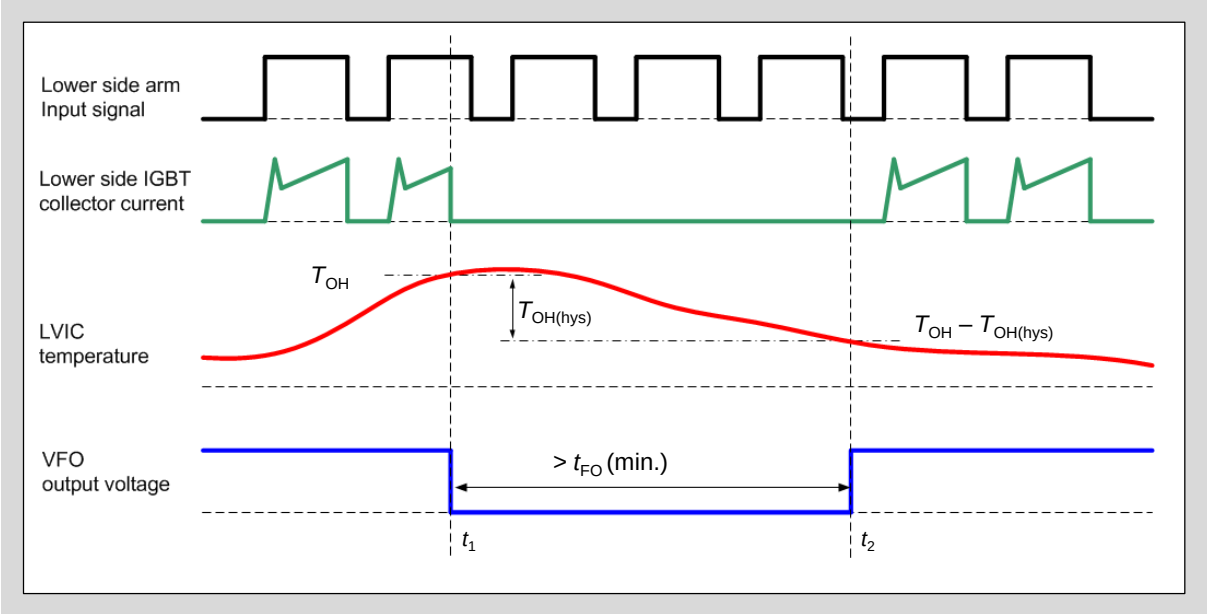


Fig.3-27 Operation sequence of the over heating operation

t_1 : The fault status is activated and all IGBTs of the lower side arm shut down, when LVIC temperature exceeds T_{OH}.

t_2 : When LVIC temperature falls below $T_{OH} - T_{OH(hys)}$, the fault status is reset after t_{FO} and next input signal is activated. $T_{OH(hys)}$ is the over heating protection hysteresis