

# Fuji IGBT Intelligent-Power-Module

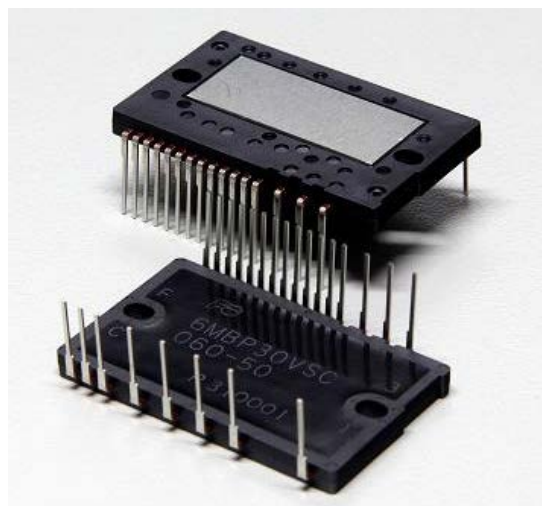
"Compact Type"  
(Preliminary)

## *Application Note*

6MBP15VS\*060-50

6MBP20VS\*060-50

6MBP30VS\*060-50



Fuji Electric Co., Ltd.  
Jun. 2015

# CONTENTS

<b>Chapter 1 Product Outline</b>	
1. Introduction .....	1-2
2. Product line-up .....	1-4
3. Definition of Type Name and Marking Spec.....	1-5
4. Package outline dimensions.....	1-6
5. Absolute Maximum Ratings .....	1-7
<b>Chapter 2 Description of Terminal Symbols and Terminology</b>	
1. Description of Terminal Symbols .....	2-2
2. Description of Terminology .....	2-3
<b>Chapter 3 Detail of Signal Input/Output Terminals</b>	
1. Control Power Supply Terminals $V_{CCH}, V_{CCL}, COM$ .....	3-2
2. Power Supply Terminals of High Side VB(U,V,W) .....	3-6
3. Function of Internal BSDs (Boot Strap Diodes) .....	3-9
4. Input Terminals IN(HU,HV,HW), IN(LU,LV,LW) .....	3-13
5. Over Current Protection Input IS .....	3-16
6. Fault Status Output VFO .....	3-17
7. Linear Temperature Sensor Output TEMP .....	3-18
8. Over Heat Protection .....	3-20
<b>Chapter 4 Power Terminals</b>	
1. Connection of Bus Input terminal and Low Side Emitters .....	4-2
2. Setting of Shunt Resistor of Over Current Protection .....	4-3
<b>Chapter 5 Recommended wiring and layout</b>	
1. Examples of Application Circuits.....	5-2
2. Recommendation and Precautions in PCB design .....	5-5
<b>Chapter 6 Mounting Guideline and Thermal Design</b>	
1. Soldering to PCB .....	6-2
2. Mounting to Heat sink .....	6-3
3. Cooler (Heat Sink) Selection.....	6-4
<b>Chapter 7 Cautions</b>	
1. Other warnings and precautions .....	7-2
2. Notice .....	7-3

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# Chapter 1

## Product Outline

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Contents	Page
1. Introduction .....	1-2
2. Product line-up .....	1-4
3. Definition of type name and marking spec .....	1-5
4. Package outline dimensions .....	1-6
5. Absolute maximum ratings .....	1-7

# 1. Introduction

The objective of this document is introducing Fuji IGBT Intelligent-Power-Module “Compact Type”.

At first, the product outline of this module is described.

Secondary, the terminal symbol and terminology used in this note and the specification sheet are explained. Next, the design guideline on signal input terminals and power terminals are shown using its structure and behavior. Furthermore, recommended wiring and layout, and the mount guideline are given.

## Feature and functions

### 1.1 Built-in drive circuit

- Drives the IGBT under optimal conditions.
  - The control IC of upper side arms have a built-in high voltage level shift circuit (HVIC).
  - This IPM is possible for driven directly by a microprocessor. Of course, the upper side arm can also be driven directly. The voltage level of input signal is 3.3V or 5V.
  - Since the wiring length between the internal drive circuit and IGBT is short and the impedance of the drive circuit is low, no reverse bias DC source is required.
  - This IPM device requires four control power sources. One is a power supply for the lower side IGBTs and control ICs. The other three power supplies are power supplies for the upper side IGBTs with proper circuit isolation.
- The IPM doesn't need insulated power supplies for the upper side drive because the IPM has a built-in bootstrap diodes (BSD).

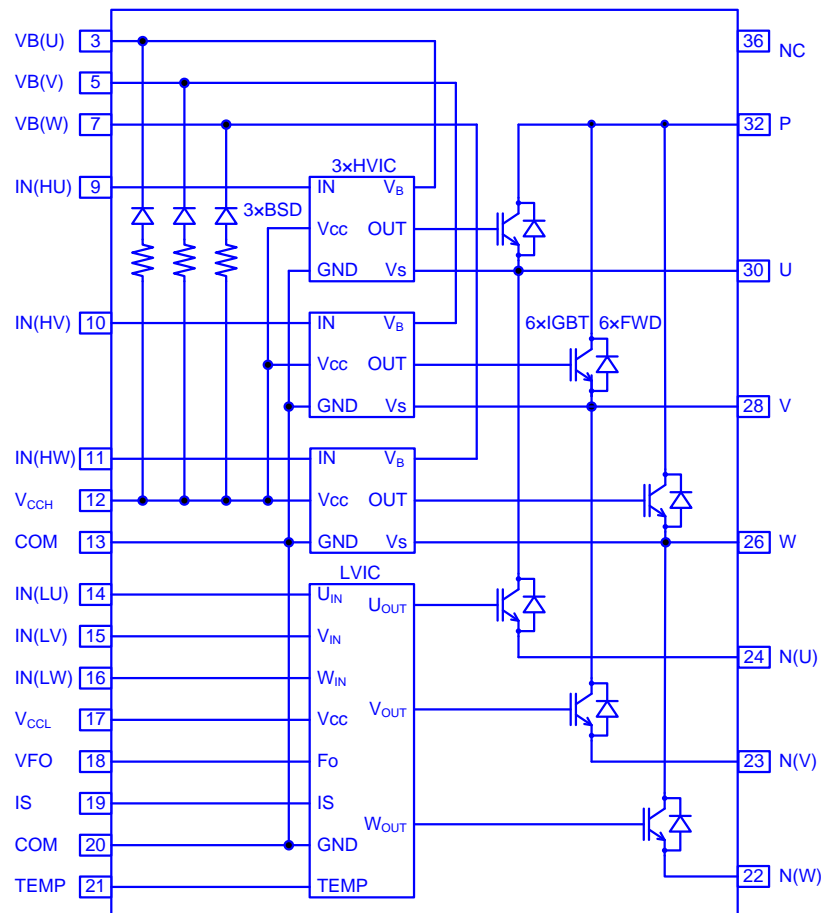


Fig. 1-1 Block Diagram of Internal Circuit

1.2 Built-in protection circuits

- The following built-in protection circuits are incorporated in the IPM device:
  - (OC): Over current protection
  - (UV): Under voltage protection for power supplies of control IC
  - (LT) or (OH): Temperature sensor output function or Overheating protection
  - (FO): Fault alarm signal output
  
- The OC protection circuits protect the IGBT against over current, load short-circuit or arm short-circuit. The protection circuit monitors the emitter current using external shunt resistor in each lower side IGBT and thus it can protect the IGBT against arm short-circuit.
- The UV protection circuit is integrated into all of the IGBT drive circuits. This protection function is effective for a voltage drop of all of the high side drive circuits and the control power supply.
- The OH protection circuit protects the IPM from overheating. The OH protection circuit is built into the control IC of the lower side arm (LVIC).
- The temperature sensor output function enables to output measured temperature as an analog voltage (built in LVIC)
- The FO function outputs a fault signal, making it possible to shutdown the system reliably by outputting the fault signal to a micro processor unit which controls the IPM when the circuit detects abnormal conditions.

1.3 Compact package

- The package of this product with an aluminum base, which further improves the heat radiation.
- The control input terminals have a shrink pitch of 1.778mm (70mil).
- The power terminals have a standard pitch of 2.54mm (100mil).
- The total dissipation loss has been improved by improvement of the trade-off between the Collector-Emitter saturation voltage  $V_{ce(sat)}$  and switching loss.

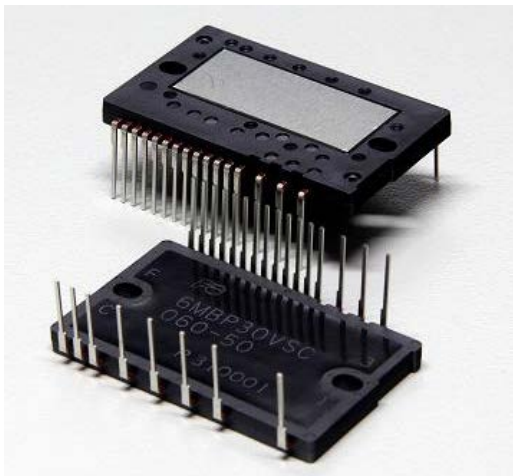


Fig.1-2 Package overview

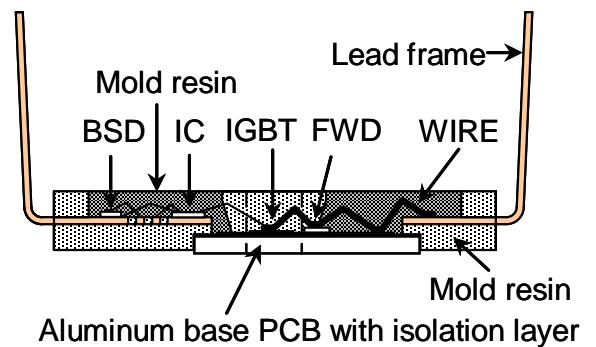


Fig.1-3 Package cross section

## 2. Product line-up and applicable products for this manual

Table. 1-1 Line-up

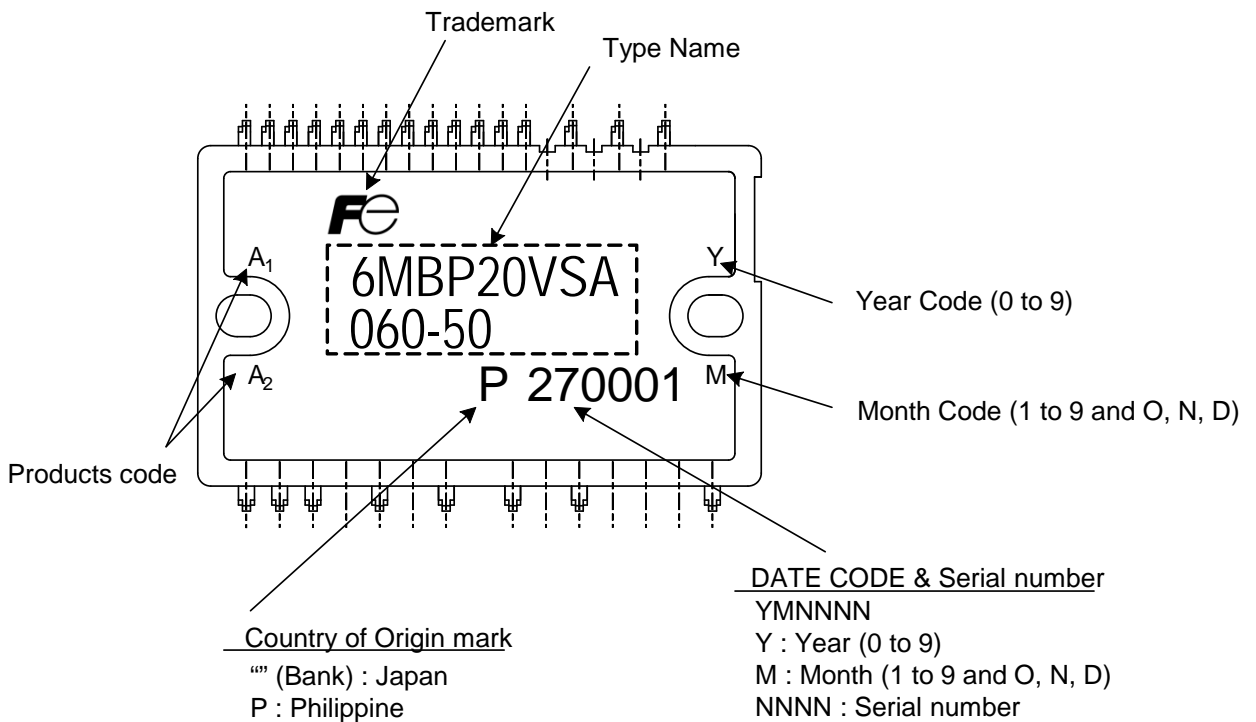
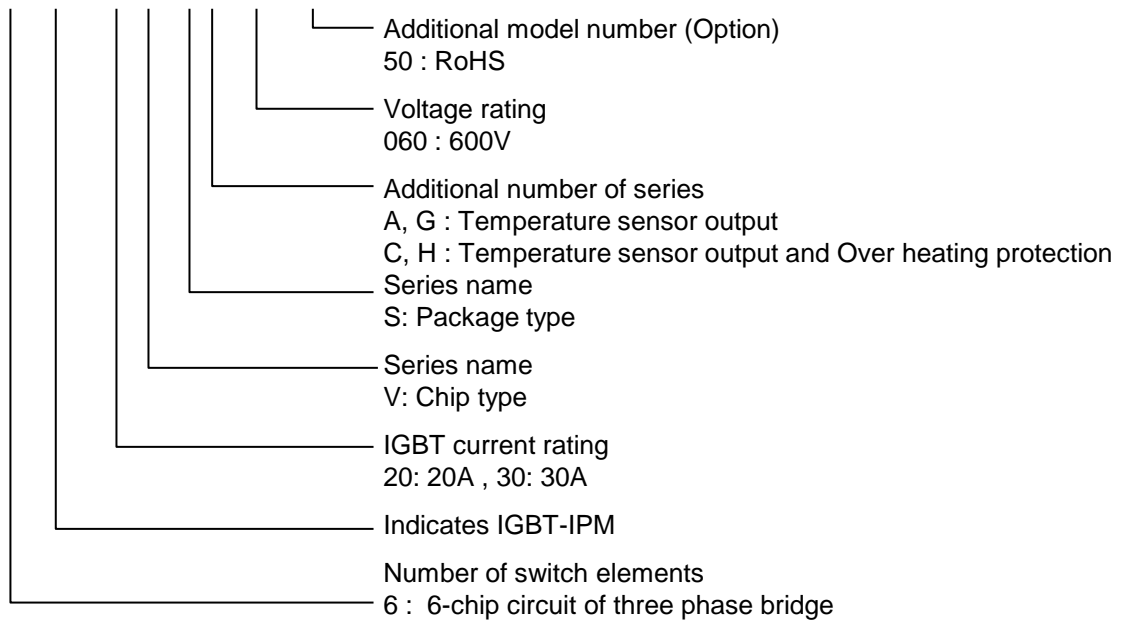
Type name	Rating of IGBT		Isolation Voltage [Vrms]	Variation	Target application
	Voltage [V]	Current [A]			
6MBP15VSG060-50	600	15	1500Vrms Sinusoidal 60Hz, 1min. (Between shorted all terminals and case)	LT*1	<ul style="list-style-type: none"> <li>▪ Roof air conditioner compressor drive</li> <li>▪ Heat pump applications</li> <li>▪ Fan motor drive</li> </ul>
6MBP15VSH060-50				LT*1 OH*1	
6MBP20VSA060-50		20		LT*1	
6MBP20VSC060-50				LT*1 OH*1	
6MBP30VSA060-50		30		LT*1	
6MBP30VSC060-50				LT*1 OH*1	

\*1 (LT): Temperature sensor output function (LT)  
(OH): Overheating protection function (OH)

### 3. Definition of Type Name and Marking Spec.

- Type name

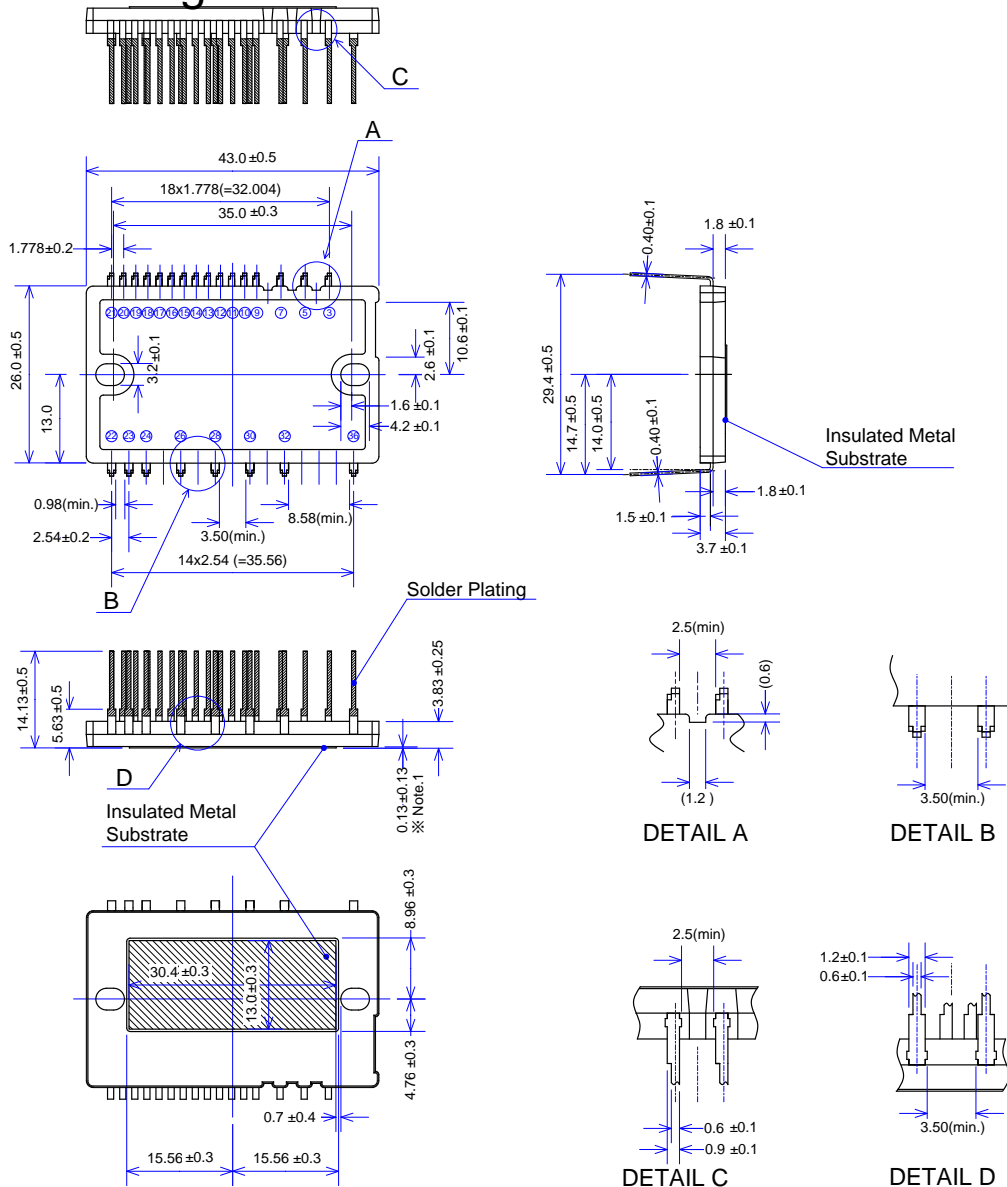
**6 MBP 20 V S A 060 -50**



Type name	Product code	
	A1	A2
6MBP15VSG060-50	F	G
6MBP15VSH060-50	F	M
6MBP20VSA060-50	G	A
6MBP20VSC060-50	G	C
6MBP30VSA060-50	I	A
6MBP30VSC060-50	I	C

Fig.1-4 Marking Specification

### 4. Package outline dimensions



Unit: mm

**Note.1**

The IMS (Insulated Metal Substrate) deliberately protruded from back surface of case. It is improved of thermal conductivity between IMS and heat-sink.

Pin No.	Pin Name	Pin No.	Pin Name
3	VB(U)	22	N(W)
5	VB(V)	23	N(V)
7	VB(W)	24	N(U)
9	IN(HU)	26	W
10	IN(HV)	28	V
11	IN(HW)	30	U
12	V <sub>CCH</sub>	32	P
13	COM	36	NC
14	IN(LU)		
15	IN(LV)		
16	IN(LW)		
17	V <sub>CCL</sub>		
18	VFO		
19	IS		
20	COM		
21	Temp		

Fig.1-5. Case outline drawings



## 5. Absolute Maximum Ratings

An example of the absolute maximum ratings of 6MBP20VSA060-50 is shown in Table 1-2.

Table 1-2 Absolute Maximum Ratings at  $T_j=25^\circ\text{C}$ ,  $V_{CC}=15\text{V}$  (unless otherwise specified)

Item	Symbol	Rating	Unit	Description
DC bus Voltage	$V_{DC}$	450	V	DC voltage that can be applied between P-N(U),N(V),N(W) terminals
Bus voltage (Surge)	$V_{DC(\text{Surge})}$	500	V	Peak value of the surge voltage that can be applied between P-N(U),N(V),N(W) terminals in switching
Collector-Emitter Voltage	$V_{CES}$	600	V	Maximum collector-emitter voltage of the built-in IGBT chip and repeated peak reverse voltage of the FWD chip
Collector Current	$I_{C@25}$	20	A	Maximum collector current for the IGBT chip $T_c=25^\circ\text{C}$ , $T_j=150^\circ\text{C}$
Peak Collector Current	$I_{CP@25}$	60	A	Maximum pulse collector current for the IGBT chip $T_c=25^\circ\text{C}$ , $T_j=150^\circ\text{C}$
Diode Forward current	$I_{F@25}$	20	A	Maximum forward current for the FWD chip $T_c=25^\circ\text{C}$ , $T_j=150^\circ\text{C}$
Peak Diode Forward current	$I_{FP@25}$	60	A	Maximum pulse forward current for the FWD chip $T_c=25^\circ\text{C}$ , $T_j=150^\circ\text{C}$
Collector Power Dissipation	$P_{D\_IGBT}$	63.1	W	Maximum power dissipation for one IGBT element at $T_c=25^\circ\text{C}$ , $T_j=150^\circ\text{C}$
FWD Power Dissipation	$P_{D\_FWD}$	30.6	W	Maximum power dissipation for one FWD element at $T_c=25^\circ\text{C}$ , $T_j=150^\circ\text{C}$
Maximum Junction Temperature of Inverter block	$T_j$	+150	$^\circ\text{C}$	Maximum junction temperature of the IGBT chips and the FWD chips
Operating Junction Temperature of Inverter block	$T_{jop}$	-40 ~ +125	$^\circ\text{C}$	Junction temperature of the IGBT and FWD chips during continuous operation
High-side Supply Voltage	$V_{CCH}$	-0.5 ~ 20	V	Voltage that can be applied between COM and $V_{CCH}$ terminal
Low-side Supply Voltage	$V_{CCL}$	-0.5 ~ 20	V	Voltage that can be applied between COM and $V_{CCL}$ terminal
High-side Bias Supply Voltage	$V_{B(U)-COM}$ $V_{B(V)-COM}$ $V_{B(W)-COM}$	-0.5 ~ 620	V	Voltage that can be applied between VB(U) terminal and COM, VB(V) terminal and COM, VB(W) terminal and COM.
High-side Bias Voltage for IGBT gate driving	$V_{B(U)}$ $V_{B(V)}$ $V_{B(W)}$	20	V	Voltage that can be applied between U terminal and VB(U) terminal, V terminal and VB(V) terminal, W terminal and VB(W) terminal.
Input Signal Voltage	$V_{IN}$	-0.5 ~ $V_{CCH}+0.5$ -0.5 ~ $V_{CCL}+0.5$	V	Voltage that can be applied between COM and each $V_{in}$ terminal
Input Signal Current	$I_{IN}$	3	mA	Maximum input current that flows from $V_{in}$ terminal to COM
Fault Signal Voltage	$V_{FO}$	-0.5 ~ $V_{CCL}+0.5$	V	Voltage that can be applied between COM and $V_{FO}$ terminal
Fault Signal Current	$I_{FO}$	1	mA	Sink current that flows from $V_{FO}$ to COM terminal

Table 1-2 Absolute Maximum Ratings at Tj=25°C, Vcc=15V (Continued)

Item	Symbol	Rating	Unit	Descriptions
Over Current sensing Input Voltage	V <sub>IS</sub>	-0.5 ~ V <sub>CCCL</sub> +0.5	V	Voltage that can be applied between IS and COM terminal
Maximum Junction Temperature of Control circuit block	T <sub>j</sub>	+150	°C	Maximum junction temperature of the control circuit block
Operating Junction Temperature of Control circuit block	T <sub>jop</sub>	-40 ~ +125	°C	Junction temperature of the control circuit block during continuous operation
Operating Case Temperature	T <sub>C</sub>	-40 ~ +125	°C	Operating case temperature (temperature of the aluminum plate directly under the IGBT or the FWD)
Storage Temperature	T <sub>stg</sub>	-40 ~ +125	°C	Range of ambient temperature for storage or transportation, when there is no electrical load
Isolation Voltage	V <sub>iso</sub>	AC 1500	V <sub>rms</sub>	Maximum effective value of the sine-wave voltage between the terminals and the heat sink, when all terminals are shorted simultaneously. (Sine wave = 60Hz / 1min)

**The Collector Emitter Voltages specified in absolute maximum rating**

Regarding the absolute maximum rating of collector-emitter voltage of the IGBT is specified below.

During operation of the IPM, the voltage between P and N(\*) is usually applied to the one phase of upper or lower side IGBT. Therefore, the voltage applied between P and N(\*) must not exceed absolute maximum ratings of IGBT. The Collector-Emitter voltages specified in absolute maximum rating are described below.

N(\*): N(U),N(V),N(W)

$V_{CES}$  :Absolute Maximum rating of IGBT Collector Emitter Voltage.

$V_{DC}$  :DC bus voltage Applied between P and N(\*).

$V_{DC(Surge)}$  :The total of DC bus voltage and surge voltage which generated by the wiring (or pattern) inductance from P-N(\*) terminal to the bulk capacitor.

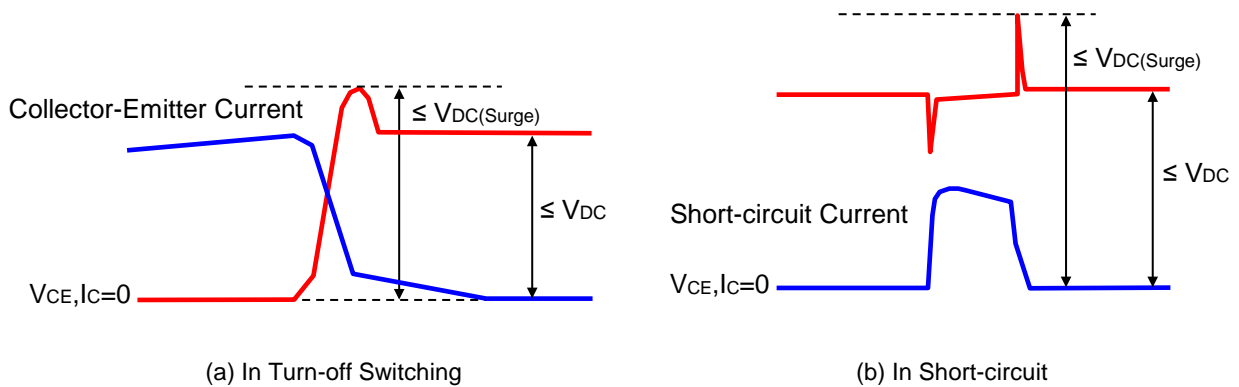


Fig. 1-6 The Collector- Emitter voltages to be considered.

Fig. 1-6 shows an example waveforms of turn-off and short-circuit of the IPM. The  $V_{DC(surge)}$  is different in the each situation, therefore,  $V_{DC}$  should be set considering these situation.  $V_{CES}$  represents the absolute maximum rating of IGBT Collector-Emitter voltage. And  $V_{DC(Surge)}$  is specified considering the margin of the surge voltage which is generated by the wiring inductance in this IPM. Furthermore,  $V_{DC}$  is specified considering the margin of the surge voltage which is generated by the wiring (or pattern) stray inductance between the P-N(\*) terminal and the capacitor.

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## Chapter 2

# Description of Terminal Symbols and Terminology

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Contents	Page
1. Description of Terminal Symbols .....	2-2
2. Description of Terminology .....	2-3

## 1. Description of Terminal Symbols

Table 2-1 and 2-2 show the description of terminal symbols and terminology respectively.

Table 2-1 Description of Terminal Symbols

Pin No.	Pin Name	Pin Description
3	VB(U)	High side bias voltage for U-phase IGBT driving
5	VB(V)	High side bias voltage for V-phase IGBT driving
7	VB(W)	High side bias voltage for W-phase IGBT driving
9	IN(HU)	Signal input for high side U-phase
10	IN(HV)	Signal input for high side V-phase
11	IN(HW)	Signal input for high side W-phase
12	V <sub>CCH</sub>	High side control supply
13	COM	Common supply ground
14	IN(LU)	Signal input for low side U-phase
15	IN(LV)	Signal input for low side V-phase
16	IN(LW)	Signal input for low side W-phase
17	V <sub>CCL</sub>	Low side control supply
18	VFO	Fault output
19	IS	Over current sensing voltage input
20	COM	Common supply ground
21	TEMP	Temperature sensor output
22	N(W)	Negative bus voltage input for W-phase
23	N(V)	Negative bus voltage input for V-phase
24	N(U)	Negative bus voltage input for U-phase
26	W	Motor W-phase output
28	V	Motor V-phase output
30	U	Motor U-phase output
32	P	Positive bus voltage input
36	NC	No Connection

## 2. Description of Terminology

Table 2-2 Description of Terminology

(1) Inverter block

Item	Symbol	Description
Zero gate Voltage Collector current	$I_{CES}$	Collector current when a specified voltage is applied between the collector and emitter of an IGBT with all input signals L (=0V)
Collector-emitter saturation voltage	$V_{CE(sat)}$	Collector-emitter voltage at a specified collector current when the input signal of only the element to be measured is H (= 5V) and the inputs of all other elements are L (=0V)
FWD forward voltage drop	$V_F$	Forward voltage at a specified forward current with all input signals L (=0V)
Turn-on time	$t_{on}$	The time from the input signal rising above the threshold value until the collector current becomes 90% of the rating. See Fig. 2-1.
Turn-on delay	$t_{d(on)}$	The time from the input signal rising above the threshold value until the collector current decreases to 10% of the rating. See Fig. 2-1.
Turn-on rise time	$t_r$	The time from the collector current becoming 10% at the time of IGBT turn-on until the collector current becomes 90%. See Fig. 2-1.
VCE-IC Cross time of turn-on	$t_{c(on)}$	The time from the collector current becoming 10% at the time of IGBT turn on until the VCE voltage of IGBT dropping below 10% of the rating. See Fig. 2-1.
Turn-off time	$t_{off}$	The time from the input signal dropping below the threshold value until the VCE voltage of IGBT becomes 90% of the rating. See Fig. 2-1.
Turn-off delay	$t_{d(off)}$	The time from the input signal dropping below the threshold value until the collector current decreases to 90%. See Fig. 2-1.
Turn-on fall time	$t_f$	The time from the collector current becoming 90% at the time of IGBT turn-off until the collector current decreases to 10%. See Fig. 2-1.
VCE-IC Cross time of turn-off	$t_{c(off)}$	The time from the VCE voltage becoming 10% at the time of IGBT turn ff until the collector current dropping below 10% of the rating. See Fig. 2-1.
FWD Reverse recovery time	$t_{rr}$	The time required for the reverse recovery current of the built-in diode to disappear. See Fig. 2-1.

(2) Control circuit block

Item	Symbol	Description
Circuit current of Low-side drive IC	$I_{CCL}$	Current flowing between control power supply $V_{CCL}$ and COM
Circuit current of High-side drive IC	$I_{CCH}$	Current flowing between control power supply $V_{CCH}$ and COM
Circuit current of Bootstrap circuit	$I_{CCHB}$	Current flowing between upper side IGBT bias voltage supply $V_{B(U)}$ and $U, V_{B(V)}$ and $V$ or $V_{B(W)}$ and $W$ on the P-side (per one unit)
Input Signal threshold voltage	$V_{th(on)}$	Control signal voltage when IGBT changes from OFF to ON
	$V_{th(off)}$	Control signal voltage when IGBT changes from ON to OFF
Input Signal threshold hysteresis voltage	$V_{th(hys)}$	The hysteresis voltage between $V_{th(on)}$ and $V_{th(off)}$ .
Operational input pulse width	$t_{IN(on)}$	Control signal pulse width necessary to change IGBT from OFF to ON. Refer Chapter 3 section 4.
Operational input pulse width	$t_{IN(off)}$	Control signal pulse width necessary to change IGBT from ON to OFF. Refer Chapter 3 section 4.

Table 2-2 Description of Terminology

(2) Control circuit block (Continued)

Item	Symbol	Description
Input current	$I_{IN}$	Current flowing between signal input IN(HU,HV,HW,LU,LV,LW) and COM.
Input pull-down resistance	$R_{IN}$	Input resistance of resistor in input terminals IN(HU,HV,HW,LU,LV,LW). They are inserted between each input terminal and COM.
Fault output voltage	$V_{FO(H)}$	Output voltage level of VFO terminal under the normal operation (The lower side arm protection function is not actuated.) with pull-up resistor 10k $\Omega$ .
	$V_{FO(L)}$	Output voltage level of VFO terminal after the lower side arm protection function is actuated.
Fault output pulse width	$t_{FO}$	Period in which an fault status continues to be output (VFO) from the VFO terminal after the lower side arm protection function is actuated. Refer chapter 3 section 6.
Over current protection voltage level	$V_{IS(ref)}$	Threshold voltage of IS terminal at the over current protection. Refer chapter 3 section 5.
Over Current Protection Trip delay time	$t_{d(IS)}$	The time from the Over current protection triggered until the collector current becomes 50% of the rating. Refer chapter 3 section 5.
Output Voltage of temperature sensor	$V(temp)$	The output voltage of temp. It is applied to the temperature sensor output model. Refer chapter 3 section 7.
Overheating protection temperature	TOH	Tripping temperature of over heating. The temperature is observed by LVIC. All low side IGBTs are shut down when the LVIC temperature exceeds overheating threshold. See Fig.2-2 and refer chapter 3 section 8.
Overheating protection hysteresis	TOH(hys)	Hysteresis temperature required for output stop resetting after protection operation. See Fig.2-2 and refer chapter 3 section 8. TOH and TOH(hys) are applied to the overheating protection model.
Vcc Under voltage trip level of Low-side	$V_{CCL(OFF)}$	Tripping voltage in under voltage of the Low-side control IC power supply. All low side IGBTs are shut down when the voltage of $V_{CCL}$ drops below this threshold. Refer chapter 3 section 1.
Vcc Under voltage reset level of Low-side	$V_{CCL(ON)}$	Resetting threshold voltage from under voltage trip status of $V_{CCL}$ . Refer chapter 3 section 1.
Vcc Under voltage hysteresis of Low-side	$V_{CCL(hys)}$	Hysteresis voltage between $V_{CCL(OFF)}$ and $V_{CCL(ON)}$ .
Vcc Under voltage trip level of High-side	$V_{CCH(OFF)}$	Tripping voltage in under voltage of High-side control IC power supply. The IGBTs of high-side are shut down when the voltage of $V_{CCH}$ drops below this threshold. Refer chapter 3 section 1.
Vcc Under voltage reset level of High-side	$V_{CCH(ON)}$	Resetting threshold voltage from under voltage trip status of $V_{CCH}$ . See Fig.3-3 Resetting voltage at which the IGBT performs shutdown when the High-side control power supply voltage $V_{CCH}$ drops. Refer chapter 3 section 1.
Vcc Under voltage hysteresis of High-side	$V_{CCH(hys)}$	Hysteresis voltage between $V_{CCH(OFF)}$ and $V_{CCH(ON)}$ .
VB Under voltage trip level	$V_{B(OFF)}$	Tripping voltage in under voltage of $V_B(^*)$ . The IGBTs of high-side are shut down when the voltage of $V_B(^*)$ drops below this threshold. Refer chapter 3 section 2.
VB Under voltage reset level	$V_{B(ON)}$	Resetting voltage at which the IGBT performs shutdown when the upper side arm IGBT bias voltage $V_B(^*)$ drops. Refer chapter 3 section 2.
VB Under voltage hysteresis	$V_{B(hys)}$	Hysteresis voltage between $V_{B(OFF)}$ and $V_{B(ON)}$ .

Table 2-2 Description of Terminology

(3) BSD block

Item	Symbol	Description
Forward voltage of Bootstrap diode	$V_{F(BSD)}$	BSD Forward voltage at a specified forward current.

(4) Thermal Characteristics

Item	Symbol	Description
Junction to Case Thermal Resistance (per single IGBT)	$R_{th(j-c)}_{IGBT}$	Thermal resistance from the junction to the case of single IGBT.
Junction to Case Thermal Resistance (per single FWD)	$R_{th(j-c)}_{FWD}$	Thermal resistance from the junction to the case of single FWD.
Case to Heat sink Thermal Resistance	$R_{th(c-f)}$	Thermal resistance between the case and heat sink, when mounted on a heat sink at the recommended torque using the thermal compound

(5) Mechanical Characteristics

Item	Symbol	Description
Tighten torque	-	Screwing torque when mounting the IPM to a heat sink with a specified screw.
Heat-sink side flatness	-	Flatness of a heat sink side. See Fig.2-3.

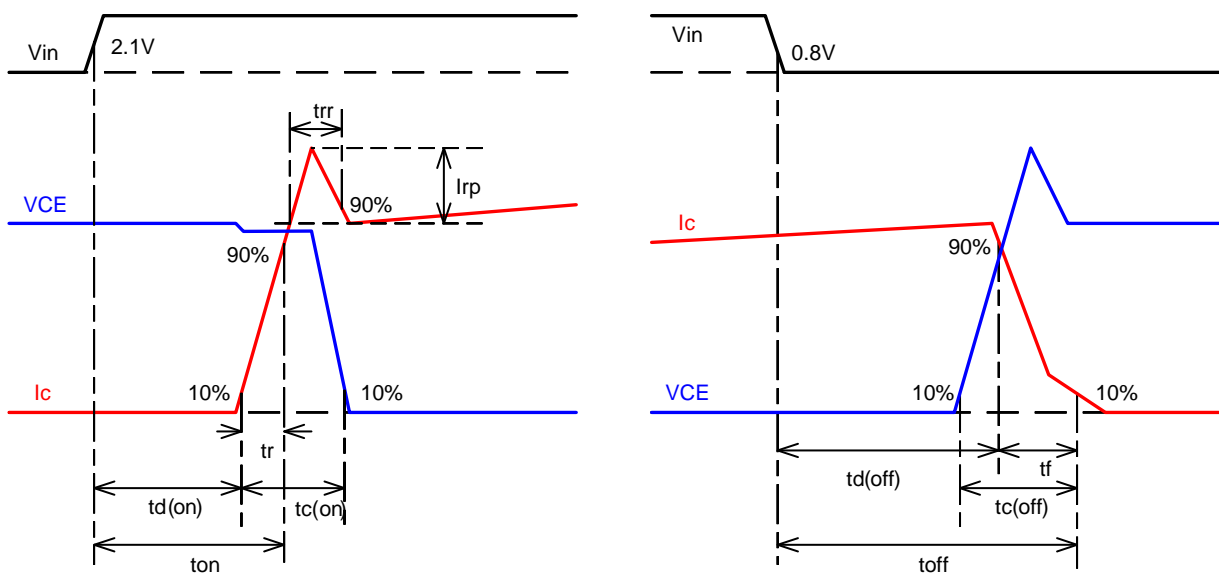


Fig.2-1 Switching waveforms



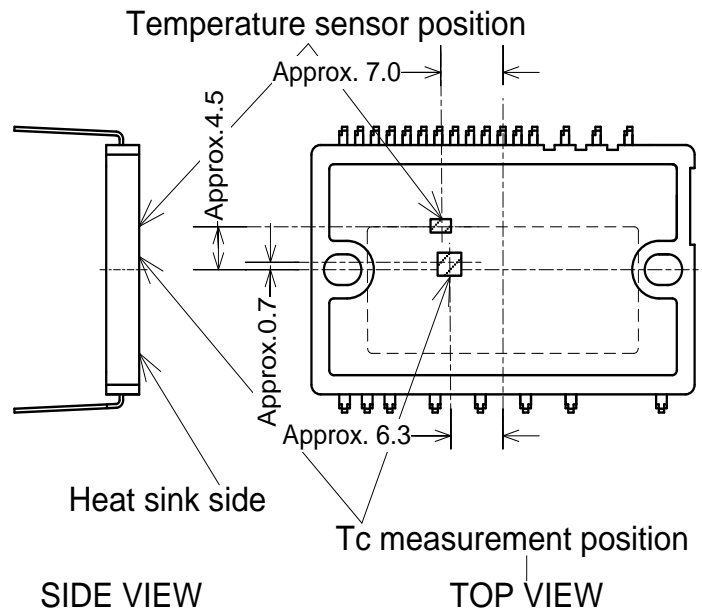


Fig.2-2 The measurement position of temperature sensor and Tc.

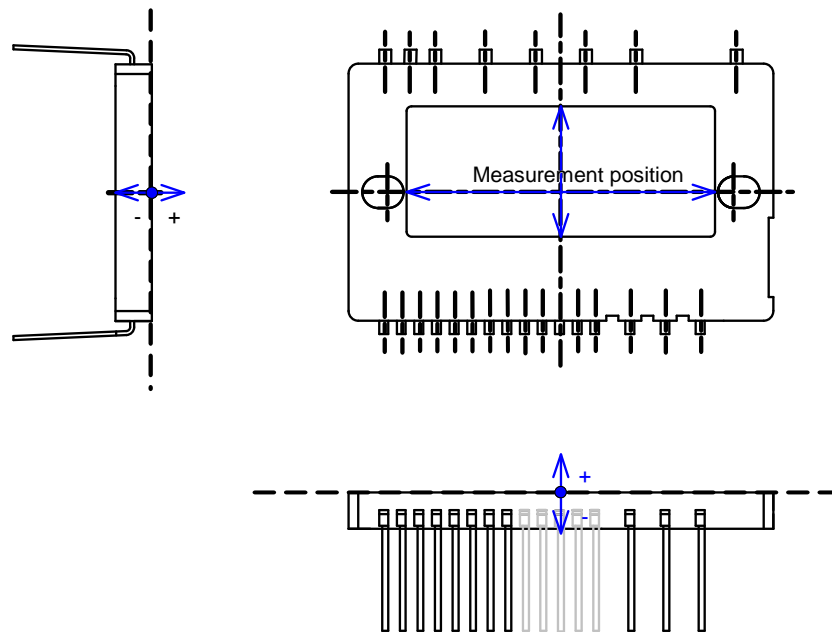


Fig.2-3 The measurement point of heat-sink side flatness.

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## Chapter 3

# Detail of Signal Input/Output Terminals

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Contents	Page
1. Control Power Supply Terminals $V_{CCH}, V_{CCL}, COM$ .....	3-2
2. Power Supply Terminals of High Side $VB(U, V, W)$ .....	3-6
3. Function of Internal BSDs (Boot Strap Diodes) .....	3-9
4. Input Terminals $IN(HU, HV, HW), IN(LU, LV, LW)$ .....	3-13
5. Over Current Protection Input Terminal $IS$ .....	3-16
6. Fault Status Output Terminal $VFO$ .....	3-17
7. Temperature Sensor Output Terminal $TEMP$ .....	3-18
8. Over Heat Protection .....	3-20

# 1. Control Power Supply Terminals $V_{CCH}$ , $V_{CCL}$ , COM

## 1. Voltage Range of control power supply terminals $V_{CCH}$ , $V_{CCL}$

Please connect a single 15Vdc power supply between  $V_{CCH}$ ,  $V_{CCL}$  and COM terminals for the IPM control power supply. The voltage should be regulated to  $15V \pm 10\%$  for proper operation. Table 3-1 describes the behavior of the IPM for various control supply voltages. A low impedance capacitor and a high frequency decoupling capacitor should be connected close to the terminals of the power supply.

High frequency noise on the power supply might cause a malfunction of the internal control IC or erroneous fault signal output. To avoid these problems, the maximum amplitude of voltage ripple on the power supply should be less than  $\pm 1V/\mu s$ .

The potential at the COM terminal is different from that at the  $N(*)^{*1}$  power terminal. It is very important that all control circuits and power supplies are referred to the COM terminal and not to the  $N(*)^{*1}$  terminals. If circuits are improperly connected, an additional current might flow through the sense resistor and it cause an improper operation of the short-circuit protection function. In general, it is best practice to make the COM as the ground in the PCB layout.

The main control power supply is also connected to the bootstrap circuit which provide a power to floating supplies for the high side gate drivers.

When high side control supply voltage ( $V_{CCH}$  and COM) falls down under  $V_{CCH}$  UV (Under Voltage protection) level, only the IGBT which occurred the under voltage condition becomes off-state even though the input signal is ON condition.

When low side control supply voltage ( $V_{CCL}$  and COM) falls down under  $V_{CCL}$  UV level, all lower side IGBTs become off-state even though the input signal is ON condition.

Table 3-1 Functions versus supply voltage  $V_{CCH}$ ,  $V_{CCL}$

Control Voltage Range [V]	Function Operations
0 ~ 4	The IPM doesn't work. UV and fault output are not activated. dV/dt noise on the main P-N supply might cause a malfunction of the IGBTs.
4 ~ 13	The IPM start to work. UV is activated, control input signals are blocked and a fault output VFO is generated.
13 ~ 13.5	UV is reset. IGBTs are operated in accordance with the control gate input. Driving voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition and high side IGBTs can't operate after $V_{B(*)}^{*2}$ initial charging because $V_{B(*)}$ can't reach to $V_{B(ON)}$ .
13.5 ~ 16.5	Normal operation. This is the recommended operating condition.
16.5 ~ 20	The lower side IGBTs are still operated. Because driving voltage is above the recommended range, IGBT's switching is faster. It causes increasing system noise. And peak short circuit current might be too large for proper operation of the short circuit protection.
Over 20	Control circuit in this IPM might be damaged. If necessary, it is recommended to insert a zener-diode between each pair of control supply terminals.

\*1  $N(*)$  :  $N(U)$ ,  $N(V)$ ,  $N(W)$

\*2  $V_{B(*)}$  :  $V_{B(U)-U}$ ,  $V_{B(V)-V}$ ,  $V_{B(W)-W}$

2. Under Voltage protection of control power supply terminals  $V_{CCH}$ ,  $V_{CCL}$

Fig.3-1 shows the UV protection circuit of high side and low side control supply( $V_{CCH}$ , $V_{CCL}$ ). Fig.3-2 and Fig.3-3 shows the sequence of UV operation of  $V_{CCH}$  and  $V_{CCL}$ .

As shown in Fig.3-1, a diode is electrically connected to the  $V_{CCH}$ ,  $V_{CCL}$  and COM terminals. The diode should not be used for a voltage clamp intentionally otherwise the IPM might be damaged.

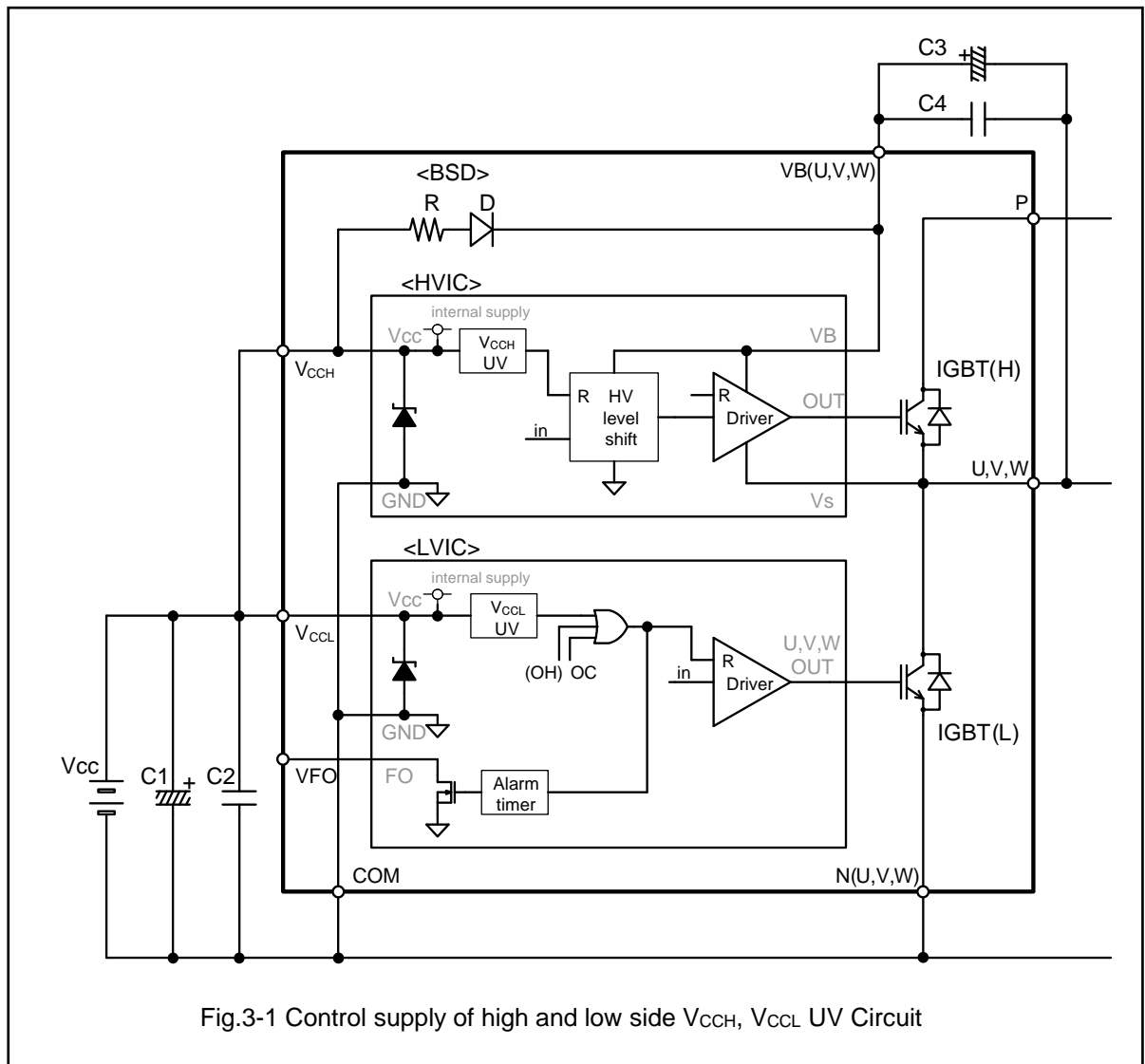
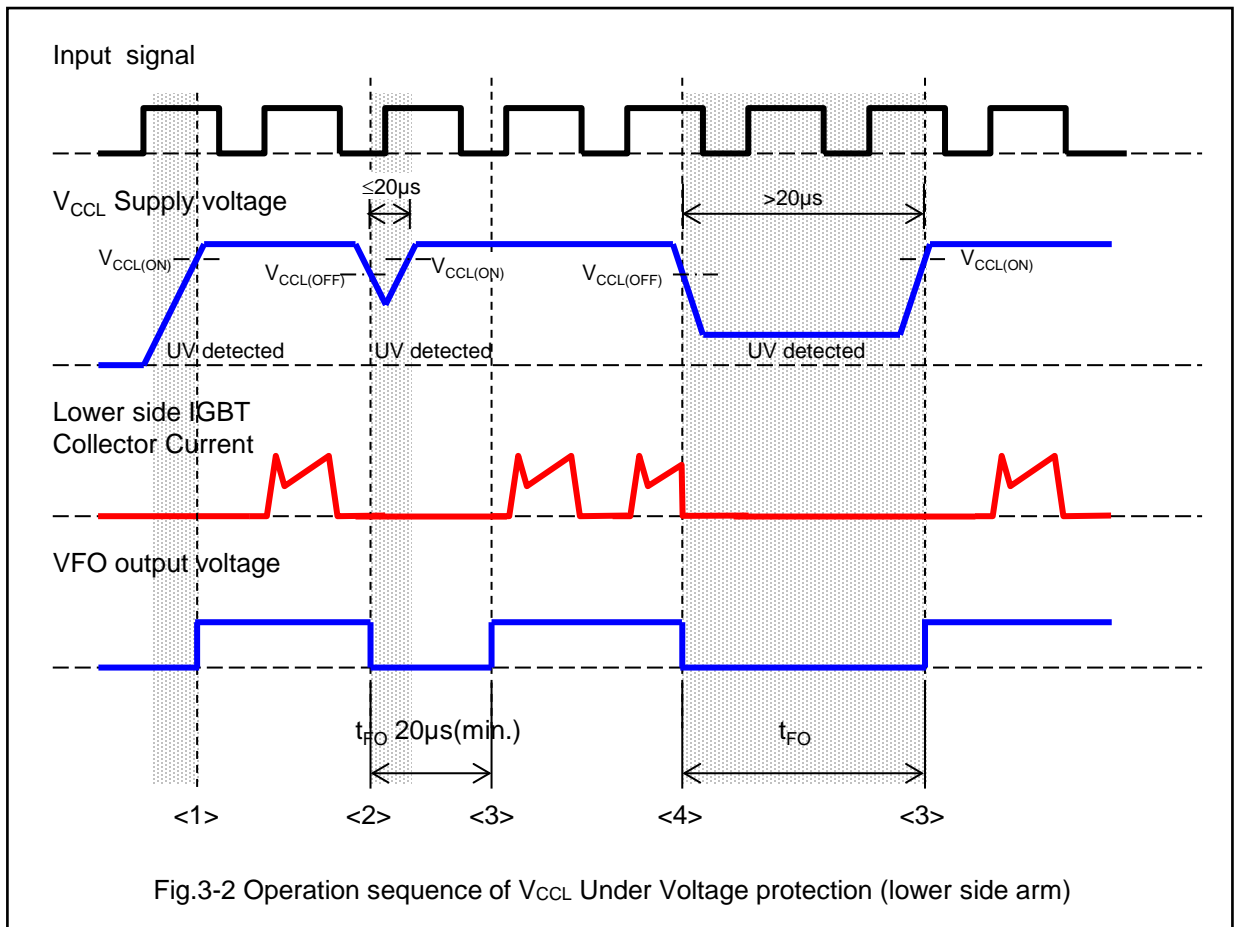
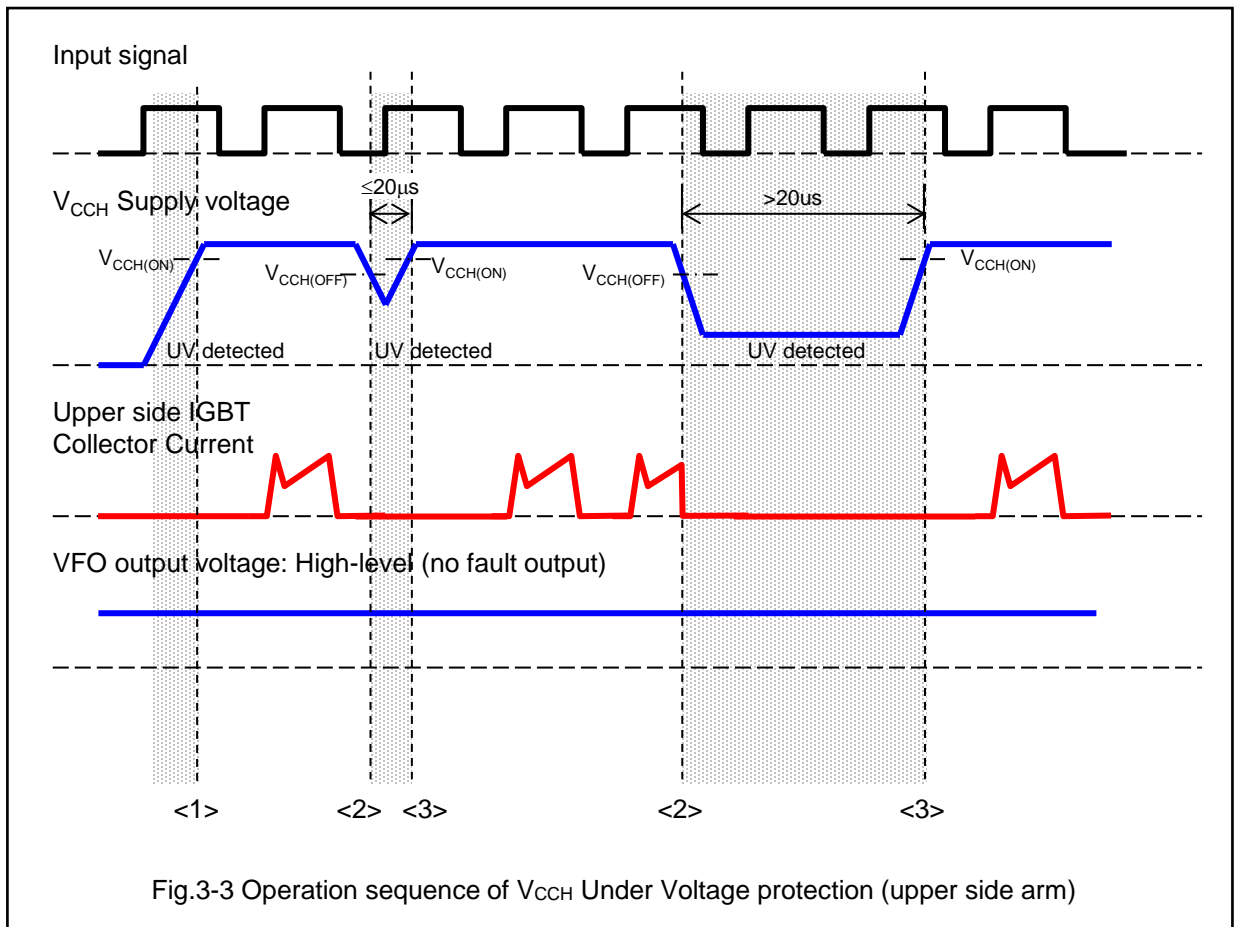


Fig.3-1 Control supply of high and low side  $V_{CCH}$ ,  $V_{CCL}$  UV Circuit



- <1> When  $V_{CCL}$  is lower than  $V_{CCL(ON)}$ , all lower side IGBTs are OFF state.  
After  $V_{CCL}$  exceeding  $V_{CCL(ON)}$ , the fault output VFO is released (high level).  
And the LVIC starts to operate, then next input is activated.
- <2> The fault output VFO is activated when  $V_{CCL}$  falls below  $V_{CCL(OFF)}$ , and all lower side IGBT remains OFF state.  
If the voltage drop time is less than  $20\mu s$ , the minimum pulse width of the fault output signal is  $20\mu s$  and all lower side IGBTs are OFF state regardless of the input signal condition.
- <3> UV is reset after  $t_{FO}$  and  $V_{CCL}$  exceeding  $V_{CCL(ON)}$ , then the fault output VFO is reset simultaneously.  
After that the LVIC starts to operate from the next input signal.
- <4> When the voltage drop time is more than  $t_{FO}$ , the fault output pulse width is generated and all lower side IGBTs are OFF state regardless of the input signal condition during the same time.



- <1> When  $V_{CCH}$  is lower than  $V_{CCH(ON)}$ , the upper side IGBT is OFF state.  
After  $V_{CCH}$  exceeds  $V_{CCH(ON)}$ , the HVIC starts to operate from the next input signals.  
The fault output VFO is constant (high level) regardless  $V_{CCH}$ .
- <2> After  $V_{CCH}$  falls below  $V_{CCH(OFF)}$ , the upper side IGBT remains OFF state.  
But the fault output VFO keeps high level.
- <3> The HVIC starts to operate from the next input signal after UV is reset.

## 2. Power Supply Terminals of High Side VB(U,V,W)

### 1. Voltage Range of high side bias voltage for IGBT driving terminals VB(U,V,W)

The VB(\*) voltage, which is the voltage difference between VB(U,V,W) and U,V,W, provides the supply to the HVICs within the IPM. This supply must be in the range of 13.0~18.5V to ensure that the HVICs can fully drive the upper side IGBTs. The IPM includes UV function for the VB(\*) to ensure that the HVICs do not drive the upper side IGBTs, if the VB(\*) voltage drops below a specified voltage (refer to the datasheet). This function prevents the IGBT from operating in a high dissipation mode. Please note here, that the UV (under voltage protection) function of any high side section acts only on the triggered channel without any feedback to the control level.

In case of using bootstrap circuit, the IGBT drive power supply for upper side arms can be composed of one common power supply with a lower side arm. In the conventional IPM, three independent insulated power supplies were necessary for IGBT drive circuit of upper side arm.

The power supply of the upper side arm is charged when the lower side IGBT is turned on or freewheel current flows the lower side IGBT. Table 3-2 describes the behavior of the IPM for various control supply voltages. The control supply should be well filtered with a low impedance capacitor and a high frequency decoupling capacitor connected close to the terminals in order to prevent a malfunction of the internal control IC caused by a high frequency noise on the power supply.

When control supply voltage (VB(U)-U,VB(V)-V and VB(W)-W) falls down under UV (Under Voltage protection) level, only triggered phase IGBT is off-state regardless the input signal condition.

Table 3-2 Functions versus high side bias voltage for IGBT driving VB(\*)

Control Voltage Range [V]	The IPM function operations
0 ~ 4	HVICs are not activated. UV does not operate. dV/dt noise on the main P-N supply might trigger the IGBTs.
4 ~ 12.5	HVICs start to operate. As the UV is activated, control input signals are blocked.
12.5 ~ 13	UV is reset. The upper side IGBTs are operated in accordance with the control gate input. Driving voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition.
13 ~ 18.5	Normal operation. This is the recommended operating condition.
18.5 ~ 20	The upper side IGBTs are still operated. Because driving voltage is above the recommended range, IGBT's switching is faster. It causes increasing system noise. And peak short circuit current might be too large for proper operation of the short circuit protection.
Over 20	Control circuit in the IPM might be damaged. It is recommended to insert a zener-diode between each pair of high side power supply terminals.

2. Under Voltage protection of high side power supply terminals VB(U,V,W)

Fig.3-4 shows of high side (VB(U)-U,VB(V)-V and VB(W)-W) UV (Under Voltage protection) circuit block of the control power supply.

Fig.3-5 shows operation sequence of VB(U)-U,VB(V)-V,VB(W)-W Under Voltage operation.

As shown in Fig.3-4, diodes are electrically connected to the VB(U,V,W), U,V,W and COM terminals. These diodes protect the IPM from an input surge voltage. Don't use these diodes for a voltage clamp because the IPM might be destroyed if the diodes are used as a voltage clamp.

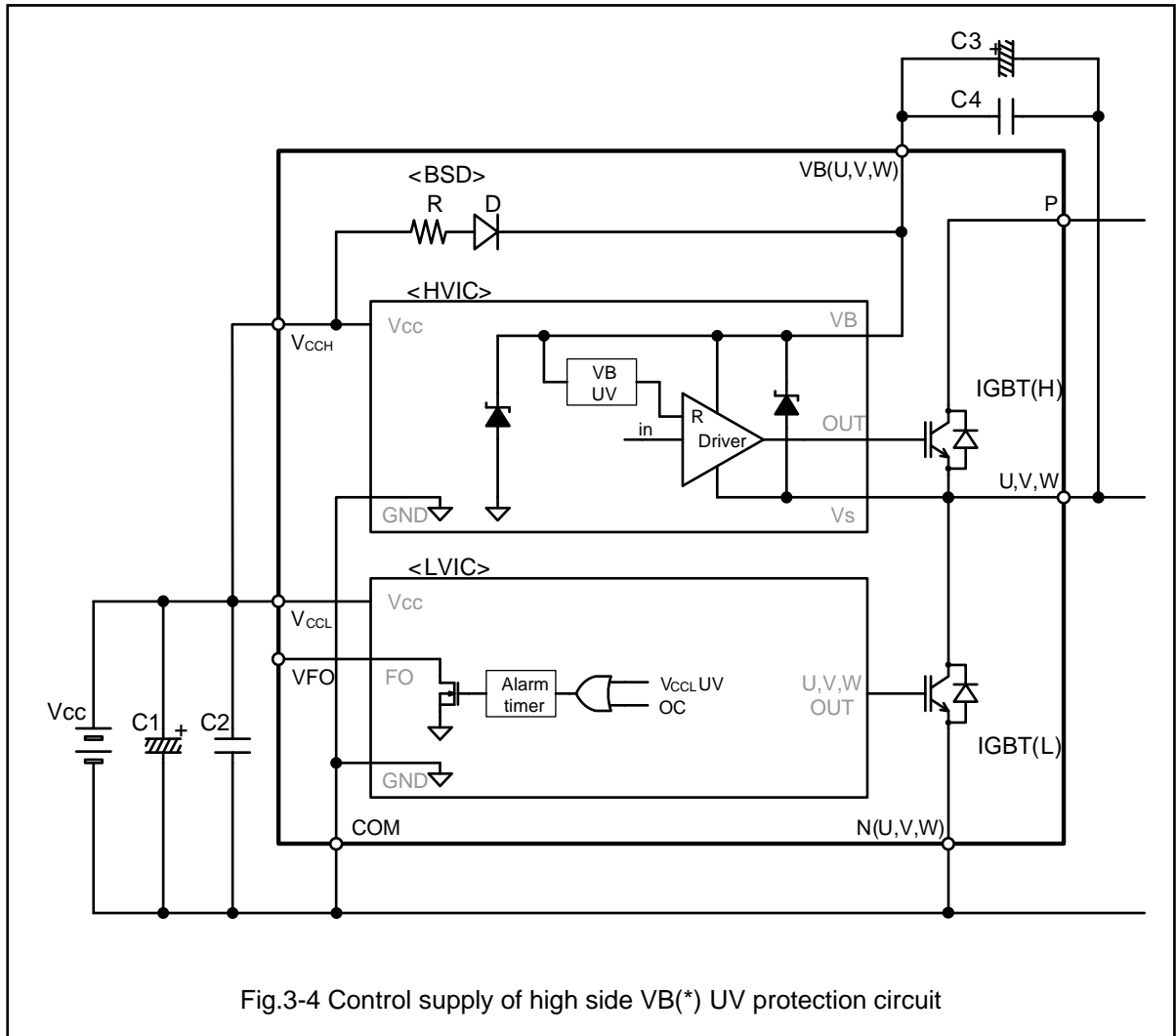
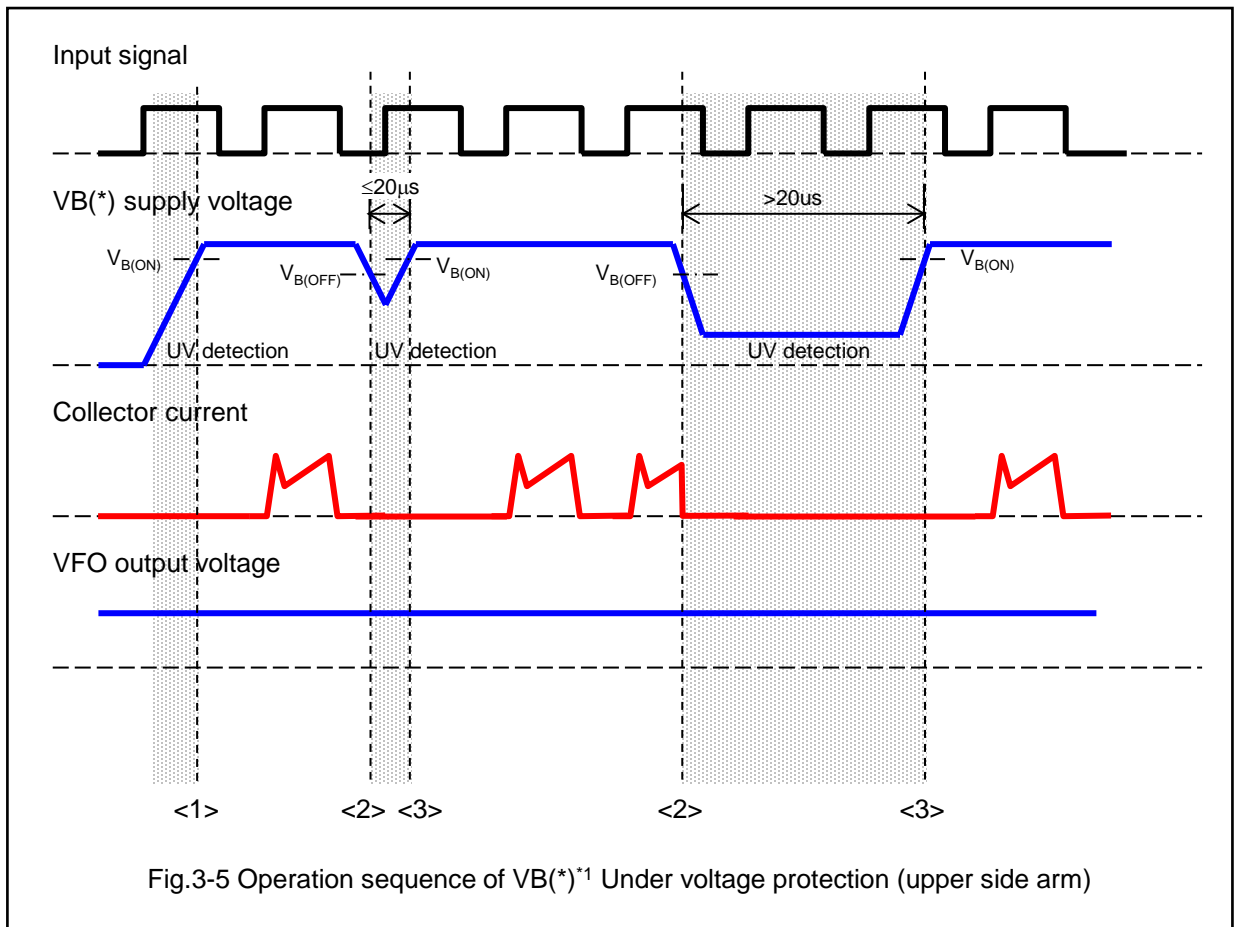


Fig.3-4 Control supply of high side VB(\*) UV protection circuit





- <1> When VB(\*) is under  $V_{B(ON)}$ , the upper side IGBT is OFF state.  
After VB(\*) exceeds  $V_{B(ON)}$ , the HVIC starts to operate from the next input signal.  
The fault output VFO is constant (high level) regardless VB(\*).
- <2> After VB(\*) falls below  $V_{B(OFF)}$ , the upper side IGBT remains OFF state.  
But the fault output VFO keeps high level.
- <3> The HVIC starts to operate from the next input signal after UV is reset.

\*1 VB(\*) : VB(U)-U,VB(V)-V,VB(W)-W

### 3. Function of Internal BSDs (bootstrap Diodes)

There are several ways in which the  $V_B^{(*)}$  floating supply can be generated. Bootstrap method is described here. The boot strap method is a simple and cheap solution. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. As show in the Fig. 3-6, Fig. 3-8 and Fig. 3-11, the boot strap circuit consists of bootstrap diode and resistor which are integrated in the IPM and an external capacitor.

#### 1.Chargin and Discharging of Bootstrap Capacitor During Inverter Operation

##### a) Charging operation timing chart of bootstrap capacitor (C)

<Sequence (Fig.3-7) : lower side IGBT is turned on in Fig.3-6>

When lower side IGBT is ON state, the charging voltage on the bootstrap capacitance  $V_c(t1)$  is calculated by the following equations.

$$V_C(t1) = V_{CC} - V_F - V_{CE(sat)} - I_b \cdot R \quad \dots\dots \text{Transient state}$$

$$V_C(t1) \approx V_{CC} \quad \dots\dots \text{Steady state}$$

- $V_F$  : Forward voltage of Boost strap diode (D)
- $V_{CE(sat)}$  : Saturation voltage of lower side IGBT
- R : Bootstrap resistance for inrush current limitation (R)
- $I_b$  : Charge current of bootstrap

When lower side IGBT is turned off, then the motor current flows through the free-wheel path of the upper side FWD. Once the electric potential of VS rises near to that of P terminal, the charging of C is stopped, and the voltage of C gradually declines due to a current consumed by the drive circuit.

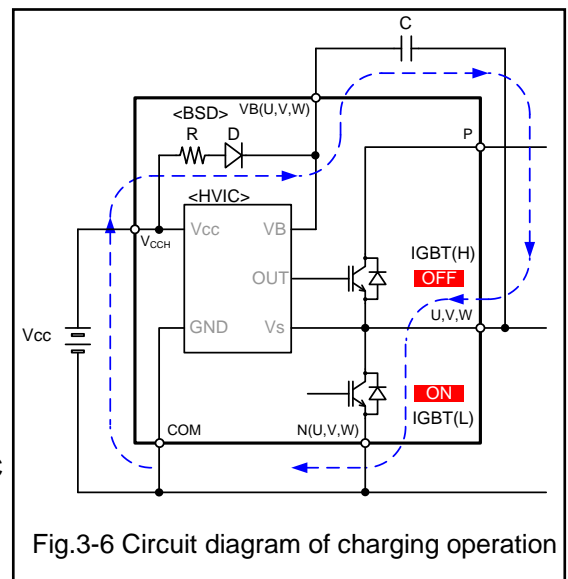


Fig.3-6 Circuit diagram of charging operation

\*1  $V_B^{(*)}$  :  $V_B(U)-U, V_B(V)-V, V_B(W)-W$

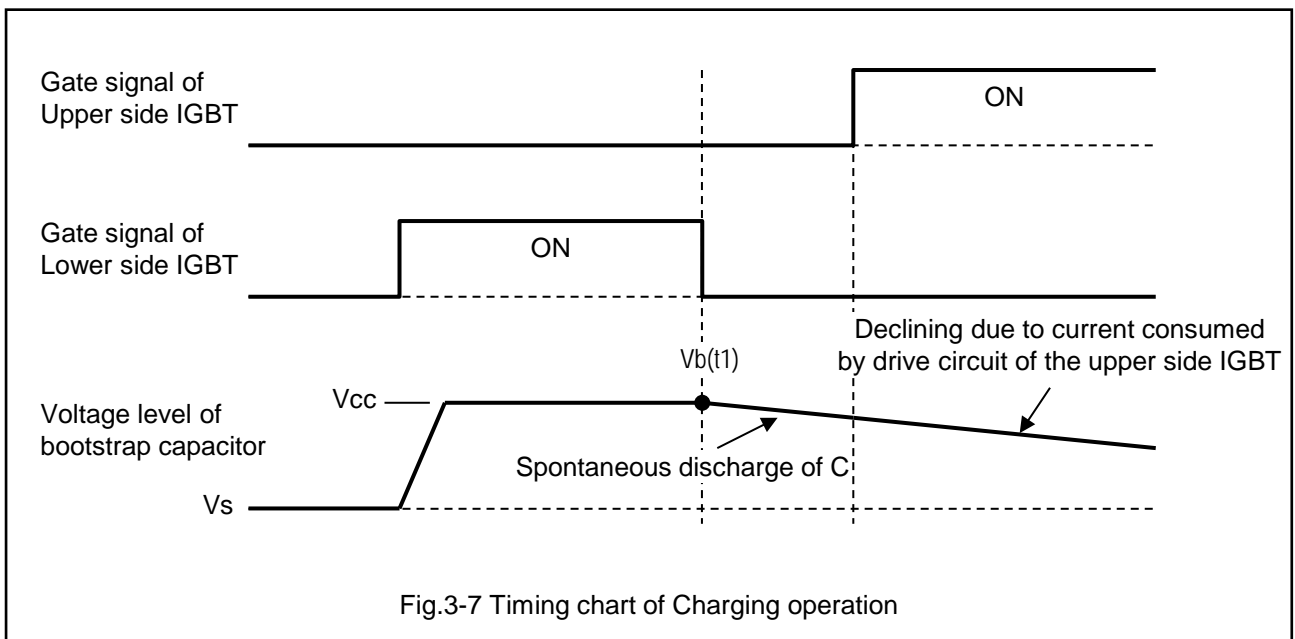


Fig.3-7 Timing chart of Charging operation

<Sequence (Fig.3-9): Lower side IGBT is OFF and Lower side FWD is ON (Freewheel current flows) in Fig.3-8 >

When the lower side IGBT is OFF and the lower side FWD is ON, a free wheeling current flows the lower side FWD. The voltage on the bootstrap capacitance  $V_c(t_2)$  is calculated by the following equations:

$$V_c(t_2) = V_{CC} - V_F + V_{F(FWD)} - I_b \cdot R \quad \dots\dots \text{Transient state}$$

$$V_c(t_2) \approx V_{CC} \quad \dots\dots \text{Steady state}$$

$V_F$  : Forward voltage of Boost strap diode (D)  
 $V_{F(FWD)}$  : Forward voltage of lower side FWD

$R$  : Bootstrap resistance for inrush current limitation (R)  
 $I_b$  : Charge current of bootstrap

When both the lower side IGBT and the upper side IGBT are OFF, a regenerative current flows continuously through the freewheel path of the lower side FWD. Therefore the potential of  $V_s$  drops to  $-V_F$ , then the bootstrap capacitor is re-charged to restore the declined potential. When the upper side IGBT is turned ON and the potential of  $V_s$  exceeds  $V_{CC}$ , the charging of the bootstrap capacitor stops and the voltage on the bootstrap capacitor gradually declines due to consumption of the stored energy by the drive circuit.

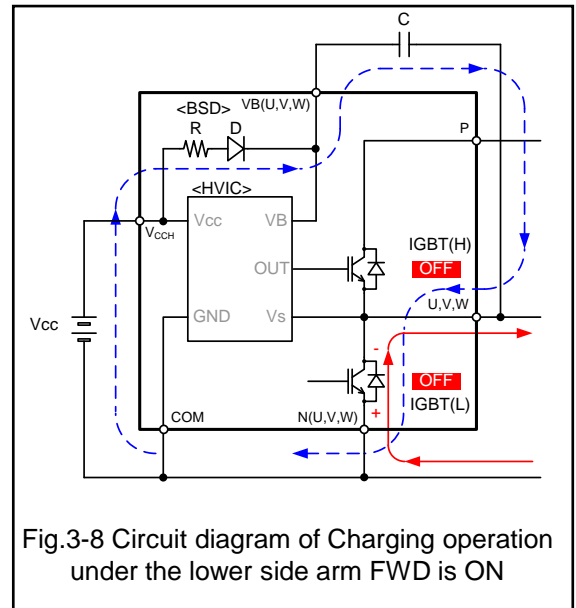


Fig.3-8 Circuit diagram of Charging operation under the lower side arm FWD is ON

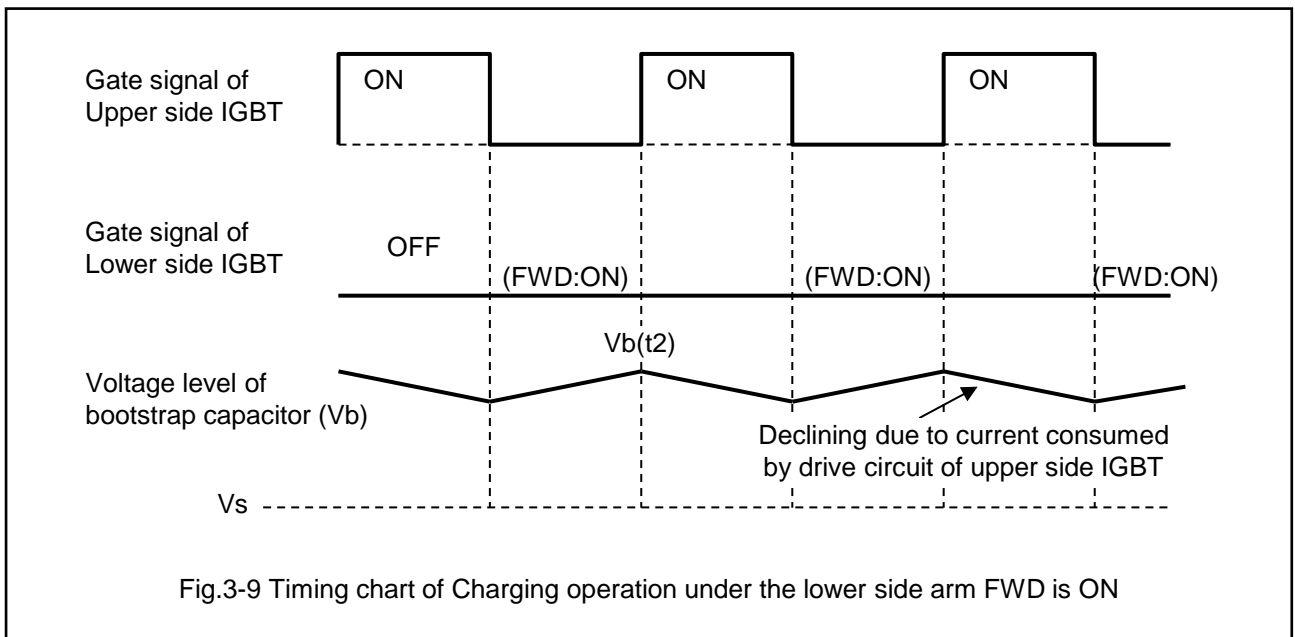


Fig.3-9 Timing chart of Charging operation under the lower side arm FWD is ON

2) Setting the bootstrap capacitance and minimum ON/OFF pulse width

The parameter of bootstrap capacitor can be calculated by the following equation:

$$C = I_b \cdot \frac{t_1}{dV}$$

- \* t1 : the maximum ON pulse width of the upper side IGBT
- \* I<sub>b</sub> : the drive current of the HVIC (depends on temperature and frequency characteristics)
- \* dV: the allowable discharge voltage. (see Fig.3-10)

A certain margin should be added to the calculated capacitance.

The bootstrap capacitance is generally selected as large as 2~3 times of the calculated value.

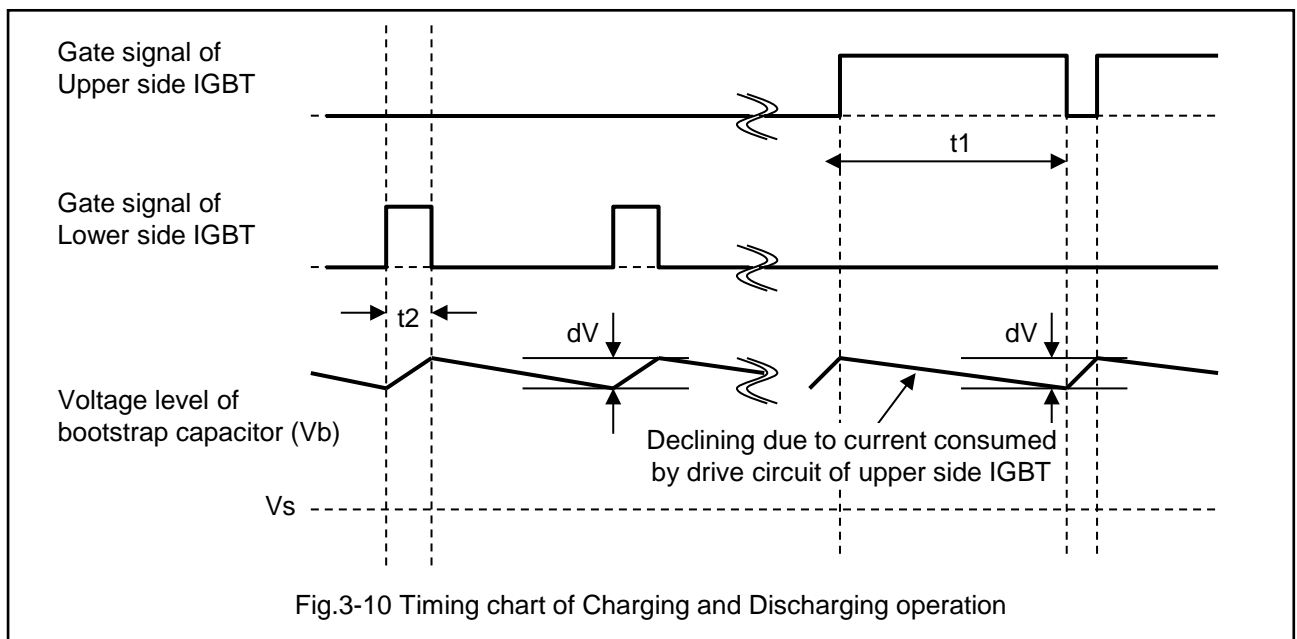
The recommended minimum ON pulse width (t2) of the lower side IGBT should be basically determined such that the time constant C·R will enable the discharged voltage (V) to be fully charged again during the ON period.

However, if only upper side IGBT has an ON-OFF-ON control mode (Sequence Fig.3-10), the time constant should be set so that the consumed energy during the ON period can be charged during the OFF period.

The minimum pulse width is decided by the minimum ON pulse width of the lower side IGBT or the minimum OFF pulse width of the upper side IGBT, whichever is shorter.

$$t_2 \geq \frac{R \cdot C \cdot dV}{V_{CC} - V_{b(\min)}}$$

- \* R : Series resistance of Bootstrap diode ΔRF(BSD)
- \* C : Bootstrap capacitance
- \* dV: the allowable discharge voltage.
- \*V<sub>CC</sub> : Voltage of HVICs and LVIC power supply (ex.15V)
- \*V<sub>b(min)</sub> : the minimum voltage of the upper side IGBT drive (Added margin to UV. ex. 14V)



3) Setting the bootstrap capacitance for Initial charging

The initial charge of the bootstrap capacitor is required to start-up the inverter.

The pulse width or pulse number should be large enough to make a full charge of the bootstrap capacitor.

For reference, the charging time of 10μF capacitor through the internal bootstrap diode is about 2ms.

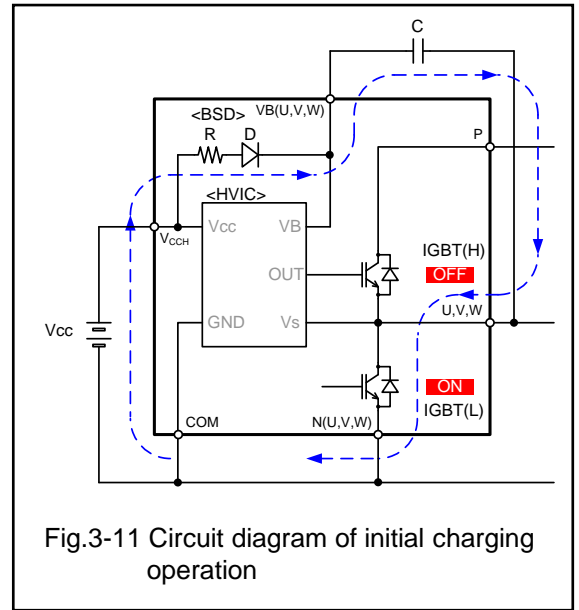


Fig.3-11 Circuit diagram of initial charging operation

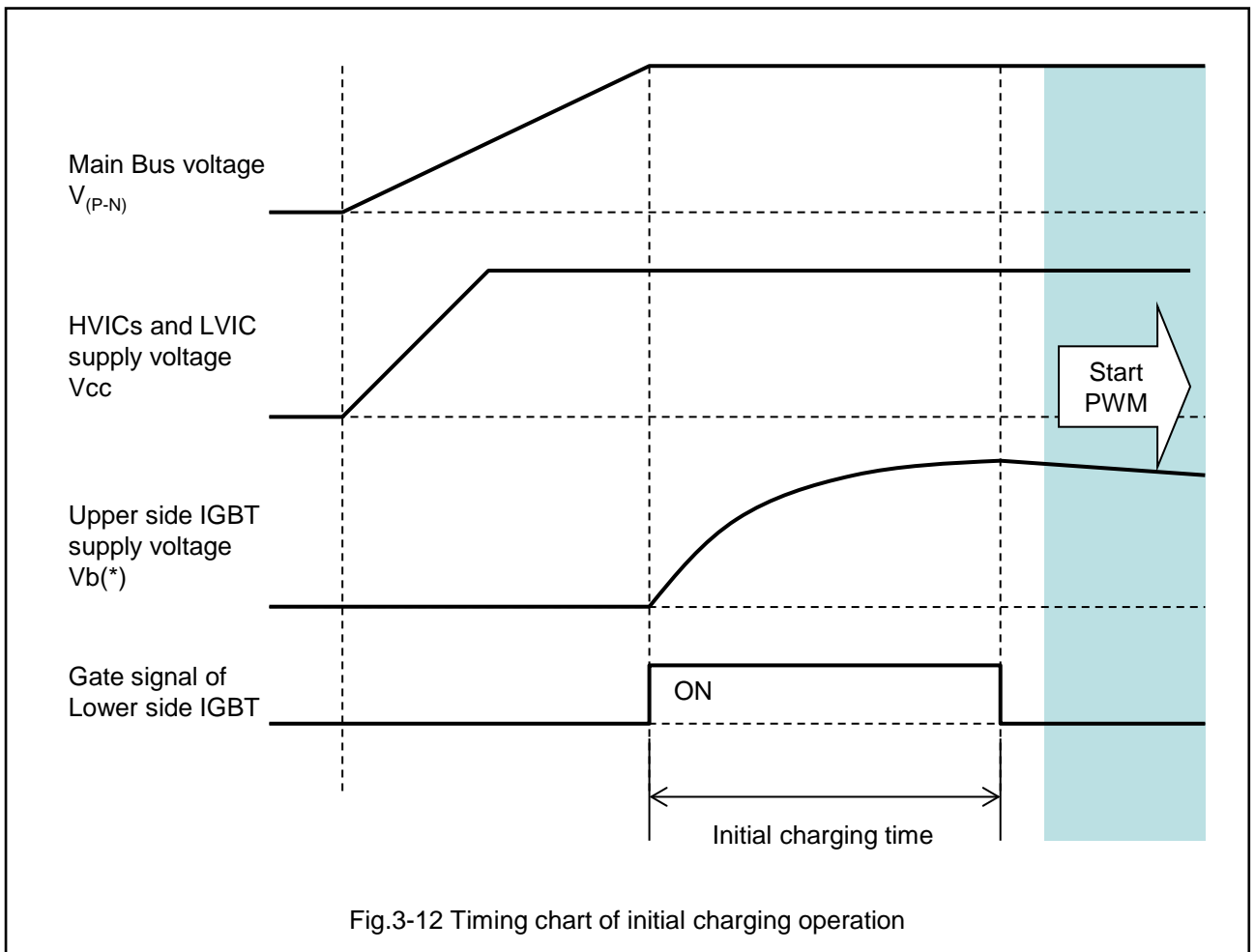


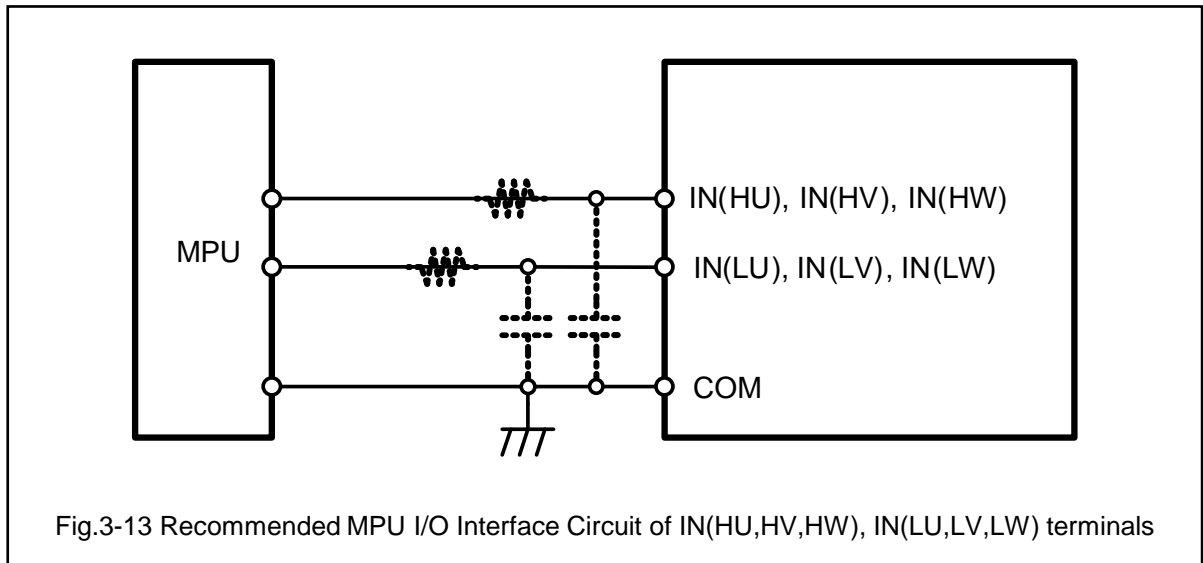
Fig.3-12 Timing chart of initial charging operation

## 4. Input Terminals IN(HU,HV,HW), IN(LU,LV,LW)

### 1. Input terminals Connection

Fig.3-13 shows the input interface circuit between the MPU and the IPM. It is possible that the input terminals connect directly to the MPU. It should not need the external pull up and down resistors connected to the input terminals, input logic is active high and the pull down resistors are built in.

The RC coupling at each input (parts shown dotted in Fig.3-13) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's PCB layout.



2. Input terminal circuit

The input logic of this IPM is active high. This logic has removed the sequence restriction between the control supply and the input signal during startup or shutdown operation. Therefore it makes the system failsafe. In addition, the pull down resistors are built in to each input terminals in Fig.3-14. Thus, external pull-down resistors are not needed reducing the required external component. Furthermore, a direct connection to 3.3V-class MPU by the low input signal threshold voltage.

As shown in Fig.3-14, the input circuit integrates a pull-down resistor. Therefore, when using an external filtering resistor between the MPU output and input of the IPM, please care to the signal voltage drop at the input terminals to satisfy the turn-on threshold voltage requirement. For instance,  $R=100\Omega$  and  $C=1000pF$  for the parts shown dotted in Fig.3-13.

Fig.3-14 shows that the internal diodes are electrically connected to the  $V_{CC}$ , IN(HU, HV, HW, LU, LV, LW) and COM terminals. They should not be used for the voltage clamp intentionally to prevent major problems and destroy the IPM.

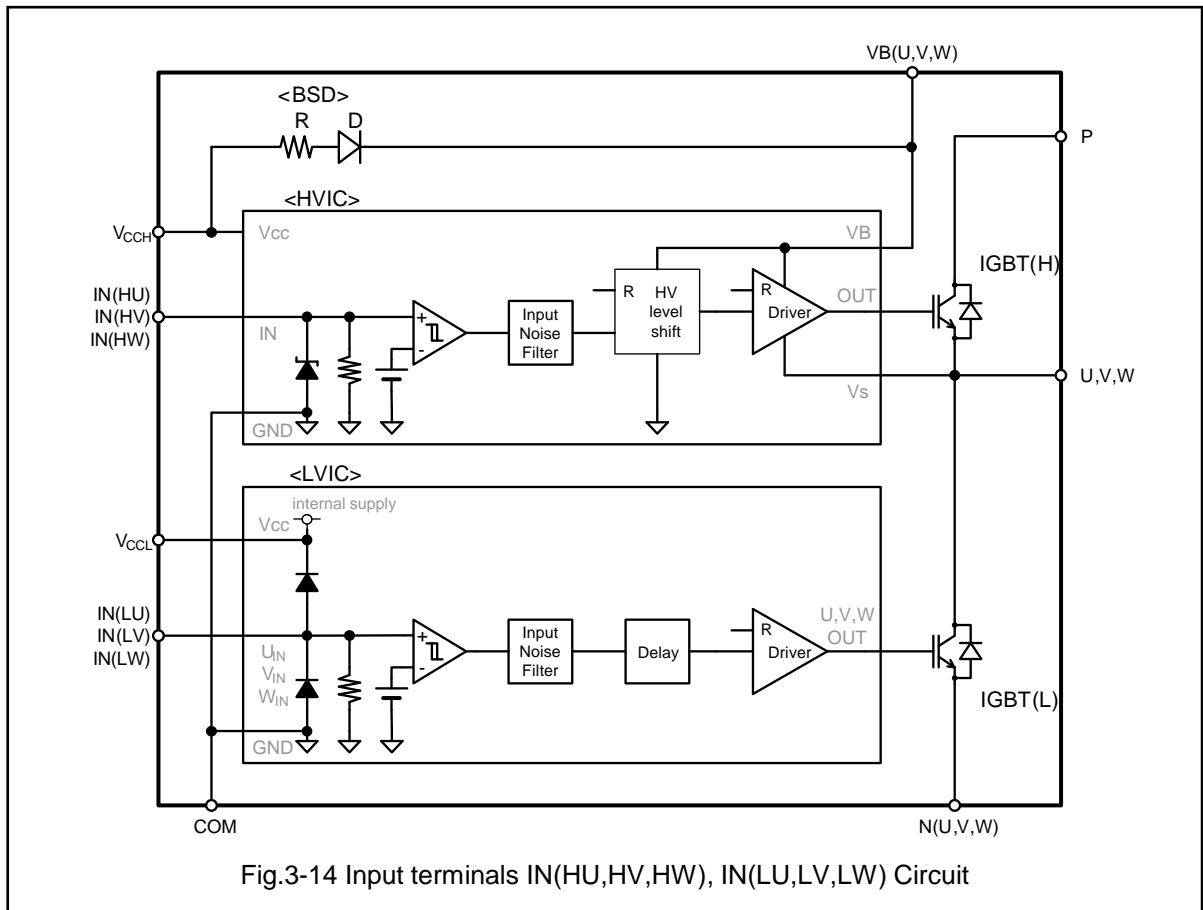


Fig.3-14 Input terminals IN(HU,HV,HW), IN(LU,LV,LW) Circuit

3. IGBT drive state versus Control signal pulse width

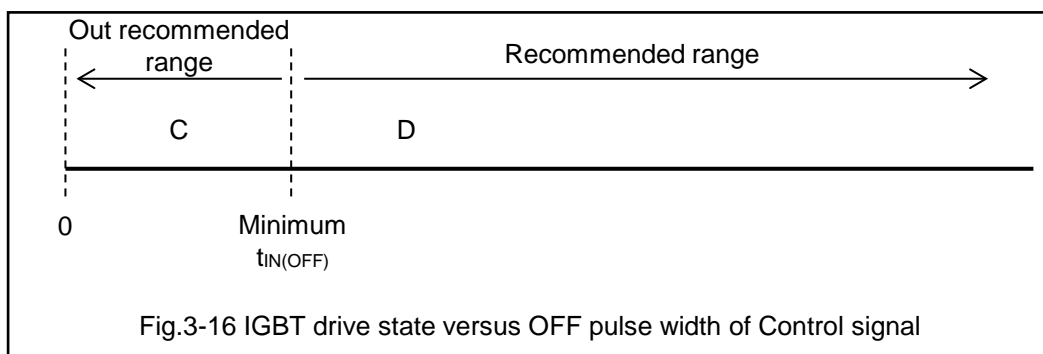
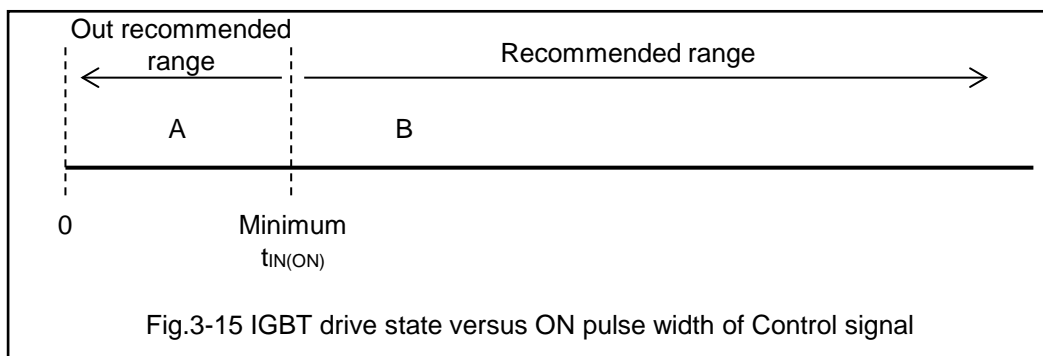
$t_{IN(ON)}$  is a recommended minimum turn-on pulse width for changing the IGBT state from OFF to ON, and  $t_{IN(OFF)}$  is a recommended minimum turn-off pulse width for changing the IGBT state from ON to OFF. Fig.3-15 and Fig.3-16 show IGBT drive state for various control signal pulse width.

state A : IGBT may turn on occasionally, even when the ON pulse width of control signal is less than minimum  $t_{IN(ON)}$ . Also if the ON pulse width of control signal is less than minimum  $t_{IN(ON)}$  and voltage is applied below -5V between U-COM,V-COM,W-COM , it may not turn off by the malfunction of the control circuit.

state B : IGBT can turn on and is saturated under normal condition.

state C : IGBT may turn on occasionally, even when the ON pulse width of control signal is less than minimum  $t_{IN(OFF)}$ . Also if the OFF pulse width of control signal is less than minimum  $t_{IN(OFF)}$  and voltage is applied below -5V between U-COM, V-COM, W-COM , it may not turn on by the malfunction of the control circuit.

state D : IGBT can turn fully off under normal condition.





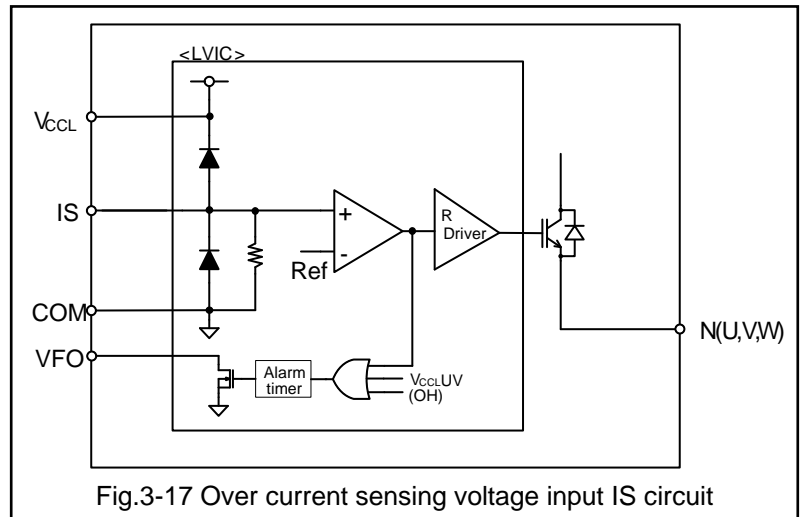
## 5. Over Current Protection Input Terminal IS

Over current protection (OC) is a function of detecting the IS voltage determined with the external shunt resistor, connected to N(\*)<sup>\*1</sup> and COM.

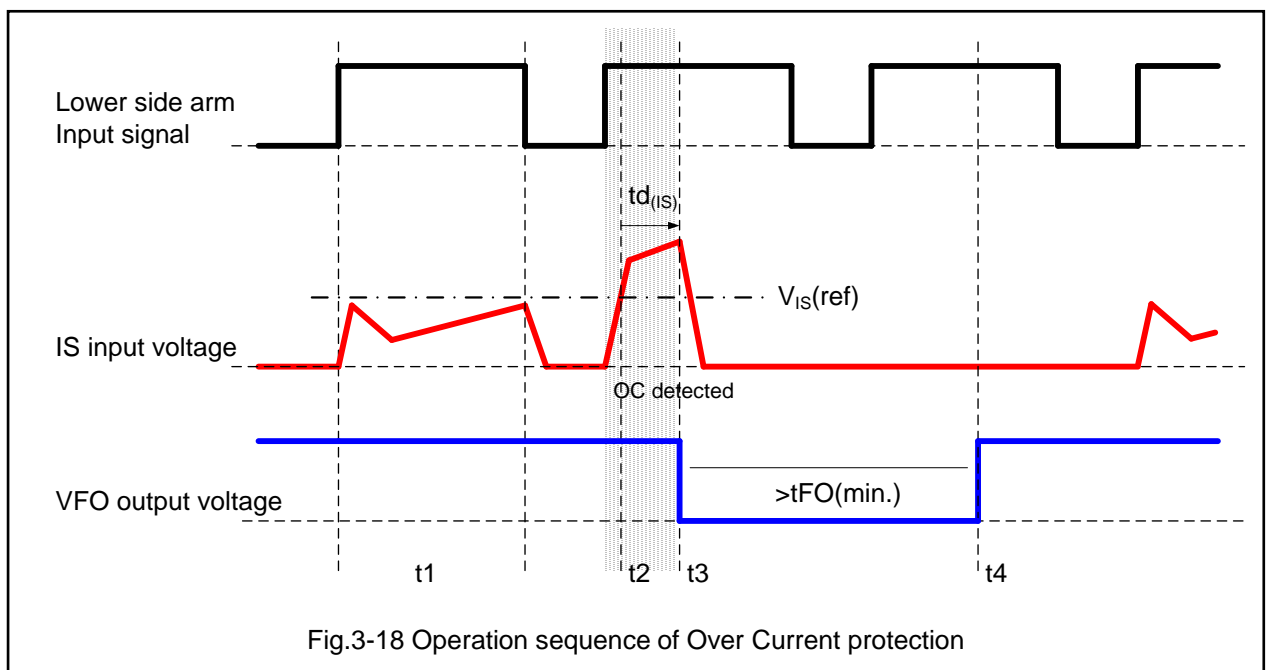
Fig.3-17 shows the over current sensing voltage input IS circuit block, and Fig.3-18 shows the OC operation sequence.

To prevent the IPM erroneous from the normal switching noise or recovery current, it is necessary to set an external R-C filter (time constant is approximately 1.5μs) to the IS terminal. Also the IPM and the shunt resistor should be wired as short as possible.

Fig.3-17 shows that the diodes in the IPM are electrically connected to the V<sub>CCL</sub>, IS and COM terminals. They should not be used for the voltage clamp intentionally to prevent major problems and destroy the IPM.



\*1 N(\*) : N(U), N(V), N(W)



- t1 : IS input voltage does not exceed  $V_{IS(ref)}$ , while the collector current of the lower side IGBT is under the normal operation.
- t2 : When IS input voltage exceeds  $V_{IS(ref)}$ , the OC is detected.
- t3 : The fault output VFO is activated and all lower side IGBT shut down simultaneously after the over current protection delay time  $t_{d(IS)}$ . Inherently there is dead time of LVIC in  $t_{d(IS)}$ .
- t4 : After the fault output pulse width  $t_{FO}$ , the OC is reset. Then next input signal is activated.

## 6. Fault Status Output Terminal VFO

As shown in Fig.3-19, it is possible that the fault status output VFO terminal connects directly to the MPU. VFO terminal is open drain configured, thus this terminal should be pulled up by a resistor of approximate 10kΩ to the positive side of the 5V or 3.3V external logic power supply, which is the same as the input signals. It is also recommended that the by-pass capacitors C1 should be connected at the MPU, and the inrush current limitation resistance R1, which is more than 5kΩ, should be connected between the MPU and the VFO terminal. These signal lines should be wired as short as possible to each device.

Fault status output VFO function is activated by the UV of V<sub>CCL</sub>, OC and OH.  
(OH is applied to “6MBP15VSH060-50”, “6MBP20VSC060-50” and “6MBP30VSC060-50”.)

Fig.3-19 shows that the diodes in the IPM are electrically connected to the V<sub>CCL</sub>, VFO and COM terminals. They should not be used for the voltage clamp intentionally to prevent major problems and destroy the IPM.

Fig.3-20 shows the Voltage-current characteristics of VFO terminal at fault state condition. The IFO is the sink current of the VFO terminal as shown in Fig.3-19.

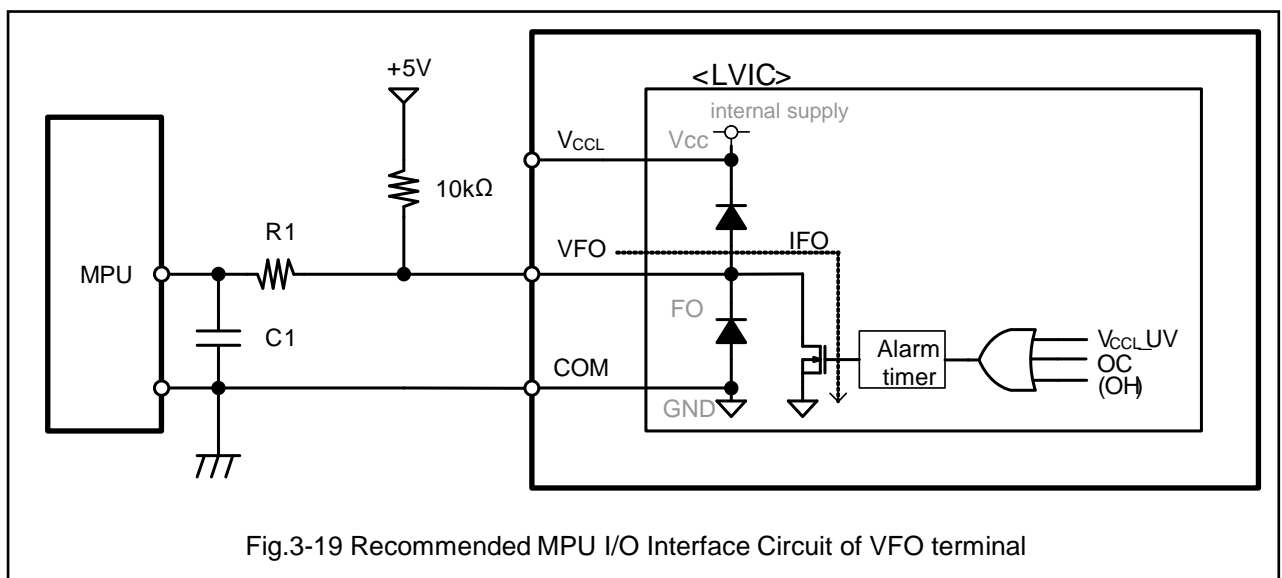


Fig.3-19 Recommended MPU I/O Interface Circuit of VFO terminal

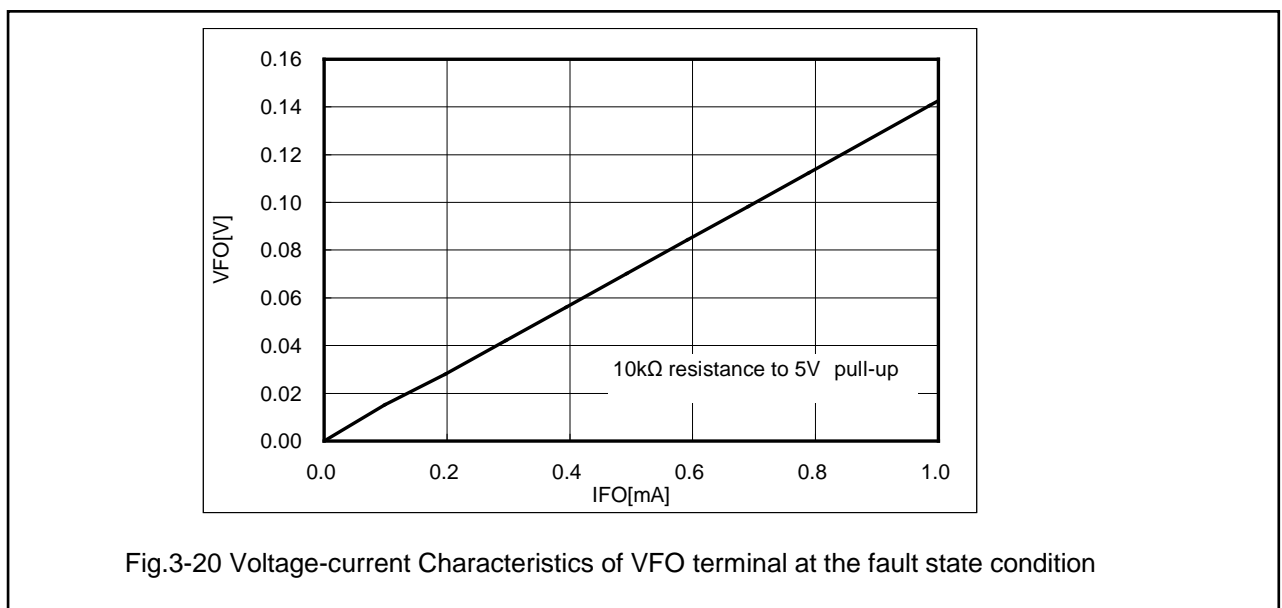


Fig.3-20 Voltage-current Characteristics of VFO terminal at the fault state condition

## 7. Temperature Sensor Output Terminal TEMP

As shown in Fig. 3-21, the temperature sensor output TEMP can be connected to MPU directly.

It is recommended that a by-pass capacitor and >10kΩ of inrush current limiting resistor are connected between the TEMP terminal and the MPU. These signal lines should be wired as short as possible to each device.

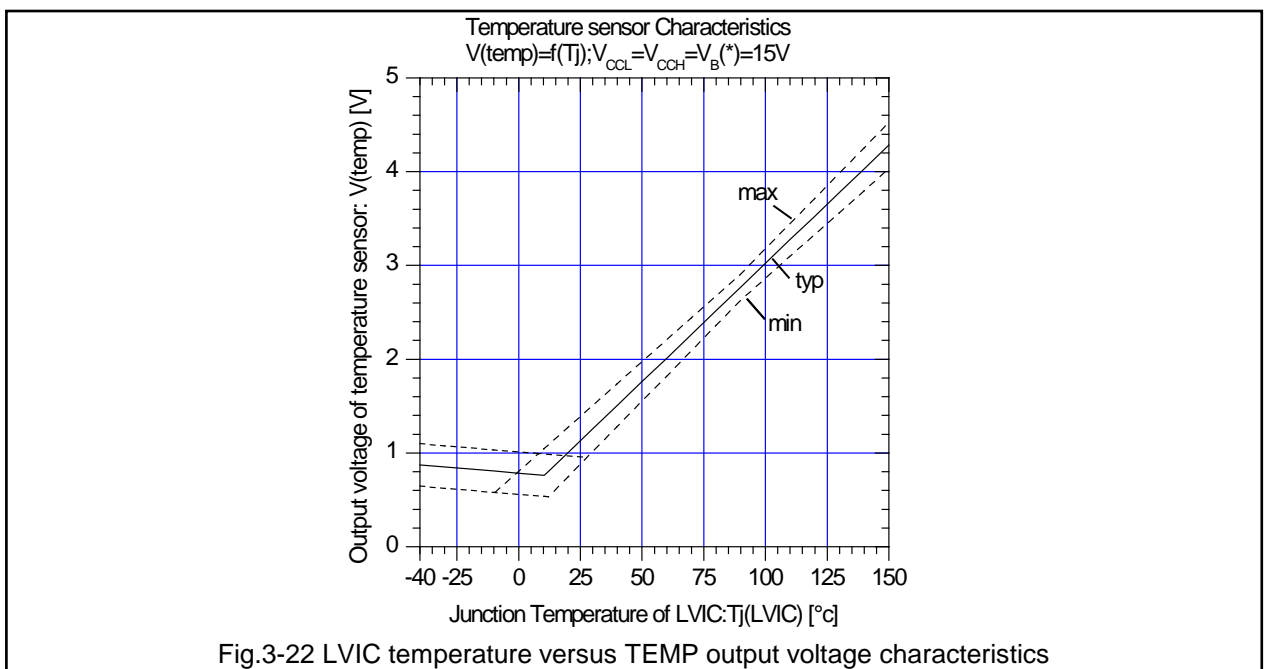
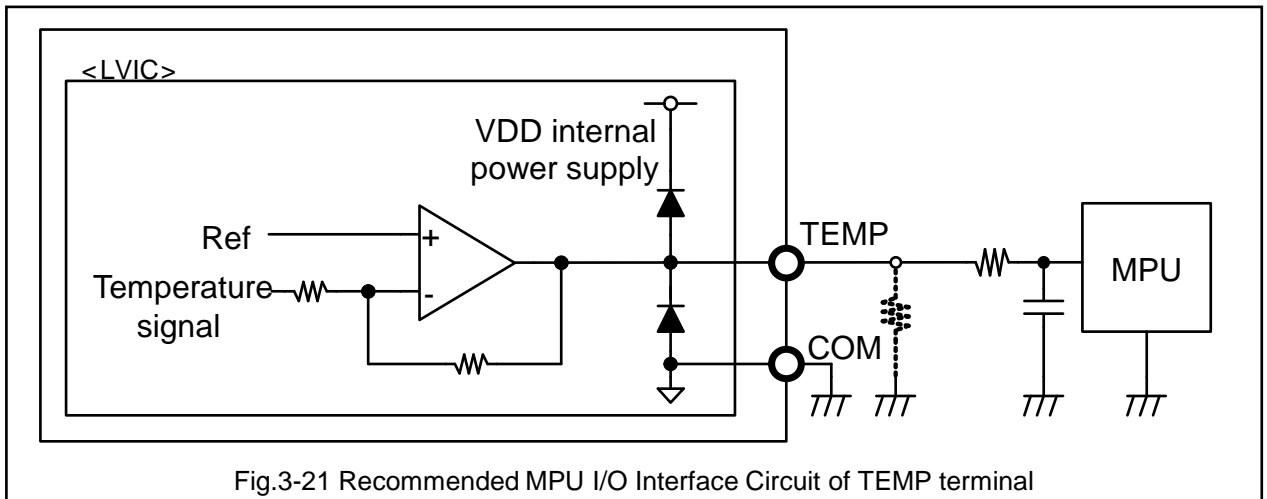
The IPM has a built-in temperature sensor, and it can output an analog voltage according to the LVIC temperature. This function doesn't protect the IPM, and there is no fault signal output.

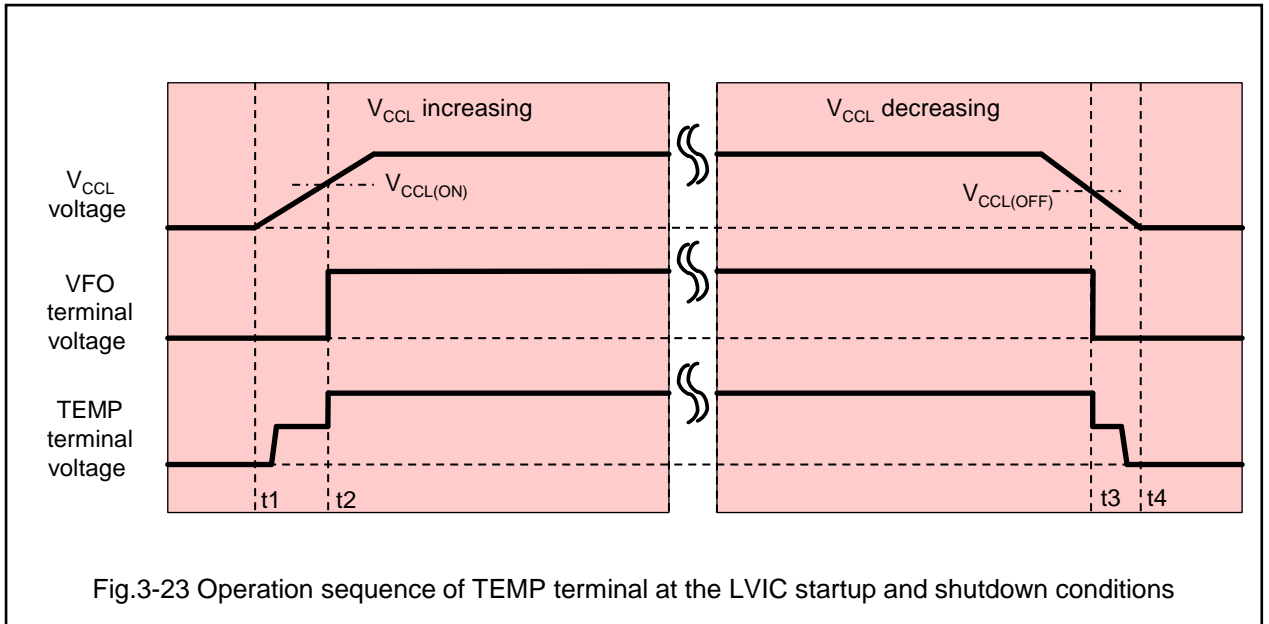
"6MBP15VSH060-50", "6MBP20VSC060-50" and "6MBP30VSC060-50" have a built-in over-heating protection. If the temperature exceeds TOH, these IPMs output a fault signal by the over-heating protection function.

A diode is electrically connected between TEMP and COM terminal as shown in Fig. 3-12. The purpose of the diode is a protection of the IPM from an input surge voltage. Don't use the diode as a voltage clamp circuit because the IPM might be damaged.

Fig.3-22 shows the LVIC temperature versus TEMP output voltage characteristics. It should be connected the TEMP terminal to a zener diode for the voltage clamp when the power supply of MPU is 3.3V.

Fig.3-23 shows the operation sequence of TEMP terminal at the LVIC startup and shutdown conditions.





- t1-t2 : TEMP function is activated when  $V_{CCL}$  exceeds  $V_{CCL(ON)}$ . If  $V_{CCL}$  is less than  $V_{CCL(ON)}$ , the TEMP terminal voltage is the same as the clamp voltage.
- t2-t3 : TEMP terminal voltage rises to the voltage determined with LVIC temperature. In case the temperature is clamping operation, the TEMP terminal voltage is the same as the clamp voltage even though  $V_{CCL}$  is less than  $V_{CCL(ON)}$ .
- t3-t4 : TEMP function is reset when  $V_{CCL}$  falls below  $V_{CCL(OFF)}$ . TEMP terminal voltage becomes shutdown and the TEMP terminal voltage is the same as the clamp voltage.

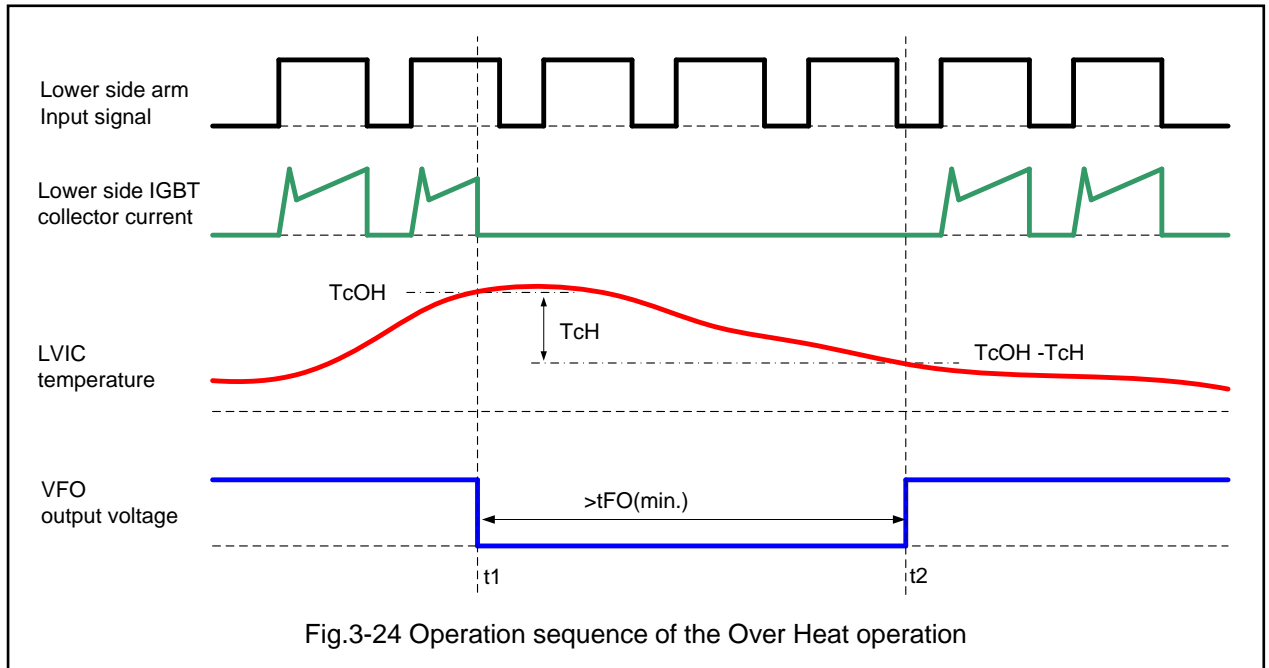
## 8. Over Heating Protection

The over-heating protection (OH) functions is integrated into “6MBP15VSH060-50”, “6MBP20VSC060-50” and “6MBP30VSC060-50”.

The OH function monitors the LVIC junction temperature.

The TOH sensor position is shown in Fig.2-2.

As shown in Fig.3-24, the IPM shutdown all lower side IGBTs while the LVIC temperature exceeds TOH. The fault status is reset when the LVIC temperature drops below (TOH-TOH(hys)).



- t1 : The fault status is activated and all IGBTs of the lower side arm shutdown, when LVIC temperature exceeds case overheating protection (OH) temperature TOH.
- t2 : The fault status, which outputs over  $t_{FO}$ , is reset and next input signal is activated, when LVIC temperature falls below TOH – TOH(hys) which is the case overheating protection hysteresis.

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## Chapter 4

# Power Terminals

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Contents	Page
1. Connection of Bus Input terminal and Low Side Emitters.....	4-2
2. Setting of Shunt Resister of Over Current Protection .....	4-3

# 1. Connection of bus input terminal and low side emitters

In this chapter, the guideline and precautions in circuit design on the power terminals, such as how to determine the resistance of shunt resistor are explained.

## (1) Description of the power terminals

Table 4-1 shows the detail about the power terminals.

Table 4-1 Detail description of power terminals

Terminal Name	Description
P	Positive bus voltage input It is internally connected to the collector of the high-side IGBTs. In order to suppress the surge voltage caused by the wiring or PCB pattern inductance of the bus voltage, connect a snubber capacitor close to this pin. (Typically metal film capacitors are used)
U,V,W	Motor output terminal Inverter output terminals for connecting to motor load.
N(U),N(V),N(W)	Negative bus voltage input terminals These terminals are connected to the low-side IGBT emitter of the each phase. In order to observe the current on each phase, shunt resistors are inserted between these terminals and the negative bus voltage input (power ground).

## (2) Recommended wiring of shunt resistor and snubber capacitor

External current sensing resistors are applied to detect OC (over current) condition or phase currents. A long wiring patterns between the shunt resistor and the IPM will cause excessive surge that might damage internal IC, and current detection components. To decrease the pattern inductance, the wiring between the shunt resistors and the IPM should be as short as possible.

As shown in the Fig.4-1, snubber capacitors should be installed in the right location so as to suppress surge voltage effectively. Generally a 0.1 ~ 0.22  $\mu$ F snubber is recommended. If the snubber capacitor is installed in wrong location "A" as shown in the Fig.4-1, the snubber capacitor can not suppress the surge voltage effectively because inductance of wiring is not negligible.

If the capacitor is installed in the location "B", the charging and discharging currents generated by wiring and the snubber capacitor will appear on the shunt resistor. This will impact the current sensing signal and the OC protection level will be lower than the calculated design value. Although the suppression effect when the snubber capacitor is installed in location "B" is greater than the location "A" or "C", the location "C" is a reasonable position considering the impact to the current sensing accuracy. Therefore, the location "C" is generally used.

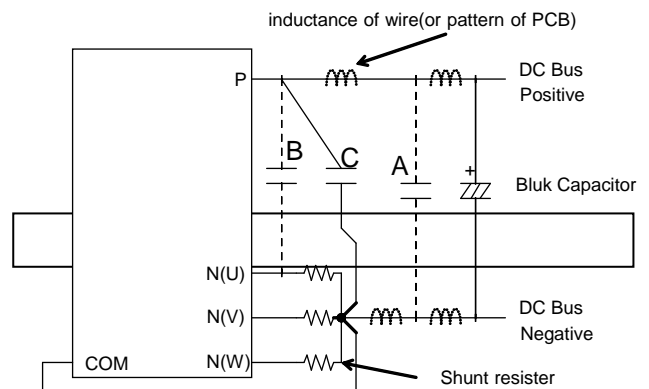


Fig.4-1 Recommended wiring of shunt resistor and snubber capacitor

## 2. Setting of Shunt Resistor of Over Current Protection

### (1) Selecting current sensing shunt resistor

The value of current sensing resistor is calculated by the following equation:

$$R_{Sh} = \frac{V_{IS(ref)}}{I_{OC}} \quad (4.1)$$

Where  $V_{IS(ref)}$  is the Over current protection (OC) reference voltage level of the IPM and  $I_{OC}$  is the current of OC detection level.  $V_{IS(ref)}$  is 0.43V(min.), 0.48V(typ.) and 0.53V(max.). And  $R_{Sh}$  is the Resistance of the shunt resistor.

The maximum value of OC level should be set lower than the repetitive peak collector current in the spec sheet of this IPM considering the tolerance of shunt resistor.

For example, if OC level is set 30A, the recommended value of the shunt resistor is calculated as:

$$R_{Sh(min)} = \frac{V_{IS(ref)(max)}}{I_{OC}} = \frac{0.53}{60} = 8.8 [\text{m}\Omega] \quad (4.2)$$

Where  $R_{Sh(min)}$  is the minimum resistance of the shunt resistor.

Based on above expressions, minimum shunt resistance of shunt resistor is introduced.

It's note that a proper resistance should be chosen and confirmed considering OC level required in the practical application.

### (2) Filter delay time setting of over current protection

An external RC filter is necessary in the over current sensing circuit to prevent malfunction of OC caused by noise. The RC time constant is determined depending on the applying time of noise and the short circuit withstand capability of IGBTs. It is recommended to be set approximately 1.5 $\mu$ s.

When the voltage of the shunt resistor exceeds the OC level, the filter delay time ( $t_{delay}$ ) that the input voltage of IS terminal rises to the OC level is caused by RC filter delay time constant and it is given by:

$$t_{(delay)} = -\tau \cdot \ln\left(1 - \frac{V_{IS(ref)(max)}}{R_{Sh} \cdot I_P}\right) \quad (4.3)$$

Where  $\tau$  is the RC time constant,  $I_P$  is the peak current flowing through the shunt resistor.

In addition, there is the shutdown propagation delay  $t_{d(IS)}$  of OC.

Therefore, the total time  $t_{total}$  from OC triggered to shutdown of the IGBT becomes:

$$t_{total} = t_{delay} + t_{d(IS)} \quad (4.4)$$

The total delay time  $t_{total}$  must be considered the short circuit withstand capability of IGBT.

Please confirm a proper delay time in the actual equipment.



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## Chapter 5

# Recommended wiring and layout

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Contents	Page
1. Examples of Application Circuits.....	5-2
2. Recommendation and Precautions in PCB design.....	5-5

# 1. Examples of Application Circuits

In this chapter, a recommended wiring and layout are explained  
At first, hints and cautions in design are described with example of application circuit in section 1.

Fig. 5-1 and Fig.5-2 show examples of application circuit, and its Notes.  
In these figure, although two method of current sense are shown, these Notes are common.

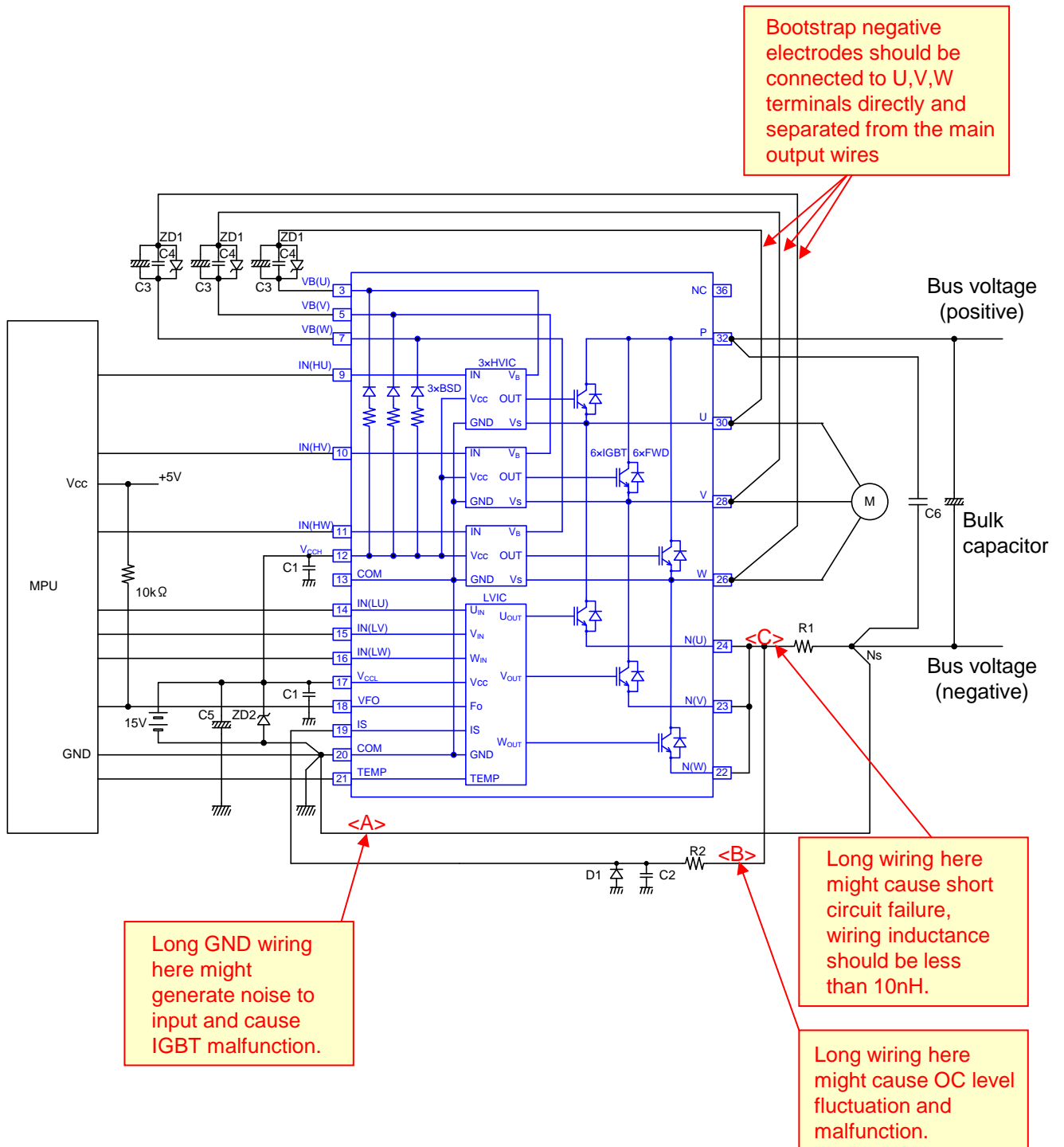


Fig. 5-1 Example of application circuit  
(Sensing currents at once with 1 shunt resistor)

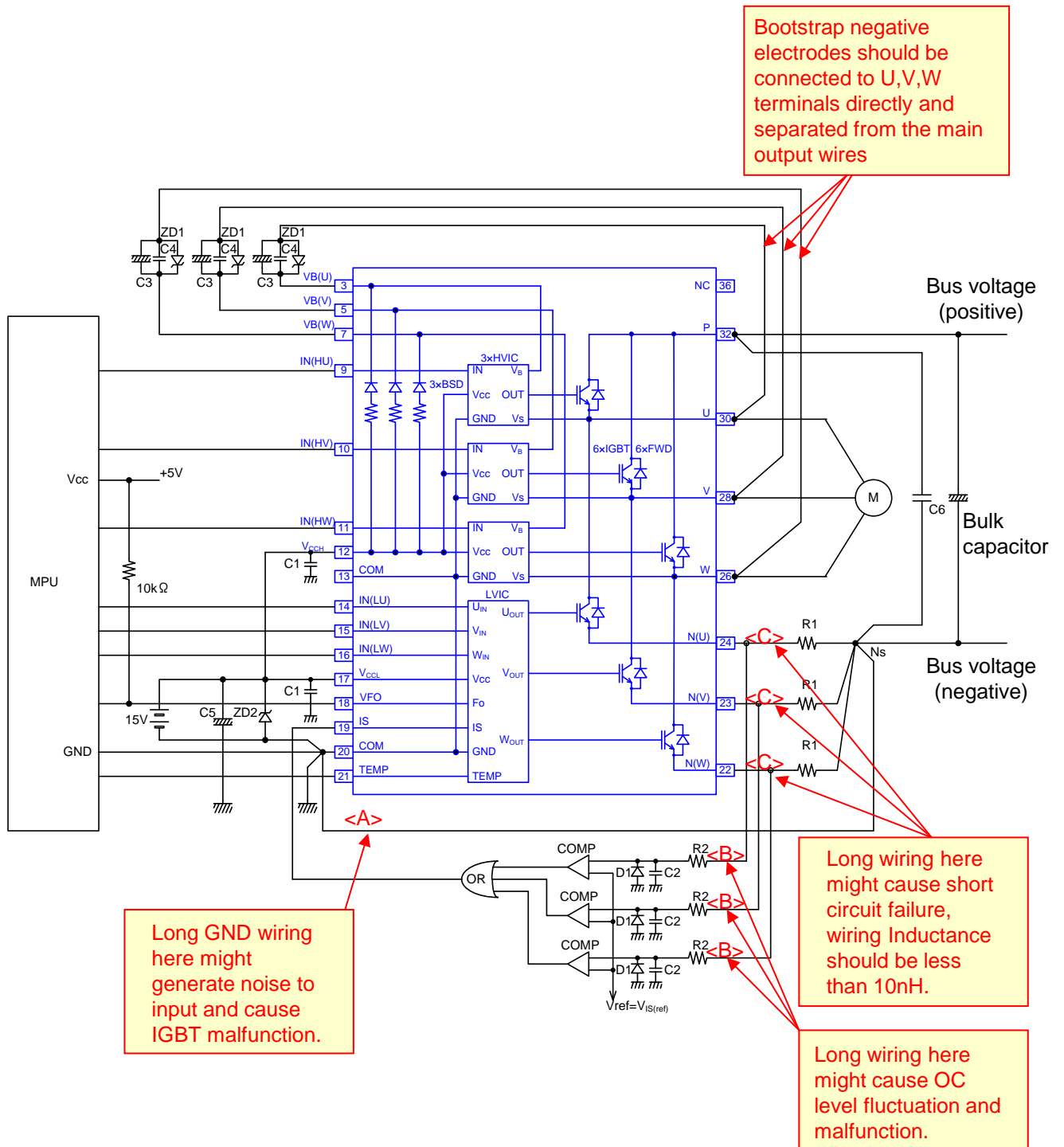


Fig. 5-2 Another example of application circuit  
(Sensing currents of each phase using external protection circuit)

<Note>

1. Input signal for IGBT driving is High-Active. The input circuit of the IC has a built-in pull-down resistor. To prevent a malfunction, the wiring of each input should be as short as possible. When using R-C coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
2. The IPM has a built-in HVIC and it is possible to be connected to a microprocessor (MPU) directly without any photo-coupler or pulse-transformer isolation.
3. VFO output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10k $\Omega$ .
4. To prevent erroneous protection, the wiring of (A), (B), (C) should be as short as possible.
5. The time constant R2-C2 of the protection circuit should be selected approximately 1.5 $\mu$ s. Over current (OC) shutdown time might vary due to the wiring pattern. Tight tolerance, temp-compensated type is recommended for R2, C2.
6. Please recommended to set the threshold voltage of the comparator reference input to be same as the IPM OC trip reference voltage  $V_{IS(ref)}$ .
7. Please use high speed type comparator and logic IC to detect OC condition quickly.
8. If negative voltage is applied to R1 during the switching operation, a schottky barrier diode D1 is recommended to be connected.
9. All capacitors should be connected as close to the terminals of the IPM as possible. (C1, C4 : narrow temperature drift, higher frequency and DC bias characteristic ceramic type are recommended, and C3, C5: narrow temperature drift, higher frequency and electrolytic type.)
10. To prevent surge destruction, the wiring between the snubber capacitor and the P terminal, Ns node should be as short as possible. Generally 0.1 $\mu$  to 0.22 $\mu$ F snubber capacitor (C6) between the P terminal and Ns node is recommended.
11. Two COM terminals (9 & 16 pin) are electrically connected inside the IPM, it must be connected either one to the signal GND outside and leave another one open.
12. It is recommended to insert a zener-diode (22V) between each pair of control supply terminals to prevent surge destruction.
13. If signal GND is connected to power GND by broad pattern, it may cause a malfunction by power GND fluctuation. It is recommended to connect signal GND and power GND at one point.

## 2. Recommendation and Precautions in PCB design

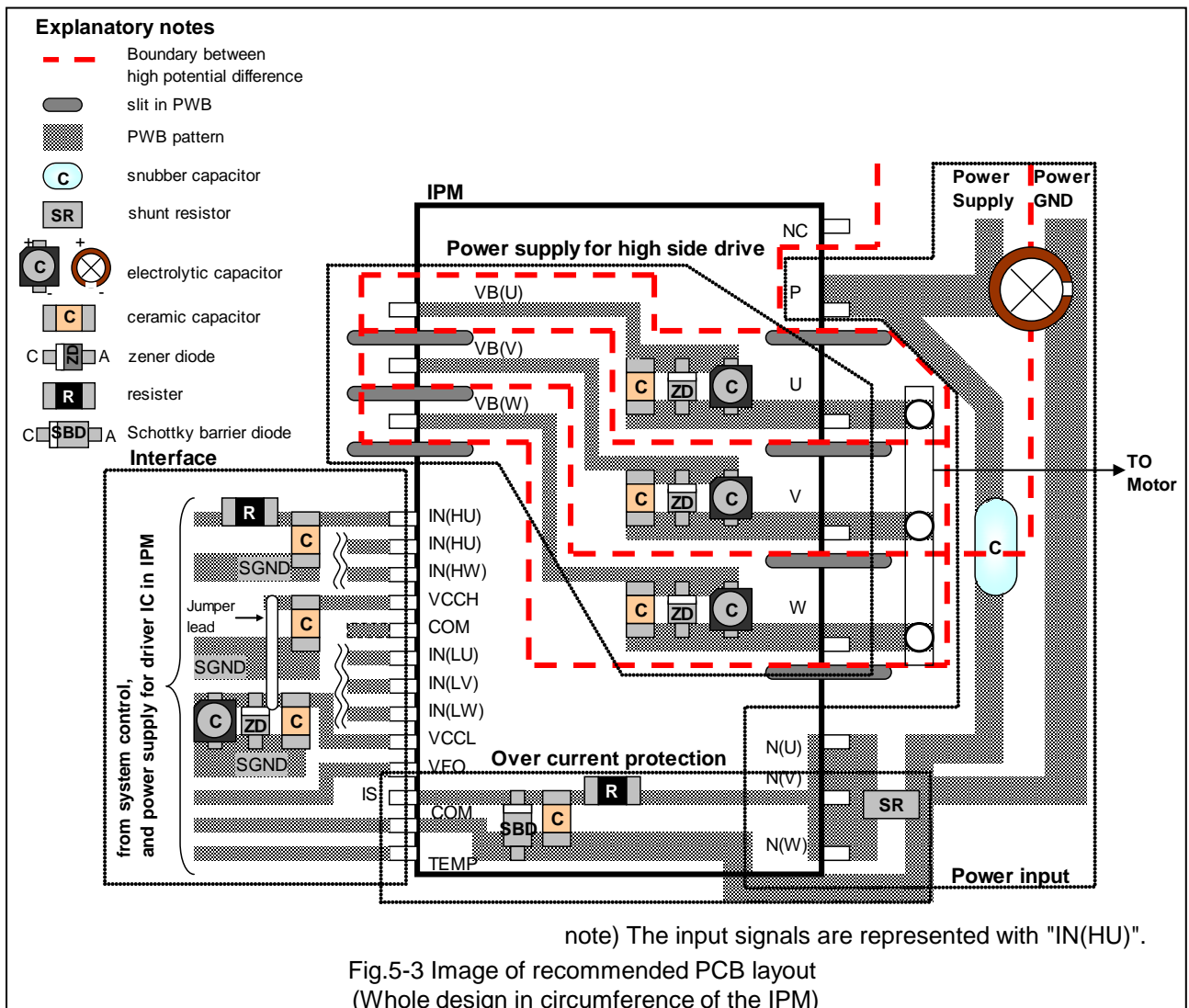
In this section, the recommended pattern layout and precautions in PCB design are described. Fig.5-3 to Fig.5-7 show the image of recommended PCB layout, referring Fig.5-1 and Fig.5-2. In these Fig., the input signals from system control are represented with "IN(HU)".

The recommendation and precautions are as follows,

(1) Whole design in circumference of the IPM

- (A) Keep a relevant creepage distance at the boundary.  
(Place a slit between there if needed.)
- (B) The pattern of the power input (DC bus voltage) part and the power supply for high side drive part should be separated each other to prevent increasing the conduction noise. Please care to stray capacitance and insulating performance of PCB if these patterns cross using multi layer PCB.
- (C) The pattern of the power supply for high side drive part and the interface circuit part should be separated each other to avoid a malfunction of system. It is strongly recommended to lay out without crossing each other using multi layer PCB.

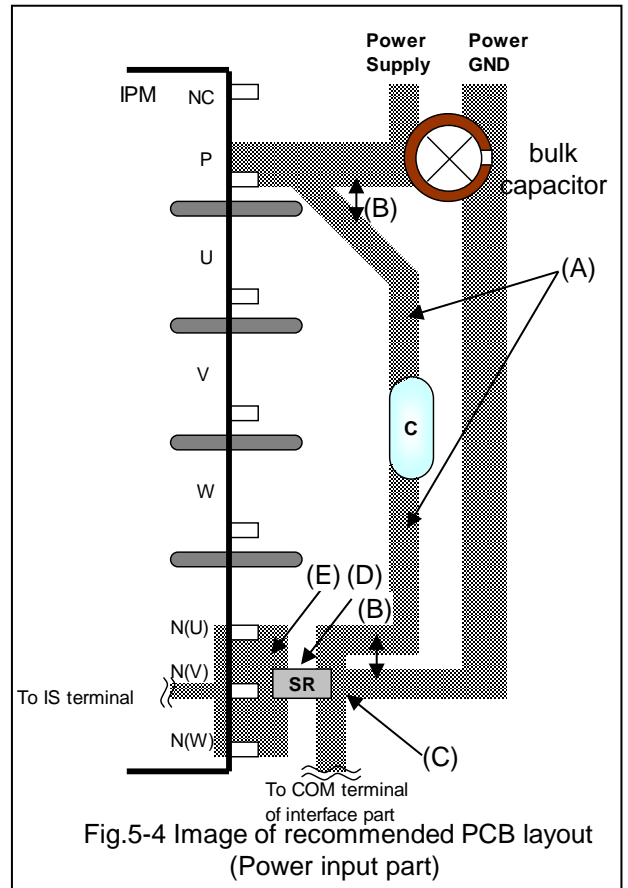
More detail in each part are described in next page.



## 2. Recommendation and Precautions in PCB design

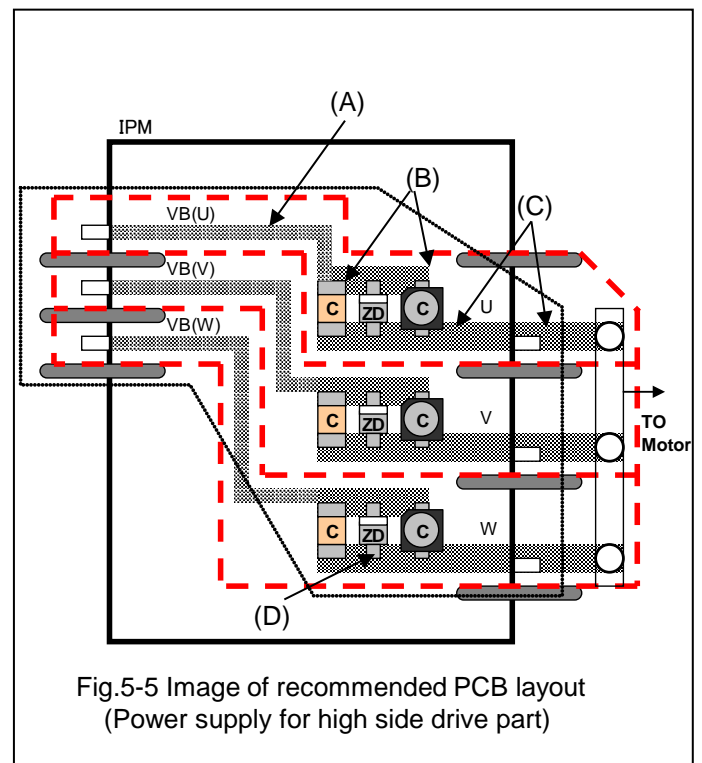
### (2) Power input part

- (A) Locate the snubber capacitor between P terminal and the negative node of the shunt resistor as close as possible. The pattern between the snubber capacitor and P terminal and shunt resistor should be short as possible to avoid the influence of the pattern inductance.
- (B) Pattern from the bulk capacitor and pattern of the snubber capacitor should be separated each other near the P terminal and close the shunt resistor.
- (C) The pattern of Power GND and the pattern from COM terminal should be connected shortly the shunt resistor with single-point-grounding.
- (D) The shunt resistor should be chosen low-inductance type.
- (E) The pattern between N(U),N(V),N(W) terminals and the shunt resistor should be as short as possible.



### (3) Power supply for high side drive part.

- (A) The pattern length from VB(U,V,W) and the components (ceramic capacitor, electrolytic capacitor and zener diode) of its nodes should be as short as possible to avoid the influence of the pattern inductance.
- (B) Please use a relevant capacitance by the applications. And especially, please place the ceramic capacitor or low-ESR capacitor closely to the VB(U,V,W) terminals.
- (C) The pattern to Motor output and the pattern to negative pole of the capacitor for VB(U,V,W) should be separated each other close the U,V and W terminals to avoid a malfunction by common impedance of these patterns.
- (D) If the stray capacitance between VB(U) and Power GND (or equal potential) is large, the voltage between VB(U) and U might be over or under voltage when IGBT turns on and off with high  $dV/dt$ . Therefore, placing the zener diode between VB(U) and U are recommended. And it should be placed close VB(U) terminal.  
(VB(V), VB(W) are also same as VB(U).)

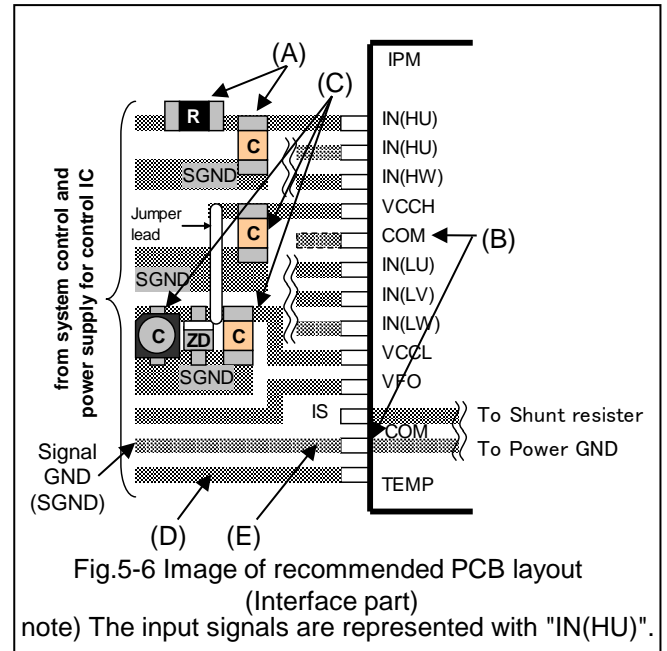


(4) Interface part

- (A) Inserting the capacitor between the input signal and COM pattern are recommended if the influence of noise from the power supply for high side drive part (and so forth) can't be negligible. And the negative pole of the capacitor should be connected to the pattern of signal GND near the terminal of COM as possible.

If the series resistor or the capacitor are inserted, please consider the internal pull down resistors in this IPM and please confirm signal quality in actual system.

- (B) The IPM has two COM terminals. These two terminals are connected inside, so must be used either one.
- (C) Electrolytic capacitor and ceramic capacitor should be connected between  $V_{CCCL}$  and COM patterns,  $V_{CCH}$  and COM patterns. These should be as close to each terminal as possible.
- (D) The signal from TEMP terminal should be located parallel with Signal GND to suppress noise influence.
- (E) The pattern of signal GND from system control and the pattern from COM terminal should be connected together at one point ground. The one point ground should be as close to the COM terminal as possible.



(5) Over Current Protection part

Like Fig.5-1 and Fig. 5-2, to detect and protect the OC condition, 2 methods of current-sense are shown by example. One is "One-shunt type" (Fig.5-7 (a)) and the other is "3-shunt type" (Fig.5-7 (b)).

In Fig.5-7 (a)

- (A) The pattern between negative pole of the shunt resistor and the COM terminal is very important. It plays a role of not only the reference zero level of internal control IC, but also the pass of bootstrap charging current of high side and the pass of gate driving current of low side IGBTs. So, to make the influence of common impedance of them minimum, this pattern should be as short as possible.
- (B) The pattern of IS signal should be as short as possible to avoid OC level fluctuation and malfunction.
- (C) Inserting the RC filter between the IS signal is needed to prevent the miss detection of OC at the timing of switching. And the negative pole of this capacitor should be connected to the pattern of signal GND near the terminal of COM.
- (D) If a negative voltage at the switching timing is applying to IS terminal, the schottky barrier diode should be inserted between IS terminal and COM terminal or parallel to the shunt resistor .

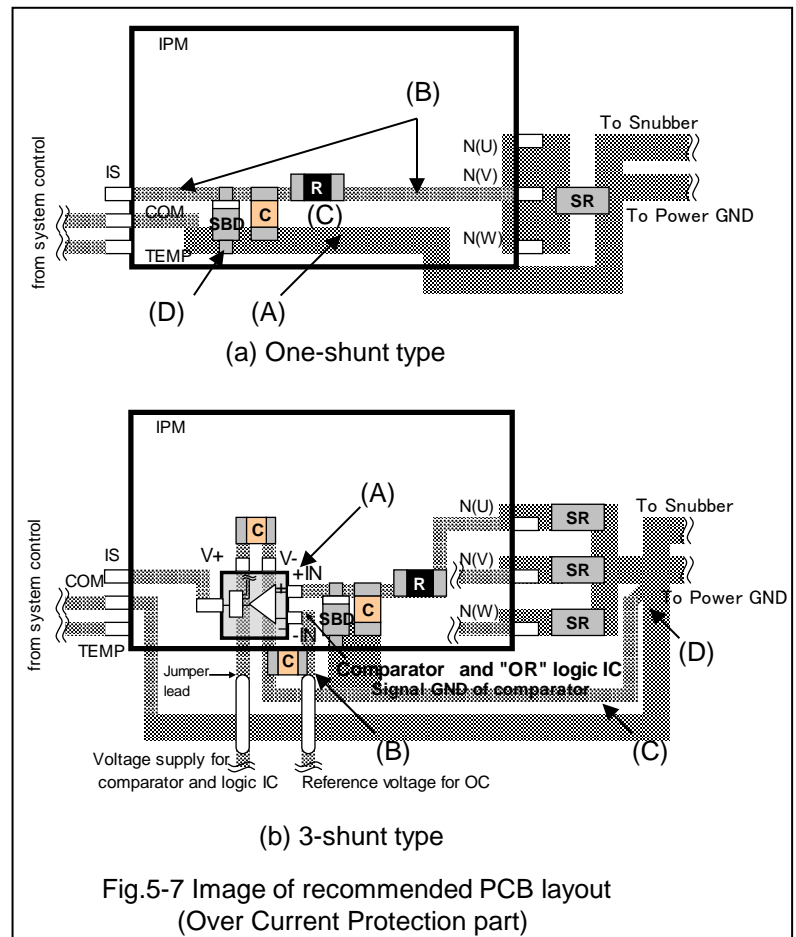


Fig.5-7 Image of recommended PCB layout  
(Over Current Protection part)

In Fig.5-7 (b)

- (A) Please use high speed type comparator and logic IC to detect OC condition quickly.
- (B) The reference voltage level of OC which is inputted to the comparator should be coupled by capacitor to signal GND. And it should be as close to comparator as possible.
- (C) The pattern of signal GND for COM terminal and the pattern of signal GND for the comparator should be separated each other.
- (D) The pattern of signal GND from COM and the pattern of signal GND of the comparator should be connected together at one point ground. The one point ground should be as close to the negative pole of the shunt resistors.
- (E) The other precautions and recommendations are same as Fig.5-7 (a).

For more detail of determination circuit parameters please refer to Chapter 4 section 2.



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## Chapter 6

# Mounting Guideline and Thermal Design

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Contents	Page
1. Soldering to PCB .....	6-2
2. Mounting to Heat sink .....	6-3
3. Cooler (Heat Sink) Selection.....	6-4

# 1. Soldering to PCB

## **Soldering**

- (1) The device temperature during soldering is possible to exceed the maximum storage temperature. To avoid device damage and to ensure reliability, the following guidelines are recommended from the quality assurance standard.

Table 6.1 Soldering temperature and duration

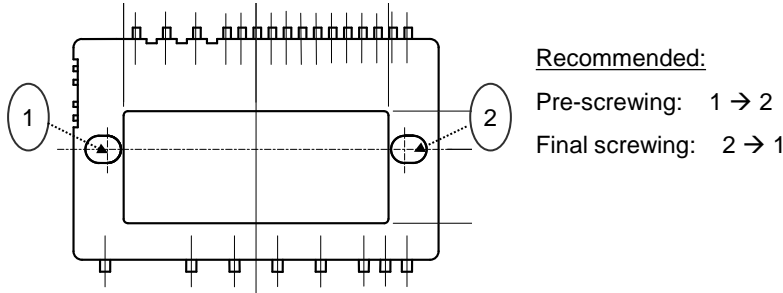
	Methods	Soldering Temp. & Time	Note
a	Solder dipping / Soldering iron	260±5°C, 10±1sec	
b	Solder dipping / Soldering iron	350±10°C, 3.5±0.5sec	

- (2) The immersion depth of the lead terminal should keep the distance 1.5mm apart from the device. When using flow-soldering, be careful to avoid immersing the package in the solder bath.
- (3) We do not recommend to re-use the device once after solder is removed and detached from the board. The detached device from PCB might be damaged by thermal or mechanical stress when the solder is removed.

## 2. Mounting to heat sink

### Mounting procedure and precautions

When mounting the IPM to a heat sink, please refer to the following recommended procedure of fastening conditions. One side screwing with excessive torque might cause a destruction and degradation of the chip.



**Note:** the pre-screwing torque is set to 30% of the maximum torque rating.

Fig.6-1 Recommended screw fastening procedure

Fig.6-2 shows the measurement position of heat sink flatness.

The heat sink flatness should be from 0 $\mu$ m/100mm to +100 $\mu$ m/100mm, and the surface roughness (Rz) should be less than 10 $\mu$ m.

If the heat sink surface is concave, a gap occurs between the heat sink and the IPM, leading to deterioration of cooling efficiency.

If the flatness is +100  $\mu$ m or more, the aluminum base of the IPM is deformed and cracks could occur in the internal isolating substrates.

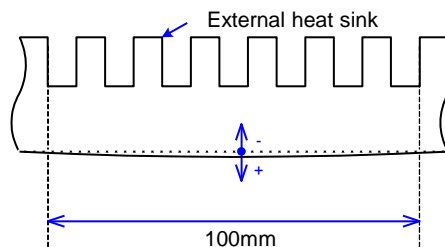


Fig.6-2 The measurement point of heat sink flatness

In order to obtain effective heat dissipation, thermal compound with good thermal conductivity should be applied uniformly with +50 $\mu$ m thickness on the contacting surface between the IPM and heat sink. Refer to the following information for an application position and application quantity.

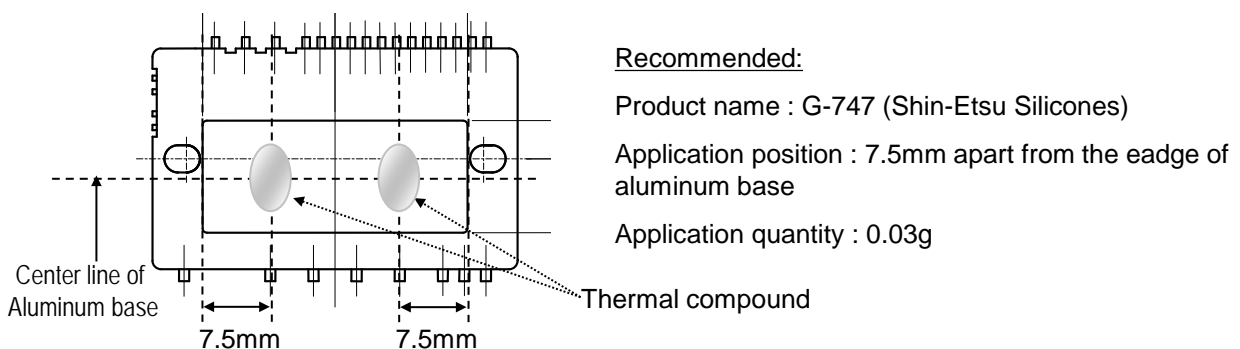


Fig.6-3 Recommended an application position and application quantity.

### 3. Cooler (Heat Sink) Selection Method

- Please make sure that the junction temperature  $T_j$  should not exceed  $T_{jmax}$  for safe operation. Cooling device (heat sink) should be designed to ensure that  $T_j$  is always below  $T_{jmax}$  even in abnormal conditions such as overload operation as well as under the rated load.
- If the IGBT junction temperature is higher than  $T_{jmax}$ , it might cause a damage to the chips. The  $T_{jOH}$  protection function works if the junction temperature exceeds  $T_{jmax}$ . However, if the temperature rises too quickly, the  $T_{jOH}$  protection may not work.
- Please note that the junction temperature of FWD should not exceed  $T_{jmax}$  also.
- When selecting a cooling device (heat sink), please measure the temperature directly as shown in Fig.2-2.

For more detail about thermal design, please refer Chapter 6 Section 2 of this note and “IGBT MODULE APPLICATION MANUAL REH984b”

Contents:

- Power dissipation loss calculation
- Selecting heat sinks
- Heat sink mounting precautions
- Troubleshooting

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## Chapter 7

# Cautions

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Contents	Page
1. Other warnings and precautions .....	7-2
2. Notice .....	7-3

## Other warnings and precautions

### **Warnings in operating and handling**

- (1) This IPM should be used in products within their absolute maximum rating (voltage, current, temperature, etc.). This IPM may be broken if used beyond the rating.
- (2) The equipment containing this IPM should have adequate fuses or circuit breakers to prevent the equipment from causing secondary destruction (ex. fire, explosion etc...).
- (3) Use this IPM within their reliability and lifetime under certain environments or conditions. This IPM may fail before the target lifetime of your products if used under certain reliability conditions.
- (4) Be careful when handling this IPM for ESD damage. (It is an important consideration.)
- (5) When handling the IPM, hold them by the case (package) and don't touch the leads and terminals.
- (6) It is recommended that any handling of the IPM is done on grounded electrically conductive floor and tablemats.
- (7) Before touching the IPM, Discharge any static electricity from your body and clothes by grounding out through a high impedance resistor (about 1M $\Omega$ )
- (8) When soldering, in order to protect the IPM from static electricity, ground the soldering iron or soldering bath through a low impedance resistor.
- (9) Consider the possible temperature rise not only for the junction and case, but also for the outer leads.
- (10) Do not directly touch the leads or package of the IPM while power is supplied or during operation in order to avoid electric shock and burns.
- (11) The IPM is made of incombustible material. However, if the IPM fails, it may emit smoke or flame.
- (12) When operating the IPM near any flammable place or material may cause the IPM to emit smoke or flame in case the IPM become even hotter during operation. Design the arrangement to prevent the spread of fire.
- (13) The IPM should not used in an environment in the presence of acid, organic matter, or corrosive gas (hydrogen sulfide, sulfurous acid gas etc.)
- (14) The IPM should not used in an irradiated environment since they are not radiation-proof.
- (15) During open short test, the internal of the IPM might explode instantaneously and the resin mold package might be blown off when high voltage is applied to the low voltage terminals. Make sure in your design that during open short test, high voltage will not be applied to the low terminals. To avoid accidents and explosion damage if high voltage is applied, use fuses in your design.

### **Precautions in storage**

- (1) The IPM must be stored at a standard temperature of 5 to 35°C and relative humidity of 45 to 75%. If the storage area is very dry, a humidifier may be required. In such a case, use only deionized water or boiled water, since the chlorine in tap water may corrode the leads.
- (2) The IPM should not be subjected to rapid changes in temperature to avoid condensation on the surface of the IPM. Therefore store the IPM in a place where the temperature is steady.
- (3) The IPM should not be stored on top of each other, since this may cause excessive external force on the case.
- (4) The IPM should be stored with the lead terminals remaining unprocessed. Rust may cause presoldered connections to fail during later processing.
- (5) The IPM should be stored in antistatic containers or shipping bags.
- (6) Under the above storage condition, use the IPM within one year.

## NOTICE

- (1) The contents will subject to change without notice due to product specification change or some other reasons. In case of using the products stated in this document, the latest product specification shall be provided and the data shall be checked.
- (2) The application examples in this note show the typical examples of using Fuji products and this note shall neither assure to enforce the industrial property including some other rights nor grant the license.
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- (4) The product introduced in this Application note is intended for use in the following electronic and electrical equipment which requires ordinary reliability:
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  - Inverter for Compressor motor for heat pump applications.
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  - Trunk communications equipment
  - Gas leakage detectors with an auto-shutoff function
  - Safety devices, etc.
  - Traffic-signal control equipment
  - Disaster prevention / security equipment
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  - Airborne equipment
  - Atomic control equipment
  - Submarine repeater equipment
  - Medical equipment
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