Chapter 4

Detail of Power Terminals

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1. Connection of Bus Input terminal and Low Side Emitters

In this chapter, the guideline and precautions in circuit design on the Power terminals, such as how to determine the resistance of shunt resister are explained.

(1) Description of the Power terminals

Table 4-1 shows the detail description about Power terminals.
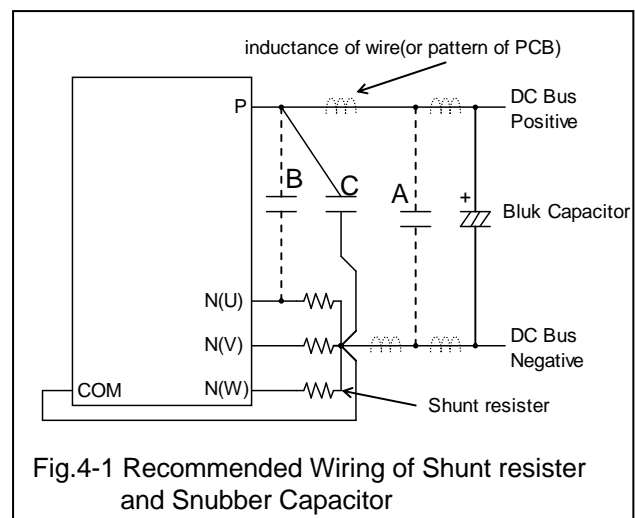
Table 4-1 Detail description of Power terminals

Terminal Name	Description
P	Positive bus voltage input It is internally connected to the collector of the high-side IGBTs. In order to suppress the surge voltage caused by the wiring or PCB pattern inductance of the bus voltage, connect a snubber capacitor close to this pin. (Typically metal film capacitors are used)
U,V,W	Motor output terminal Inverter output terminals for connecting to the motor load.
N(U),N(V),N(W)	Negative bus voltage input terminals These terminals are connected to the low-side IGBT emitter of the each phase. In order to observe the current of the each phase, the shunt resisters are inserted between these terminals and negative bus voltage input (power ground).

(2) Recommended wiring of shunt resister and snubber capacitor

External current sensing resisters are applied to detect OC (over current) condition or phase currents. A long wiring patterns between the shunt resister and the IPM will cause excessive surge that might damage internal IC, and current detection components. To decrease the pattern inductance, the wiring between the shunt resisters and the IPM should be as short as possible.

As shown in the Fig.4-1, snubber capacitors should be installed in the right location so as to suppress surge voltage effectively. Generally a 0.1 ~ 0.22 μF snubber is recommended. If the snubber capacitor is installed in wrong location "A" as shown in the Fig.4-1, the snubber capacitor can not suppress the surge voltage effectively because inductance of wiring is not negligible.

If the capacitor is installed in the location "B", the charging and discharging currents generated by wiring and the snubber capacitor will appear on the shunt resister. This will impact the current sensing signal and the OC protection level will be lower than the calculated design value. Although the suppression effect when the snubber capacitor is installed in location "B" is greater than the location "A" or "C", the location "C" is a reasonable position considering the impact to the current sensing accuracy. Therefore, the location "C" is generally used.

Fig.4-1 Recommended Wiring of Shunt resister and Snubber Capacitor

2. Setting of Shunt Resister of Over Current Protection

(1) Selecting current sensing shunt resistor

The value of current sensing resistor is calculated by the following expression:

$$R_{Sh} = \frac{V_{IS(ref)}}{I_{OC}} \tag{4.1}$$

Where $V_{IS(ref)}$ is the Over current protection (OC) reference voltage level of the IPM and I_{OC} is the current of OC detection level. $V_{IS(ref)}$ is 0.43V(min.), 0.48V(typ.) and 0.53V(max.). And R_{Sh} is the Resistance of the shunt resister.

The maximum value of OC level should be set lower than the repetitive peak collector current in the spec sheet of this IPM considering the tolerance of shunt resistor.

For example, if OC level is set 30A, the recommended value of the shunt resistor is calculated as:

$$R_{Sh(min)} = \frac{V_{IS(ref)(max)}}{I_{OC}} = \frac{0.53}{30} = 17.7 \, [\text{m}\Omega] \tag{4.2}$$

Where $R_{Sh(min)}$ is the minimum resistance of the shunt resister.

Based on above expressions, minimum shunt resistance of shunt resister is introduced.

It's note that a proper resistance should be chosen and confirmed considering OC level required in the practical application.

(2) Filter delay time Setting of Over Current Protection

An external RC filter is necessary in the over current sensing circuit to prevent malfunction of OC caused by noise. The RC time constant is determined depending on the applying time of noise and the short circuit withstand capability of IGBTs. It is recommended to be set approximately 1.5μs.

When the voltage of the shunt resistor exceeds the OC level, the filter delay time (t_{delay}) that the input voltage of IS terminal rises to the OC level is caused by RC filter delay time constant and it is given by:

$$t_{(delay)} = -\tau \cdot \ln(1 - \frac{V_{IS(ref)(max)}}{R_{Sh} \cdot I_P}) \tag{4.3}$$

Where τ is the RC time constant, I_P is the peak current flowing through the shunt resister.
In addition, there is the shutdown propagation delay $t_{d(IS)}$ of OC.
Therefore, the total time t_{total} from OC triggered to shutdown of the IGBT becomes:

$$t_{total} = t_{delay} + t_{d(IS)} \tag{4.4}$$

The total delay time must be set considering the short circuit withstand capability of IGBT.

It's note that a proper delay should be confirmed in the practical application.