# SiC Hybrid Module Application Note
# Chapter 2
# -  Precautions for Use  -

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1

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## 1 Maximum junction temperature

The maximum junction temperature $T_{j(max)}$ is 150°C for all modules of Fuji's 5th generation (U,U4 series). For the 6th generation (V series), it could be increased by 25°C to 175°C.

Taking account of the design margin the U and U4 series could be used at a continuous operating temperature $T_{j(op)}$ of around 125°C. Affected by the higher $T_{j(max)}$ for the V series Fuji can guarantee a continuous operation temperature of $T_{j(op)}$=150°C for the V series modules. This value is based on the verification tests conducted according to the JEITA standards.

The benefit of this increased $T_{j(op)}$ is usable for different aspects like downsizing of applicable module and heat sink, improvement of output current and carrier frequency and expansion of the applicable range of inverter.

On the other hand, after increasing the maximum operating temperature to 150°C, a continuous operation over this temperature may degrade the power cycle capability and will lead to a reduced product lifetime.

## 2  Short circuit (overcurrent) protection

If an IGBT is short-circuited, the voltage across the collector and the emitter (C–E) will increase rapidly. In the same time the collector current will increase. The collector current will be saturated to a specific value due to the self-saturation feature of the IGBT structure. But since the IGBT is in state of high voltage and high current the dissipated power will destroy the IGBT rapidly because of high thermal stress. This situation must be eliminated as quickly as possible.

Fig. 2-1 shows the correlation between the short circuit capability (guaranteed short-circuit withstand time) and the applied voltage at the time of short circuit occurrence for the SiC hybrid module 1700V. Regarding the short circuit detection time, refer to this graph as well as operating conditions of the certain application.
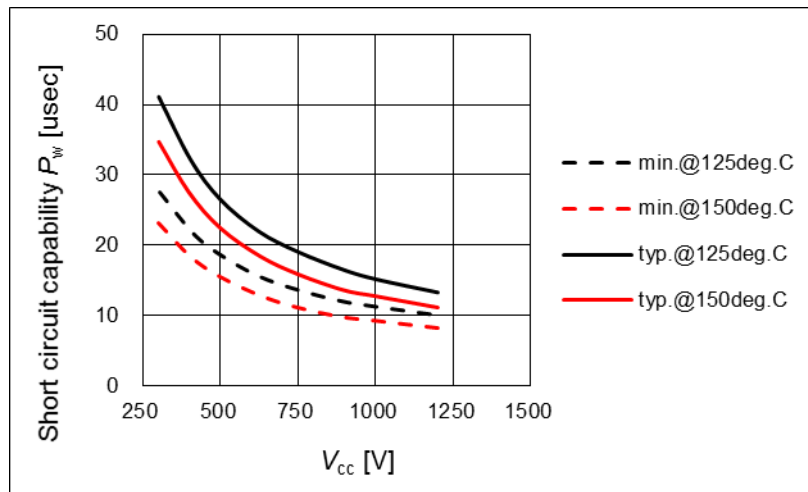


Fig.2-1    Relation between Short Circuit Capability and Applied Voltage when Short Circuit Occurs in 1700V SiC hybrid module

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## 3 Overvoltage protection

### 3.1 Overvoltage protection

Due to the high switching speed of the IGBT, high $di/dt$ is often observed when IGBT is turned off or at reverse recovery of FWD. This high $di/dt$ in combination with the wiring parasitic inductance of the main circuit leads to a surge voltage. If this surge voltage exceeds the maximum rated voltage, the IGBT is in an overvoltage state which might destroy the device in the worst case. To prevent the device failure, there are different common methods like implementation of a snubber circuit, adjustment of the gate resistance $R_G$ and reduction of the inductance of the main circuit.

To give an image of the correlation between the surge voltage and the factors of influence, an example of surge voltage characteristics for the SiC hybrid module 2MSI400VAE-170-53 is shown below.

Fig.3-1 shows an example of the dependency between the stray inductance ($L_s$) and the surge voltage at turn off. As shown in the graph, the surge voltage will be higher for a high stray inductance.

Fig.3-2 shows an example of the dependency between the collector voltage and the surge voltage at IGBT turn off. The surge voltage becomes higher when the collector voltage increases.

Fig.3-3 shows an example of the dependency between the collector current and the surge voltage at IGBT turn off. The surge voltage at IGBT turn off will be higher when the collector current is larger.

As shown above, the peak surge voltage generated in the IGBT module changes significantly. There are more dependencies than just the one to the main circuit inductance and the gate drive condition. Also circuit conditions like the type of snubber circuit and the values for the used parts, or the capacitor capacity will have an influence.

Therefore, it is recommended to make sure that the surge voltage is kept within RBSOA for all possible operating conditions of the respective devices such as inverter system that uses the module. If the surge voltage exceeds the specified RBSOA, it should be reduced by adjusting the gate resistance, reducing the stray inductance or adding a snubber or active clamp circuit.
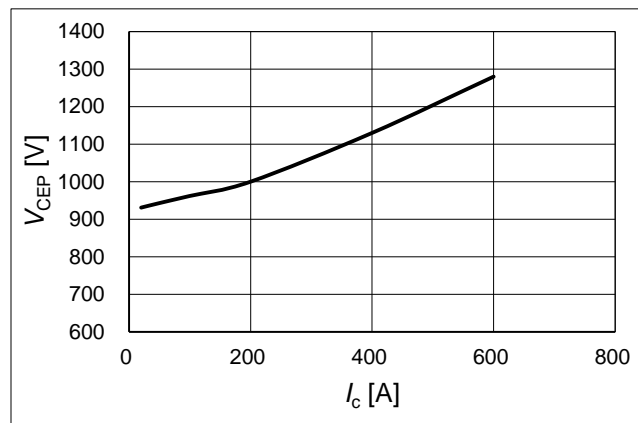
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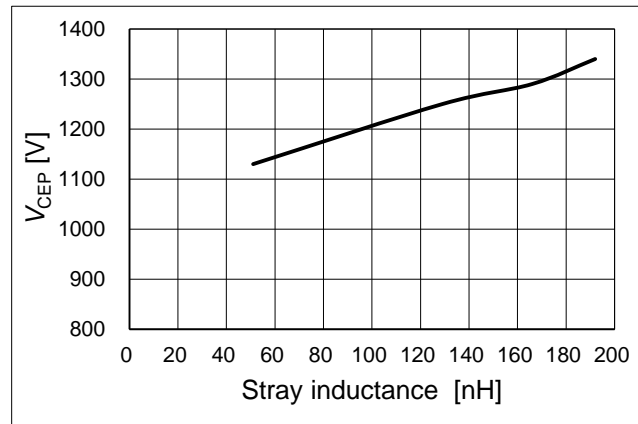
Condition : $V_{GE}=\pm15V$, $V_{CC}=900V$, $R_G=0.5\Omega$, $T_j=125°C$, $I_C=400A$

Fig.3-1　Example of Stray Inductance Dependence of Surge Voltage at IGBT Turn-Off
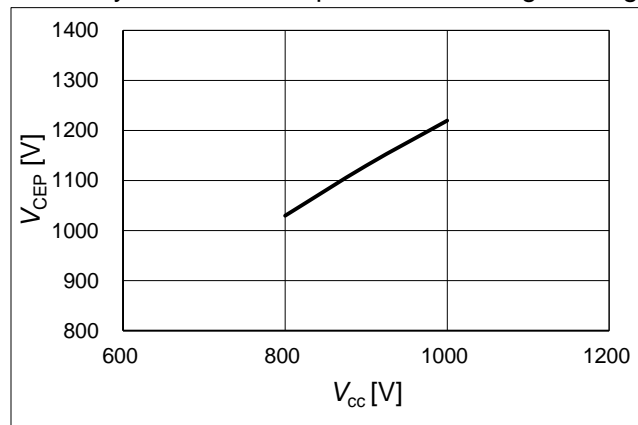


Condition : $V_{GE}=\pm15V$, $L_S=51nH$, $R_G=0.5\Omega$, $T_j=125°C$, $I_C=400A$

Fig.3-2　Example of Collector Voltage Dependence of Surge Voltage at IGBT Turn-Off



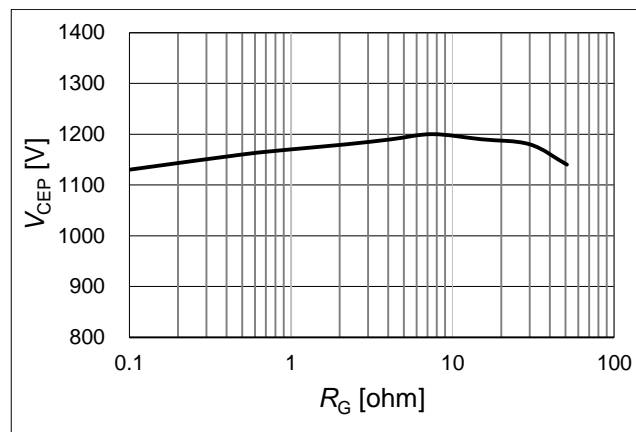Condition : $V_{GE}=\pm15V$, $V_{CC}=900V$, $L_S=51nH$, $R_G=0.5\Omega$, $T_j=125°C$

Fig.3-3　Example of Current Dependence of Surge Voltage at IGBT Turn-Off

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## 3.2    Gate resistance dependence of surge voltage at turn off

In relation to overvoltage protection, Fig.3-4 shows the gate resistance $R_G$ dependence of SiC hybrid module.

The method of increasing the gate resistance has been used commonly to reduce the surge voltage. However, the injection efficiency of IGBT chips of the latest trench technology has been improved and so the dependence between surge voltage and $R_G$ has changed (See Fig.3-4 for details.)

Therefore, if a bigger gate resistance $R_G$ is selected in order to reduce the surge voltage, the result may be different compared to conventional well-known trends. In some cases, the surge voltage may even become higher while increasing the $R_G$. Accordingly, check the choice of gate resistance carefully by using the actual machine.



Condition : $V_{GE}$=±15V, $V_{CC}$=900V, $L_s$=51nH, $I_c$=400A, $T_j$=25°C

Fig.3-4   Example of Gate Resistance Dependence of Surge Voltage at IGBT Turn-off

Reference

1)  Y. Onozawa *et al.*, "Investigation of carrier streaming effect for the low spike fast IGBT turn-off", *Proc. ISPSD*, pp.173-176, 2006.

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6

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### 3.3 Overvoltage protection when short-circuit current is cut off

If an IGBT is short-circuited, the collector voltage of the IGBT will suddenly increase. If the collector current is cutoff during this high energy state, the IGBT is facing a very high voltage and current. For this operating condition the short circuit safe operation area (SCSOA) is defined, which is different to the RBSOA.

Fig.3-5 shows SCSOA and RBSOA for SiC hybrid module (1700V). For turn off operation at short-circuit cut off, keep the operation trajectory of $V_{CE}$-$I_C$ within the SCSOA. Note that SCSOA is non-repetitive whereas RBSOA is defined as repetitive.
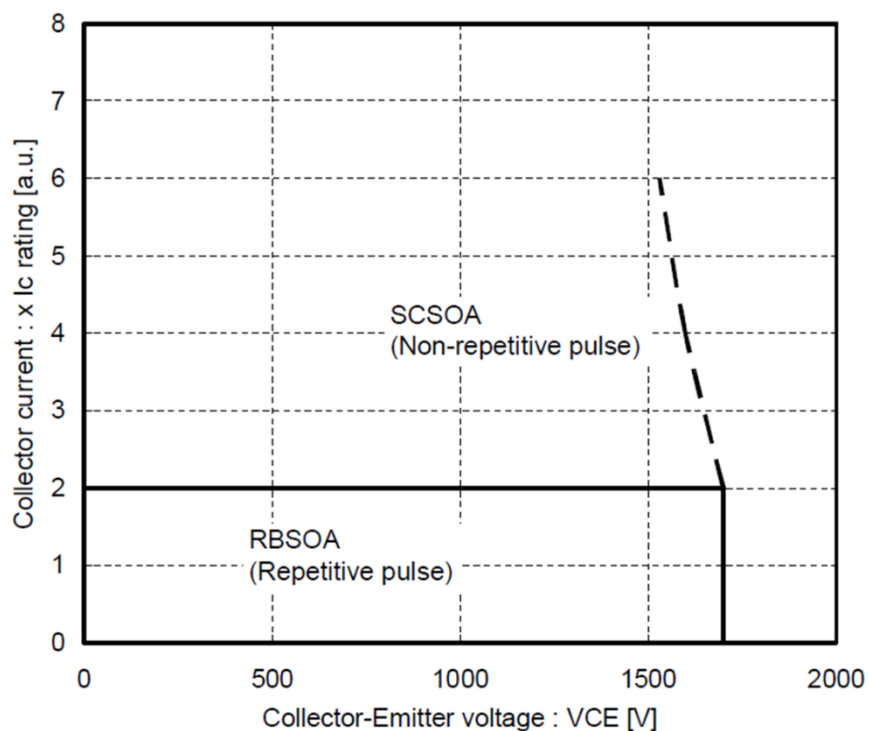


Condition : $V_{GE}$=±15V, $R_G$ ≥ $R_G$ (spec), $T_j$=150°C

Fig.3-5  RBSOA and SCSOA（1700V Family）

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# 4  $R_G$ selection

Standard gate resistance $R_G$ is indicated in the specification sheet.

Regarding the turn on $R_G$, Fuji recommends to use the standard resistance value described in the specification sheet, but it is necessary to confirm that the radiation noise stays within the allowable range.

Regarding the turn off $R_G$, as shown in Fig.4-1, increasing the $R_G$ may cause the surge voltage to increase, so it's necessary to confirm that the surge voltage in the actual machine is within the allowable range.
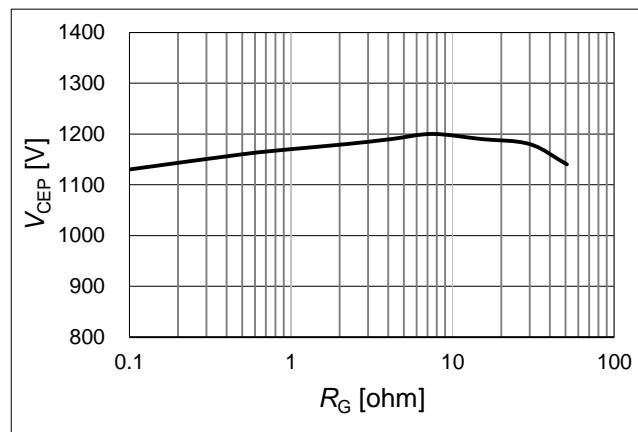


Condition : $V_{GE}$=±15V, $V_{CC}$=900V, $L_s$=51nH, $I_C$=400A, $T_j$=25°C

Fig.4-1   Example of Gate Resistance Dependence of Surge Voltage at IGBT Turn-off

Reference

1)  Y. Onozawa *et al.*, "Investigation of carrier streaming effect for the low spike fast IGBT turn-off", *Proc. ISPSD*, pp.173-176, 2006.

## 5 Parallel connection

When IGBT modules are used in a converter circuit, they are sometimes connected in parallel to handle larger output current. This section describes the precautions for parallel connection of the SiC hybrid modules.

### 5.1 Junction temperature dependence of output characteristics and current imbalance

The junction temperature dependence of the output characteristics ($V_{CE(sat)}$, $V_F$) has a big influence to the current imbalance. Typical output characteristics of a 1700V/400A rated module are shown in Fig.4-1. The temperature dependence of the V-IGBT and SiC-SBD used in the hybrid module is positive. Therefore, the collector current decreases while the junction temperature increases. This will automatically improve the current imbalance.

Because of this fact, all chips used for Fuji hybrid modules have characteristics that are suitable for parallel operation.
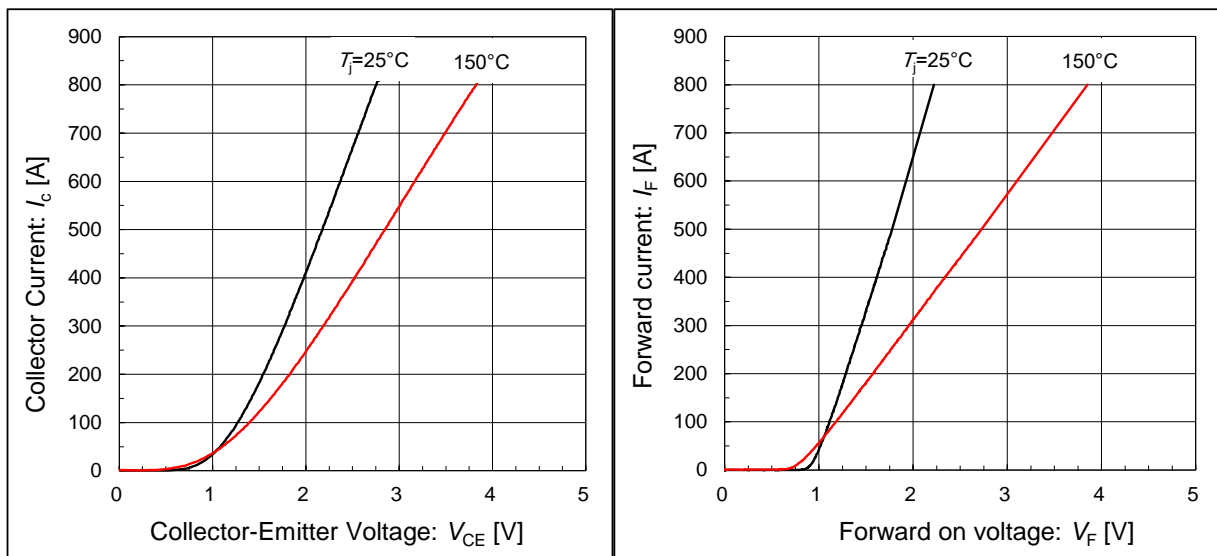


(a) Output characteristics of IGBT      (b) Output characteristics of SiC-SBD

Fig.5-1  Junction temperature dependence of output characteristics

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## 5.2 Variation and current imbalance ratio of $V_{CE(sat)}/V_F$

The ratio of current sharing, which occurs at parallel connection of SiC hybrid modules, is called current imbalance ratio. This is decided by the variation in $V_{CE(sat)}/V_F$ and the junction temperature dependence of these characteristics.

Fig.5-2 shows the relation between typical variation of $V_{CE(sat)}/V_F$ and current imbalance ratio. This figure shows the current imbalance ratio for two parallel connected modules of V series IGBT and SiC - SBD. As shown by the figure, it can be seen that the current imbalance ratio increases as the variation of $V_{CE(sat)}/V_F$ increases. Therefore, when connecting in parallel, it is important to combine products with small $V_{CE(sat)}/V_F$ difference ($\Delta V_{CE(sat)}/\Delta V_F$).



$$\alpha = \left(\frac{I_{c1}}{I_{c(ave)}} - 1\right) \times 100$$
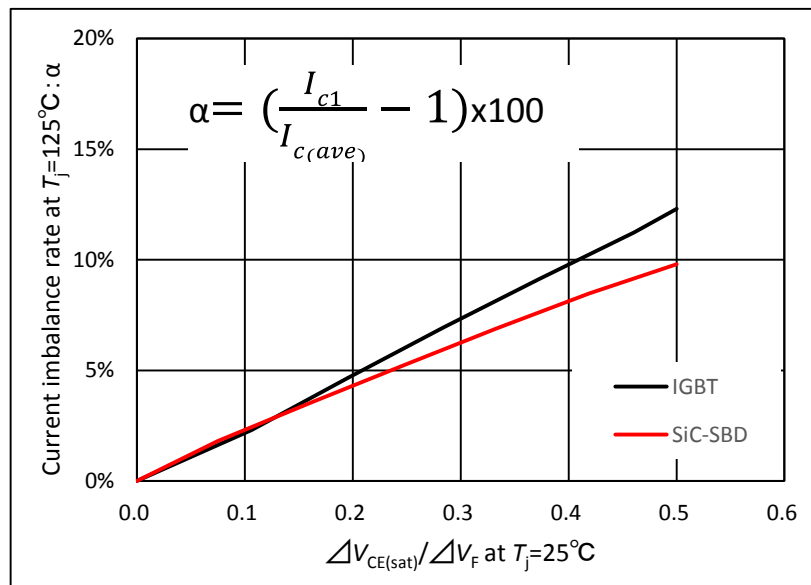
Condition : $V_{CC}$=900V, $f_{sw}$=5kHz, Total $I_C$=800Arms, Power factor=0.9, Modulation rate=0.8

Fig.5-2 Variation and current imbalance ratio of $V_{CE(sat)}/V_F$ （1700V/400A）

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■ **Supplement: regarding label notation of module characteristic data**

The module's $V_{CE(sat)}$ and $V_F$ values are mentioned on the label. Good current balance can be obtained by combining the same or close $V_F$ rank and $V_{CE(sat)}$ rank. Fig.5-3 shows an example of label notation.

Notation contents :

- $V_{CE(sat)}$, $V_F$ values           (ex. '211' = 2.105 ~ 2.114 V)
- Temperature code: R
- Product code
- Lot No.
- Serial No.
- Data matrix code



**Characteristics indication**
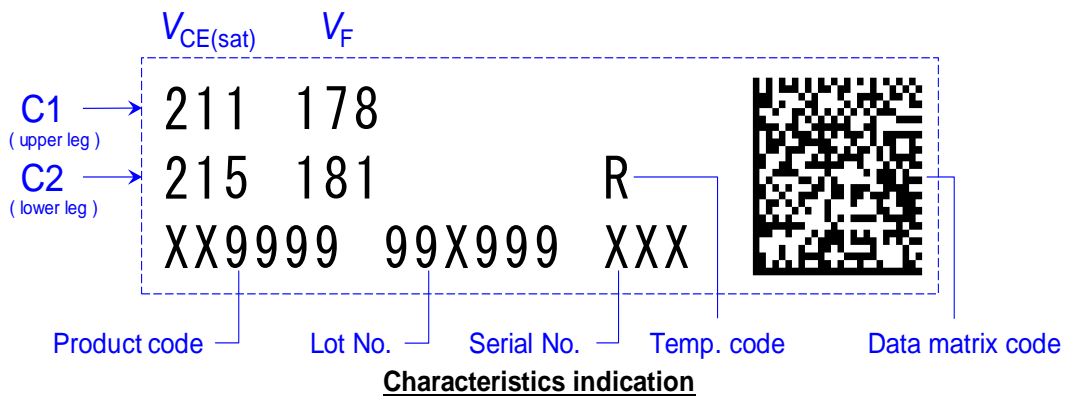
| | | Product code | comma | Lot No. | comma | Serial No. | comma | $V_{CE(sat)}$(C1) upper leg | comma | $V_F$(C1) upper leg | comma | $V_{CE(sat)}$(C2) lower leg | comma | $V_F$(C2) lower leg | comma | Temp. code* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| メイバンと同じ（右詰め6桁） | | | | メイバンと同じ | | メイバンと同じ | | | | | | | | | | |
| | | 6digits | | 5 or 6digits | | 3digits | | 3digits | | 3digits | | 3digits | | 3digits | | 1digit |

*Room temp.=R
*High temp.=H

**Data matrix code contents**

Fig.5-3. Notation example of characteristic data

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## 5.3 Current imbalance at switching

### 5.3.1 Main circuit wiring inductance distribution

Inhomogeneous main circuit wiring inductance cause an imbalanced current sharing of parallel connected devices.

Fig.5-4 shows the equivalent circuit at parallel connection in consideration with the main circuit wiring inductance. If $I_{C1}$ and $I_{C2}$ flow through IGBT1 and IGBT2 respectively, the current sharing is approximately decided by the ratio of main circuit wiring inductance, $L_{C1}+L_{E1}$ and $L_{C2}+L_{E2}$. So, the main circuit wiring is needed to be designed as equally as possible in order to reduce current imbalance at switching. However, even if ideal wiring inductance of $(L_{C1}+L_{E1}) = (L_{C2}+L_{E2})$ is realized, a difference between $L_{E1}$ and $L_{E2}$ can cause a voltage imbalance which is described below.

Inhomogeneous inductance of $L_{E1}$ and $L_{E2}$ induce a different voltage, even if the same $di/dt$ occurs. This difference in induced voltage will affect the gate emitter voltages and will cause a current imbalance. This imbalance will increase the total collector current imbalance.

Fig.5-4 Equivalent circuit at parallel connection in consideration with main circuit wiring inductance

Because of this, it's extremely important to ensure the symmetry of the wiring structure for the collector and emitter side separately: $L_{C1} = L_{C2}$, $L_{E1} = L_{E2}$.

Another point is to keep the inductance of the main circuit as low as possible because of the direct correlation between inductance and spike surge voltage during turn off. Therefore, for the purpose of reducing wiring induction, consider to place the paralleled modules as close together as possible and design the wiring as uniform as possible.

If the IGBT module has an auxiliary emitter, it is recommended to drive the gate with its emitter terminal in order to reduce the influence of the main circuit inductance.
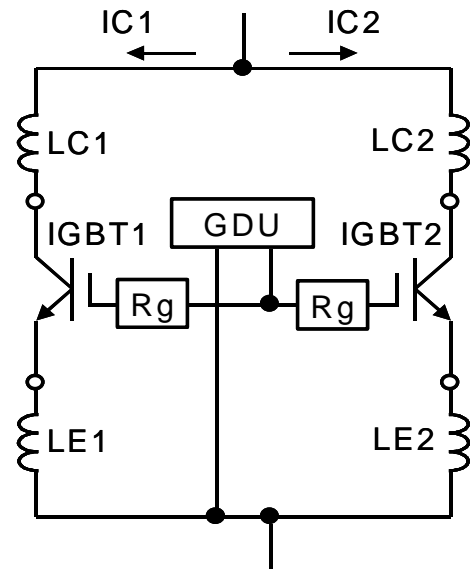
### 5.3.2 Gate drive circuit

In the case of using separated gate driving units (GDU) for each IGBT there is a potential source of trouble due to the variations in the delay time of each circuit which will have a negative effect to simultaneously switching. Therefore, it is recommended that all the gates of paralleled modules are driven by just one GDU. By using this setup, it is possible to reduce the variation in switching time caused by the gate drive circuit. However, if the module gates connected in parallel are operated by the same driving circuit, there are concerns that the switching speed is lowered due to insufficient drive capability. This may make the gate control impossible. Therefore, please select the driver capability accordingly.



Fig.5-5  Wiring gate drive unit

Also, when using a single gate drive circuit, parasitic oscillation may occur at the rise of the gate voltage depending on the wiring inductance and the IGBT input capacitance. Therefore, the gate resistances of each IGBT should connected individually to the respective gates (please refer to Fig.5-5). Also an additional emitter line resistor can help to suppress this oscillation. Keep in mind that the voltage drop which is caused by these resistors may cause a device malfunction.

When the emitter wiring of the gate drive circuit is connected to different positions of the main circuit wiring, $L_{E1}$ and $L_{E2}$ become unbalanced, shown in Fig. 5-4. This leads to an unbalanced transient current sharing. Normally, IGBT modules have an auxiliary emitter terminal for the gate drive circuit. The internal drive wiring is even.

Therefore, by using this auxiliary terminal to drive the gate, transient current imbalance inside the module can be suppressed. For this reason, this setup is recommended.

Even if the gates are driven by using the auxiliary emitter terminals, there is still the impact of the external wiring. Therefore, please make sure that the wiring of the gate drive circuit to each module connected in parallel is the shortest possible with equal length. Fuji recommends to use tightly twisted wires for the gate drive circuit which should kept away as much as possible of the main circuit wiring. This will reduce the possibility of mutual induction (especially by the collector current).
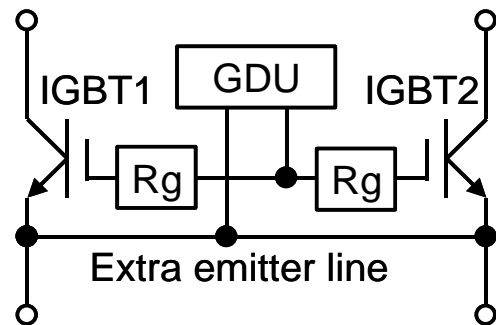
## 6 EMI

Fig.6-1 shows the radiation noise comparison of the 1700V SiC hybrid module and the conventional Si module.

While the collector current decreases, the radiation noise increases for the conventional Si module. The SiC hybrid module shows an opposite behavior. The radiation noise decreases while the collector current decrease. In the region of 300 A and less, the peak value of the radiation noise of the SiC hybrid module is equivalent to that of the conventional Si module.
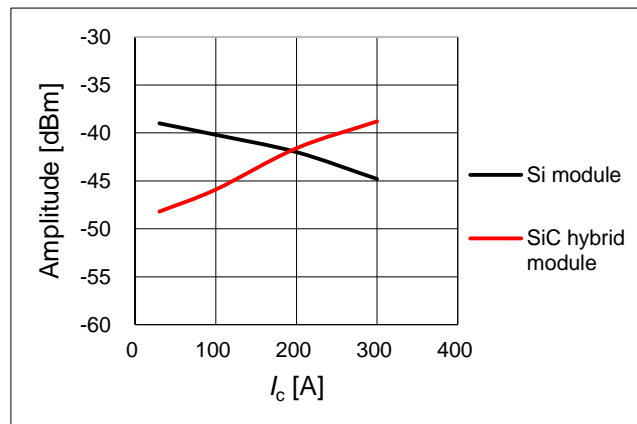


Fig.6-1 Collector current dependence of radiation noise

Reference

2) H. Wang, *et al.*, "1700V Si-IGBT and SiC-SBD Hybrid Module for AC690V Inverter system", I*nternational Power Electronics Conference (IPEC-Hiroshima 2014-ECCE=ASIA)*, pp. 3702-3706.

## 7 Method of suppressing waveform ringing

Fig.7-1 shows an example of the turn-off waveform of the SiC-SBD.

The waveform ringing can be suppressed by adding a CR snubber between the collector and the emitter of the hybrid module.



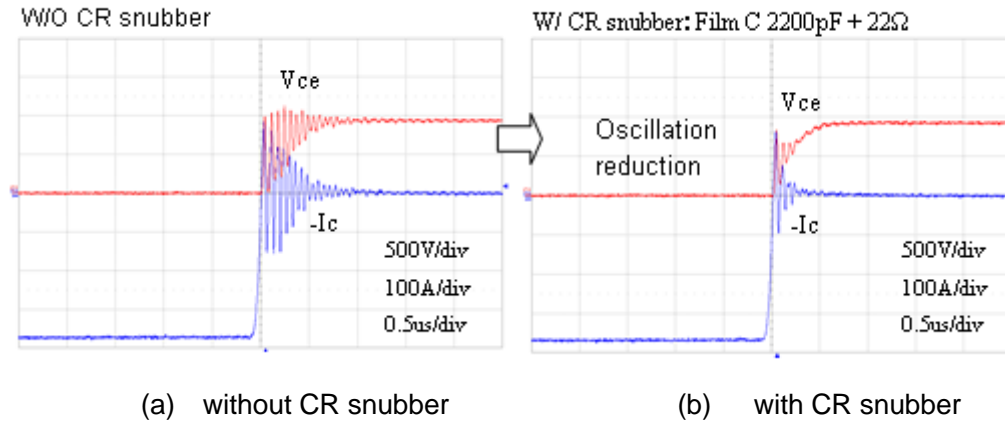(a)   without CR snubber                    (b)     with CR snubber
Fig.7-1    Suppression of waveform vibration by CR snubber circuit
※Patent pending

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