Chapter 10 Parallel Connections

This chapter explains the notes when IGBT is connected in parallel.

IGBTs would be connected in parallel in order to enlarge the current capability. In this case, the number of parallel-connected modules has no limitation. However you have to consider some disadvantages of noise or spike voltage increase, which are caused by longer interconnections. You have to pay attention to the following basic notes when connecting IGBT modules in parallel.

(1) Suppression of current imbalance at steady states
(2) Suppression of current imbalance at dynamic state of turn-on or turn-on
(3) Symmetry of gate drive circuit
(4) Strict observance of specifications such as water flow, water temperature and pressure within each water jacket

1. Current Imbalance at Steady State

An on-state current imbalance may be mainly caused by the following two factors:
(1) $V_{CE(sat)}$ distribution
(2) Main circuit wiring resistance distribution

1.1 Current imbalance caused by $V_{CE(sat)}$ distribution

As shown in Fig. 10-1, a difference in the output characteristics of two IGBT modules connected in parallel can cause a current imbalance.

The output characteristics of Q_1 and Q_2 shown in Fig. 10-1, can be approximated as follows:

$$V_{CEQ1} = V_{01} + r_1 \times I_{C1}$$
$$r_1 = V_1/(I_{C1} \_ I_{C2})$$

$$V_{CEQ2} = V_{02} + r_2 \times I_{C2}$$
$$r_2 = V_2/(I_{C1} \_ I_{C2})$$

Based on the above, if the I_{ctotal} ($=I_{C1}+I_{C2}$) collector current is made to flow through the circuit of Q_1 and Q_2 connected in parallel, then the IGBT's collector current becomes the following:

$$I_{C1} = (V_{02} - V_{01} + r_2 \times I_{Ctotal})/(r_1+r_2)$$
$$I_{C2} = (V_{01} - V_{02} + r_1 \times I_{Ctotal})/(r_1+r_2)$$

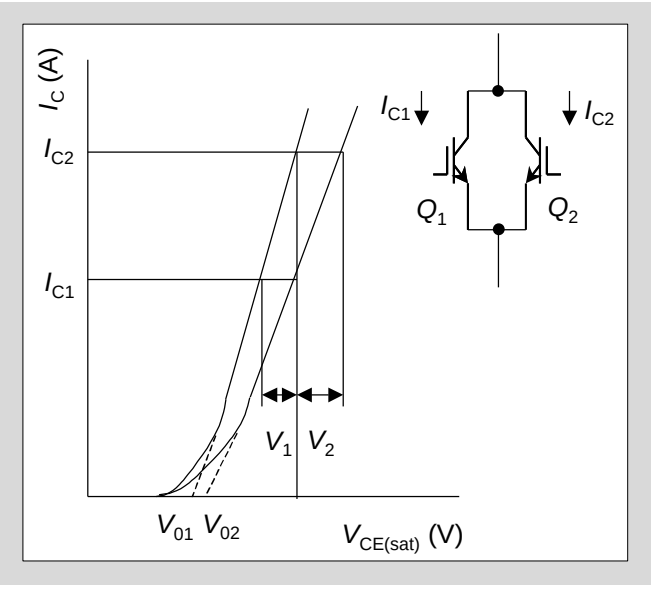

Fig. 10-1 Example of a $V_{CE(sat)}$ pair

For simplicity, assuming V_{01}=V_{02} in the above equations, I_{C1} could be r_2/r_1 times larger than I_{C2}. Also, it can be seen from Fig. 10-1 that r2> r1.This result means that current sharing for Q_1 is larger than Q_2.

In this way, $V_{CE(sat)}$ becomes a major factor in causing current imbalances. Therefore, in order to ensure the desired current sharing it is necessary to pair modules that have a similar $V_{CE(sat)}$ which is small variation. $V_{CE(sat)}$ distribution can be minimized with the use of the same production lot, because influence of fabrication processes is minimized. From this reason, connecting IGBT modules in parallel is recommended with the use of the same production lot.

1.2 Current imbalance by main circuit wiring resistance distribution

The equivalent circuit with the main circuit's wiring resistance is shown in Fig. 10-2. The effect is larger with emitter resistance than with collector resistance, so collector resistance has been omitted here. If there is resistance in the main circuit as shown in Fig. 10-2, then the slope of the IGBT modules' output characteristics will lessen, and the collector current will drop in comparison without emitter resistance. In addition, if $R_{E1}>R_{E2}$, then the slope of the Q_1 output characteristics will lessen and if $I_{C1}<I_{C2}$ then a current sharing imbalance will appear. Moreover, if gate voltage is applied without extra-emitter terminals for parallel-connected IGBTs, the actual gate-emitter voltage drop ($V_{GE}=V_G - V_E$) will be decreased, because an electrical potential difference may appear, depending on how well the collector current can flow through this resistance. So, the IGBTs' output characteristics change and the collector current decline.

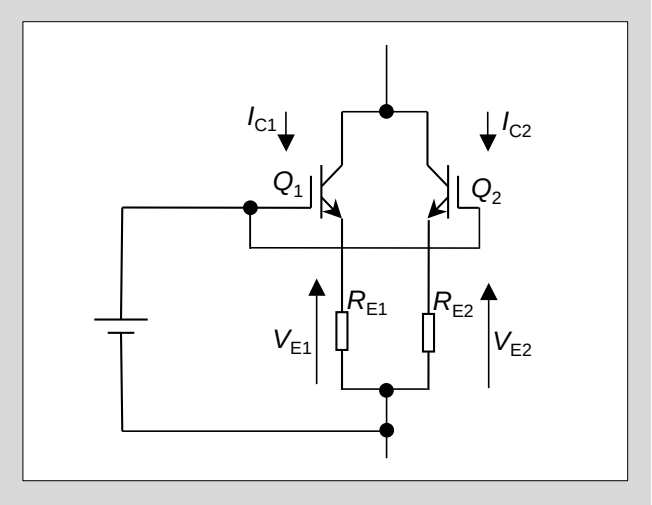

Fig. 10-2 The effect of main circuit wiring resistance

Therefore, in order to reduce this imbalance, it is necessary to make the wiring on the emitter side as short and as uniform as possible as well as to apply the gate voltage between gate terminal and additional emitter terminal.

1.3 T_{vj} dependence of output characteristics and current imbalance

T_{vj} dependency of output characteristics deeply affects current imbalance. Here, output characteristic, whose $V_{CE(sat)}$ is higher and lower with the increase of T_{vj}, is respectively defined as the positive and negative T_{vj} dependency. Fig. 10-3 shows the representative output waveform with negative and positive dependency, which are 100A rating. Collector current at the same V_{CE} is decreased as T_{vj} is increased in case of positive dependency.

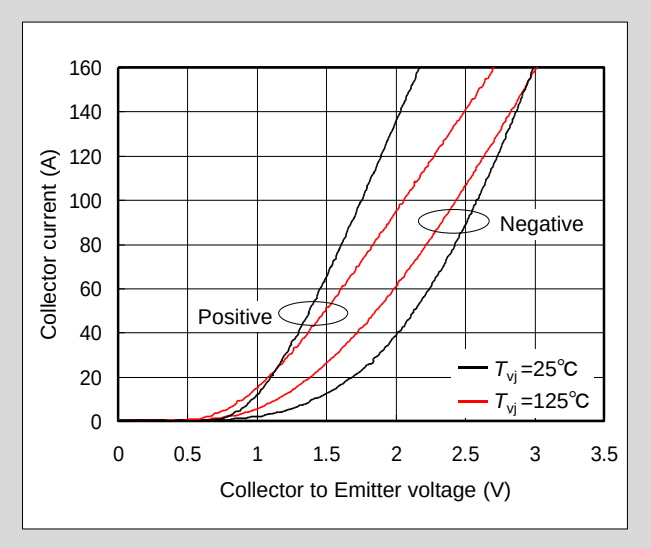

Fig. 10-3 Comparison output characteristics

As described 1.1, shared current of IGBT with lower $V_{CE(sat)}$ is larger at the parallel connecting. Therefore, steady-state loss is larger for IGBT with lower $V_{CE(sat)}$ than another to increase junction temperature. In this way, in case of positive dependency of IGBT, this leads to make shared current between them balanced. On the contrary, in case of negative dependency, current sharing is act as opposite work. Therefore, you need to pay attention to current imbalance in designing the machines or components. Selecting the IGBTs with the positive dependency of output characteristic is recommended when IGBTs are parallel-connected, because IGBTs with positive dependency of output characteristic are relatively easier to use for parallel connection of IGBTs than that with negative one. Please refer to the each series specification for details of T_{vj} dependency of output characteristic.

1.4 Deviation of $V_{CE(sat)}$ and current imbalance rate

Ratio of shared current in parallel connection is called as current imbalance rate, which is determined by deviation of $V_{CE(sat)}$ and T_{vj} dependency of output characteristic.

Fig. 10-4 shows the representative relationship between deviation of $V_{CE(sat)}$ and current imbalance rate. This figure is an example for 2 parallel connections of a series of IGBTs. From this figure, current imbalance rate is found to be larger as deviation of $V_{CE(sat)}$ is increased. Therefore, it is important to use IGBTs for parallel connection, whose deviation of $V_{CE(sat)}$ is small, that is, $\Delta V_{CE(sat)}$ is small.

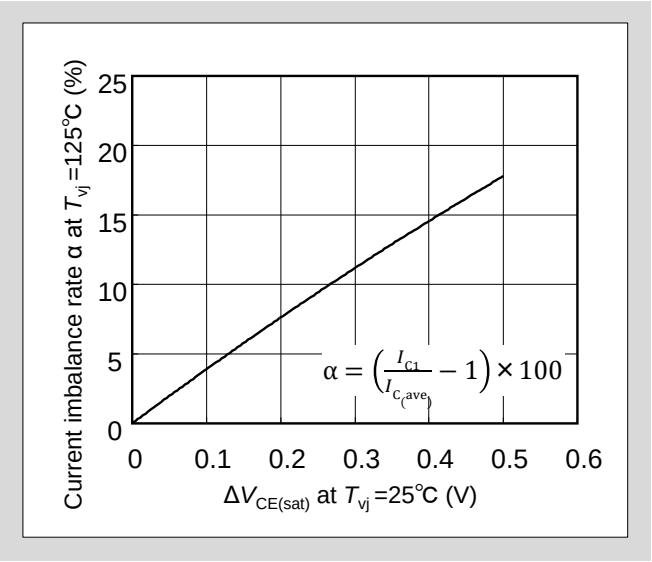

Fig. 10-4 Deviation of $V_{CE(sat)}$ and current imbalance rate

*Fig. 10-4 is an example of an IGBT series. In fact, when calculating the available maximum current (Σ*I*) for parallel connection, refer to the technical data for each IGBT series.

1.5 Derating in parallel connection using many numbers of IGBTs

Derating (Decrease of total current) is needed in consideration with current imbalance in parallel connection of IGBTs.

When n-number of modules are connected in parallel, the following shows the maximum current that can be applied under the worst case conditions where the entire current is concentrated into one module, whose $V_{CE(sat)}$ is the smallest. Therefore, available maximum current Σ*I* is expressed by a, which is connected in parallel using 2 modules:

$$\sum I = I_{C(max)} \left[1 + (n-1)\frac{\left(1-\frac{\alpha}{100}\right)}{\left(1+\frac{\alpha}{100}\right)}\right] \qquad \alpha = \left(\frac{I_{C1}}{I_{C(ave)}} - 1\right) \times 100$$

Here $I_{C(max)}$ represents the maximum current for a single element, Σ*I* represents the maximum current in parallel connection. However, to operate in total current Σ*I*, each module connected in parallel is satisfied with the RBSOA on the specification, T_{vjmax} for dissipation wattage as well. Note especially that T_{vj} rise caused by dissipation wattage is various on the condition such as switching frequency, driving condition, cooling condition and snubber condition and so on.

For example, if α=15%, $I_{C(max)}$ =200A and n=4, then Σ*I*=643.4A, and the parallel connected total current should be set so as not to exceed this value. In this case, Derating of 19.6% is needed. In this way, the parallel connected total current is need to be derated for simply calculating n × $I_{C(max)}$.

Fig. 10-5 shows the derating rate for α=15%. It is found from this figurer that derating rate is increased as the parallel number n is larger. Therefore, derating the total current for parallel connection, depending on the parallel number n. in addition, note that derating rate is various by current imbalance rate.

Because derating rate for this example is a calculated value. It should be determined after confirmation and verification of imbalance current using designed machines.

If you need to change paralleled modules for troubles and/or maintenances, it is recommended that all the paralleled modules be exchanged. In this case, it is recommended that parallel connection be set up using IGBTs with the same production lots.

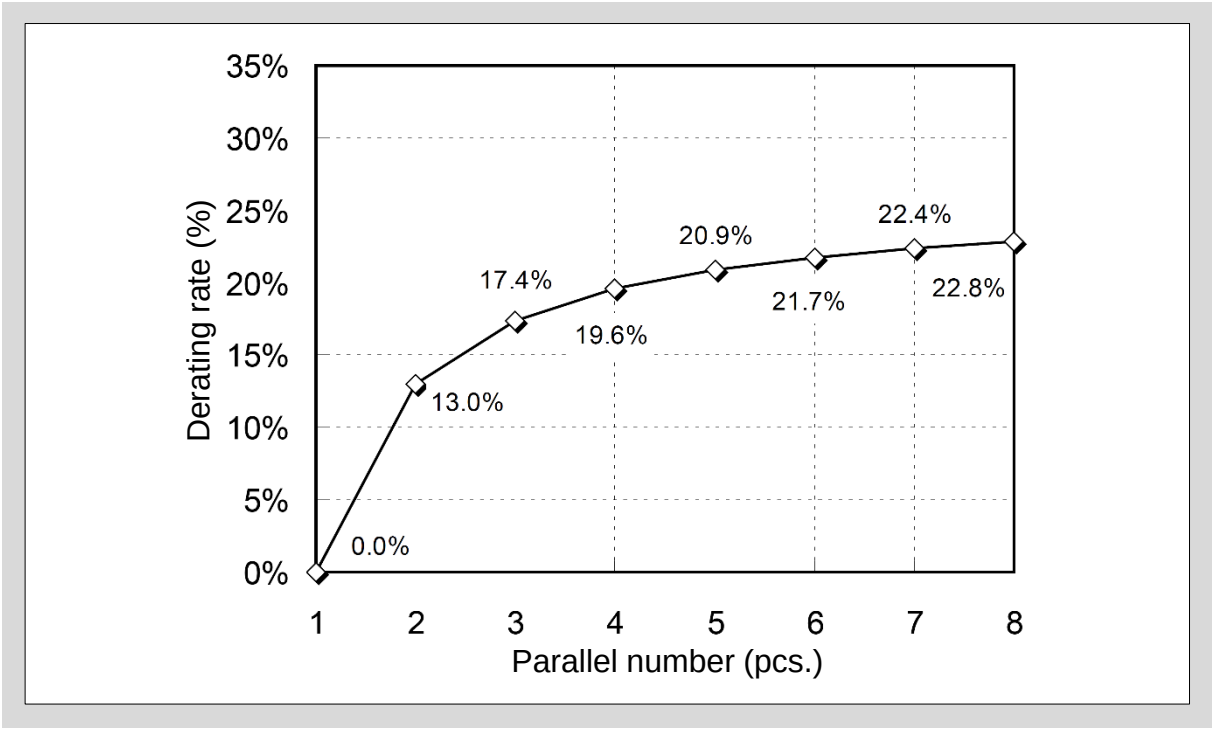

Fig. 10-5 Relationship between derating rate and parallel number

2. Current Imbalance at Switching

Current imbalance at switching may be mainly caused by the following two factors:

(1) Module characteristics distribution

(2) Main circuit wiring resistance distribution

2.1 Module characteristics distribution

An IGBTs' switching current imbalance, especially just before turn-off and after turn-on, is mostly determined by an on-state current imbalance, therefore if the on-state current imbalance is controlled simultaneously as shown previously, so will the switching voltage imbalance.

2.2 Main circuit wiring inductance distribution

Inhomogeneous main circuit wiring inductance caused current sharing. Fig. 10-6 shows the equivalent circuit at parallel connection in consideration with main circuit wiring inductance. When I_{C1} and I_{C2} flow through $IGBT_1$ and $IGBT_2$ respectively, shared currents for them are approximately decided by the ratio of main circuit wiring inductance, $L_{C1}+L_{E1}$ and $L_{C2}+L_{E2}$. So, main circuit wiring is need to be connected as equally as possible in order to relieve current imbalance at switching. However, even if ideal wiring inductance of $L_{C1}+L_{E1}=L_{C2}+L_{E2}$ is realized, the difference between L_{E1} and L_{E2} causes the current imbalance as described bellows.

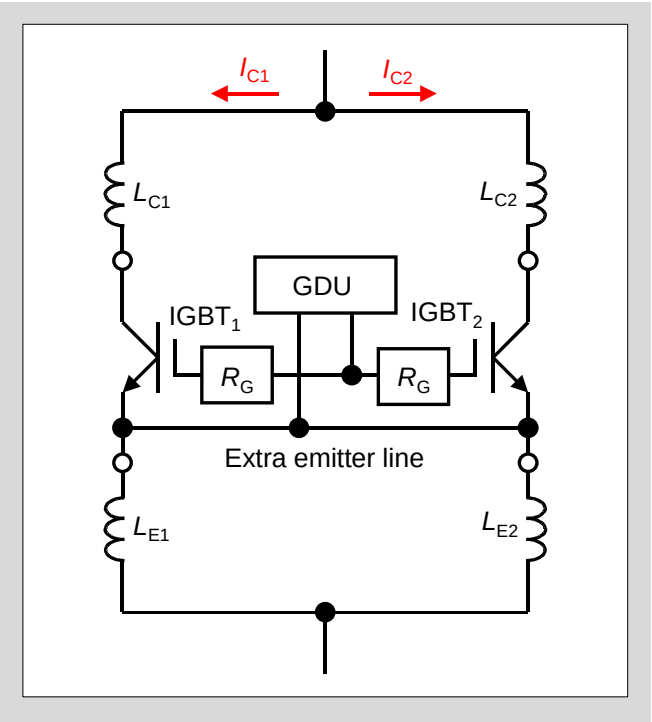

Fig. 10-6 Equivalent circuit at parallel connection in consideration with main circuit wiring inductance

Inhomogeneous inductance between L_{E1} and L_{E2} causes the different inductive voltage originated d*i*/d*t* at turn-on. This difference between their inductive voltages affects current imbalance more, because it biases to different way to gate to emitter voltage.

If the inductance of the main circuit is large, then the spike voltage at IGBT turn-off will also be high. Therefore, for the purpose of reducing wiring induction, consider setting the modules that are to be connected in parallel as close together as possible and making the wiring as uniform as possible.

3. Gate Drive Circuit

It would be worried that duration until switching (turn-off or turn-on) is varied by the delay time of gate driving unit (GDU), when each gate of parallel-connected modules is driven by each GDU, separately independent on the number of modules. Therefore, it is recommended that all the gates are driven by just only a GDU, when connecting modules in parallel. This can lead the decrease of deviation for different duration until switching.

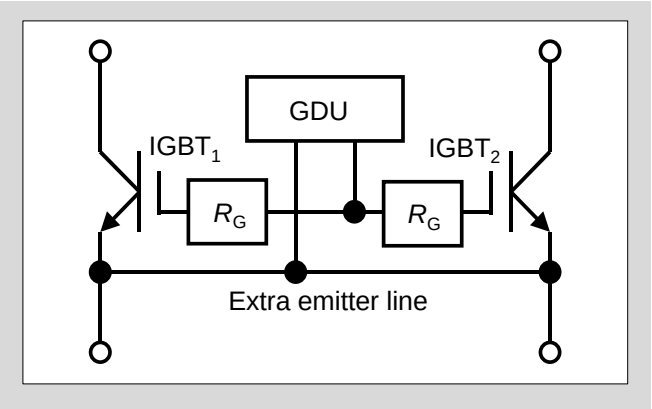

Fig. 10-7 wiring gate drive unit

At the same time, connect gate resistances between gate terminal of each module and a GDU so as to avoid the gate voltage oscillation caused by coupling gate wiring inductance with input capacitance of IGBT as shown in Fig. 10-7.

As stated previously, if the drive circuit's emitter wiring is connected in a different position from the main circuit, then the modules' transient current sharing (especially at turn-on) will become imbalanced, because L_{E1} is different from L_{E2} as described in Fig. 10-6.

In general, IGBT modules have an auxiliary emitter terminal for use by drive circuits. By using this terminal, the drive wiring of each module becomes uniform, and transient current imbalances attribute to drive circuit wiring can be controlled. Furthermore, be sure to wind the drive circuit wiring tightly together, and lay it out so that it is as far away from the main circuit as possible in order to avoid mutual induction.

4. Wiring Example for Parallel Connections

As described before, pay attention in order to connect the modules in parallel. Fig. 10-8 shows the equivalent circuit with parallel-connected 2in1 modules. From this figure, it is found that all the wiring to parallel-connected IGBTs ($IGBT_1$ and $IGBT_2$) are connected symmetrically. This can realize the better current sharing.

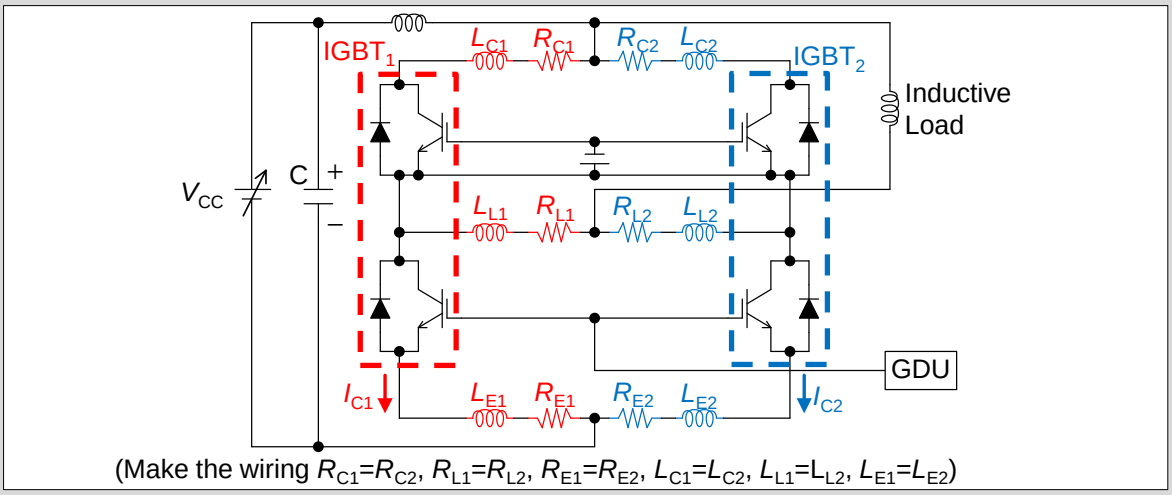

Fig. 10-8 Equivalent circuit with parallel-connected 2in1 modules

5. Cooler

This IGBT module has the cooler with the water jacket. Even when IGBT modules are connected in parallel, please adhere strictly to the specifications of water temperature, water flow and pressure within each water jacket and fully confirm that there are no problems with the junction temperature etc. of each IGBT.