– Chapter 2 –

Description of terminal marking and terms

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1 Descriptions of the I/O terminals

Main terminals

Terminal Name	Description
P (P1, P2) N (N1, N2)	DC-bus terminals after smoothing capacitor P: + side, N: - side
B	Collector terminal of the Brake IGBT. Connect a brake resistor for dissipating regenerated energy
U	3-phase output terminals
V	
W	

* P1, P2, N1 and N2 terminals are P631 package only.

Control terminals

Terminal Name	P629 Pin#	P626, P630, P636 Pin#	P631 Pin#	Description
GND U	1	1	1	Ground reference for the U-arm control power supply
Vcc U	3	4	3	U-arm control power supply positive terminal
Vin U	2	3	2	U-arm control signal input
ALM U	-	2	4	U-arm alarm signal output
GND V	4	5	5	Ground reference for the V-phase control power supply
Vcc V	6	8	7	V-arm control power supply positive terminal
Vin V	5	7	6	V-arm control signal input
ALM V	-	6	8	V-arm alarm signal output
GND W	7	9	9	Ground reference for the W-phase control power supply
Vcc W	9	12	11	W-arm control power supply positive terminal
Vin W	8	11	10	W-arm control signal input
ALM W	-	10	12	W-arm alarm signal output
GND	10	13	13	Ground reference for the lower arm control power supply
Vcc	11	14	14	Control power supply positive terminal for the lower arm
Vin X	12	16	16	X-arm control signal input
Vin Y	13	17	17	Y-arm control signal input
Vin Z	14	18	18	Z-arm control signal input
Vin DB	-	15	15	DB-arm control signal input
ALM	15	19	19	Lower-arm alarm signal output

* Pin (15) of P626 is of no contact.

* Pin (15) of each of P631 (6in1), P630 (6in1) is of no contact.

2 Description of terms

2.1 Absolute maximum rating

Term	Symbol	Description
DC power supply voltage	V_{DC}	Maximum DC bus voltage between the P and N terminal
DC power supply voltage at short circuit	V_{SC}	Maximum DC bus voltage between the P and N terminal during short-circuit protection and over current protection
Collector-Emitter blocking voltage	V_{CES}	Maximum voltage between the collector and emitter terminal of the built-in IGBT, and peak inverse voltage of the FWD.
Collector current	I_C	Maximum DC collector current for each IGBT
	I_{CP}	Maximum peak collector current for each IGBT
	$-I_C$	Maximum DC forward current for each FWD
Diode forward current for DB	I_F	Maximum DC forward current for FWD in brake circuit
Collector loss	P_C	Maximum power dissipation for each IGBT at Tc=25°C, Tj≤150°C
Control power supply voltage	V_{CC}	Maximum voltage between the V_{CC} and GND terminal
Input voltage	Vin	Maximum voltage between the Vin and GND terminal
Alarm voltage	V_{ALM}	Maximum voltage between the ALM and GND terminal
Chip junction temperature	T_j	Maximum IGBT/FWD chip junction temperature during continuous operation
Case temperature during operation	T_{opr}	Allowable case temperature range during operation (measured point of the case temperature Tc is shown in Figure 5-4)
Storage temperature	T_{stg}	Allowable ambient temperature during storage or transportation without being subject to electrical load.
Soldering temperature	T_{sol}	Maximum temperature for soldering the terminals to a PCB
Isolation voltage	V_{iso}	Maximum RMS isolation of sinusoidal voltage between all the terminals and heat sink (all terminals are shorted)
Screw torque — Terminal	-	Maximum screw torque for the main terminal with specified screw
Screw torque — Mounting	-	Maximum screw torque for mounting the IPM on heat sink with specified screw

2.2 Electrical characteristics

2.2.1 Main circuit

Term	Symbol	Description
Collector-Emitter leakage current	I_{CES}	Leakage current when specified voltage is applied between the collector and emitter and all input signals are "H" (=all IGBTs are turned-off).
Collector-Emitter saturation voltage	$V_{CE(sat)}$	Voltage drop between the collector and emitter when gate input signal is "L" (=IGBT is turned-on)
Diode forward voltage	V_F	Voltage drop across the diode at defined forward current at input signal is "H" (=IGBT is turned of)
Turn-on time	t_{on}	Time interval between the moment when gate input voltage has exceed Vinth(on) and the collector current has increased to 90% of the load current. (see Figure 2-1)
Turn-off time	t_{off}	Time interval between the moment when the gate input voltage has dropped less than Vinth(off) and the corrector current drops to 10% of the load current. If the collector dropping waveform is not a straight line, a tangential line is used as the substitute (see Figure 2-1)
Fall time	t_f	Time interval the collector current decreased from 90% to 10% of the load current
Reverse recovery time	t_{rr}	Time interval between the moment when the collector current exceeds 100% of the load current and the reverse recovery current disappears
Dead time	t_{dead}	Time delay of the turn-on signal from the alternate IGBT turn-off signal.

2.2.2 Control circuit

Term	Symbol	Description
Control power supply consumption current	I_{CCP}	Current flows into V_{CC} terminal of upper arm control power supply
	I_{CCN}	Current flows into V_{CC} terminal of lower arm control power supply
Input threshold voltage	$V_{inth(on)}$	Voltage above which considerable the control IC can detect the input signal as ON
	$V_{inth(off)}$	Voltage below which considerable the control IC can detect the input signal as OFF

2.2.3 Protection circuit

Term	Symbol	Description
Over current protection current	I_{CCP}	Current flows into the V_{CC} terminal of upper arm control power supply
Over current interruption lag time	t_{doc}	Lag time since the over current reaches the trip level until the protection start. See Figure 2-3
Short-circuit protection current	I_{SC}	Threshold current for short-circuit protection
Short-circuit protection lag time	t_{SC}	Lag time since the short circuit current reaches the trip level until the protection start. See Figure 2-4
Chip over heat protection temperature	T_{jOH}	Threshold junction temperature for overheat protection
Chip over heat protection hysteresis	T_{jH}	Lower hysteresis offset temperature to reactivate after the over temperature protection
Control power supply under voltage protection voltage	V_{UV}	Trip voltage to start under-voltage protection
Control power supply under voltage protection hysteresis	V_H	Higher threshold offset voltage to reactivate after the low voltage protection
Alarm output hold time	$t_{ALM(OC)}$	Alarm signal pulse width of the overcurrent protection (OC)
	$t_{ALM(UV)}$	Alarm signal pulse width of under the voltage protection (UV)
	$t_{ALM(TjOH)}$	Alarm signal pulse width of the overheat protection (TjOH)
Alarm output resistance	R_{ALM}	Value of the built-in resistance that is connected in series to alarm terminals. It limits the primary forward current of opto-coupler.

2.3 Thermal characteristics

Term	Symbol	Description
Thermal resistance between chip and case	$R_{th(j-c)Q}$	Thermal resistance between the case and IGBT chip
	$R_{th(j-c)D}$	Thermal resistance between the case and FWD chip
Thermal resistance between case and heat sink	$R_{th(c-f)}$	Thermal resistance between the case and heat sink at the condition
Case temperature	T_C	IPM case temperature (bottom surface of the cupper base plate directly under the chip)

2.4 Noise tolerance

Term	Symbol	Description
Common mode	-	Common mode noise tolerance in our test circuit

2.5 Others

Term	Symbol	Description
Mass	Wt	Mass of the IPM
Switching frequency	f_{SW}	Allowable switching frequency for the control signals to the input terminals.
Reverse recovery current	I_{rr}	Peak value of the reverse recovery current. See Figure 2-1.
Reverse bias safe operating area	RBSOA	The area of the voltage and current which the device can operate without self-damage during turn-off switching. There is a possibility to brake down when voltage or current exceed the area.
Switching loss	E_{on}	Dissipated switching energy of the IGBT during turn-on
	E_{off}	Dissipated switching energy of the IGBT during turn-off
	E_{orr}	Dissipated switching energy of the FWD during reverse recovery
Inverse voltage	V_R	Repetitive reverse peak voltage of the FRD chip in the brake unit
Input current	I_{in}	Maximum current into the Vin terminals

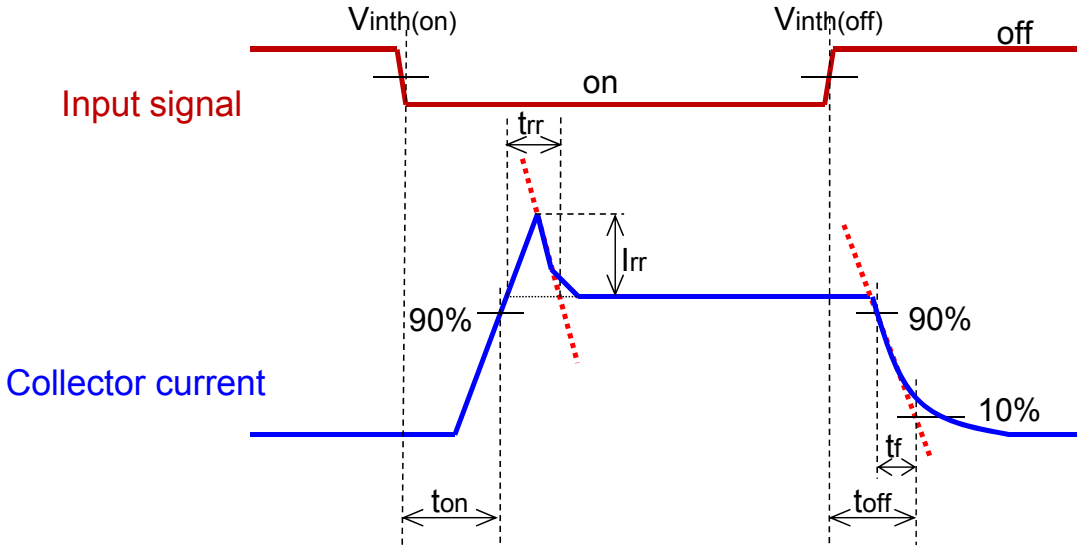

Figure 2-1 Switching times

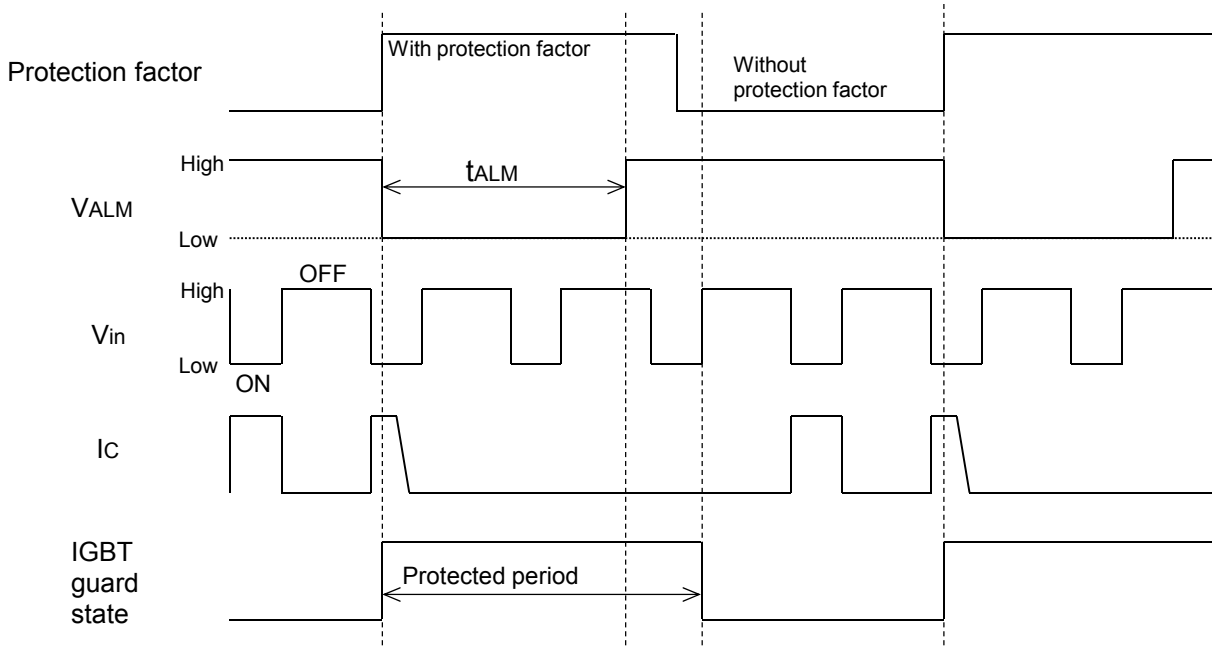

Figure 2-2 Input/output timing diagram

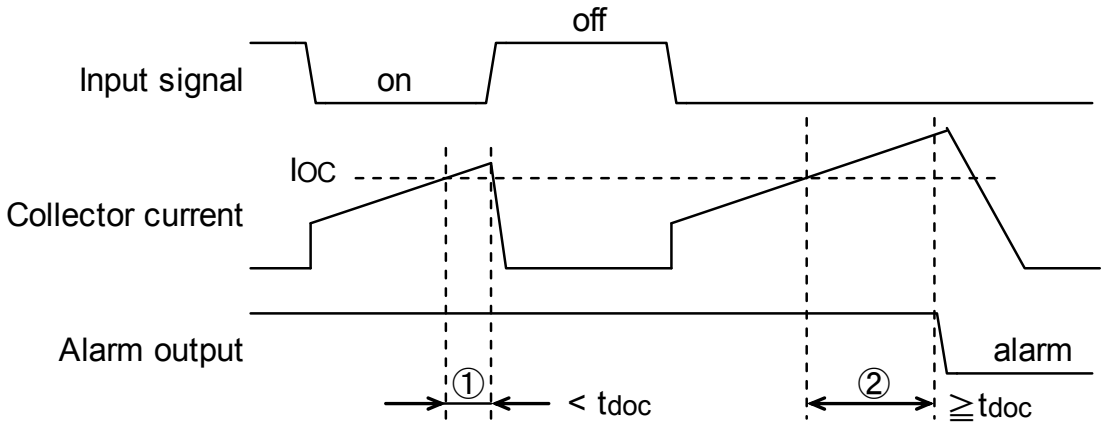

Figure 2-3 Overcurrent interruption lag time (t_{doc})

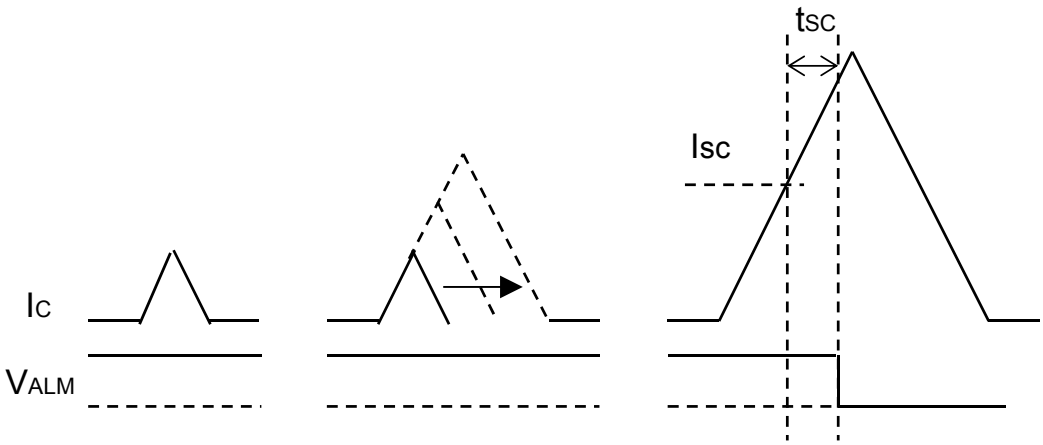

Figure 2-4 Short-circuit protection lag time (t_{sc})

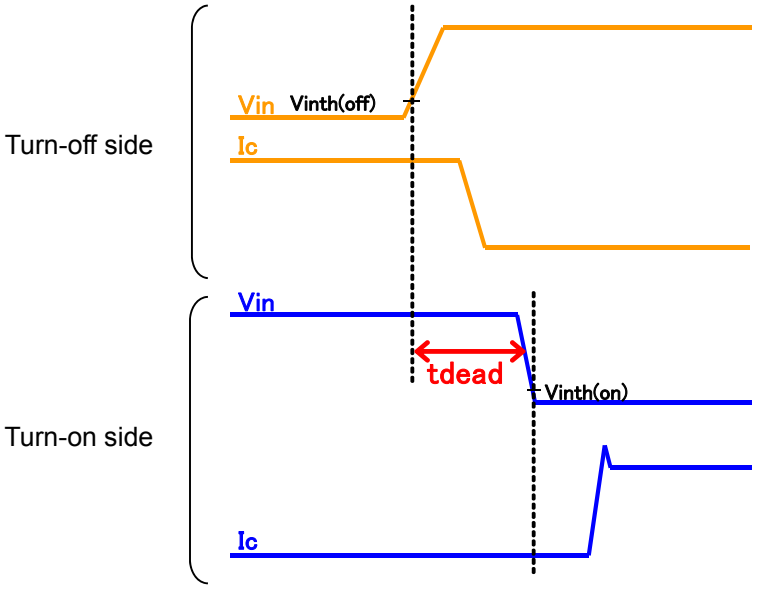

Figure 2-5 Dead time (t_{dead})