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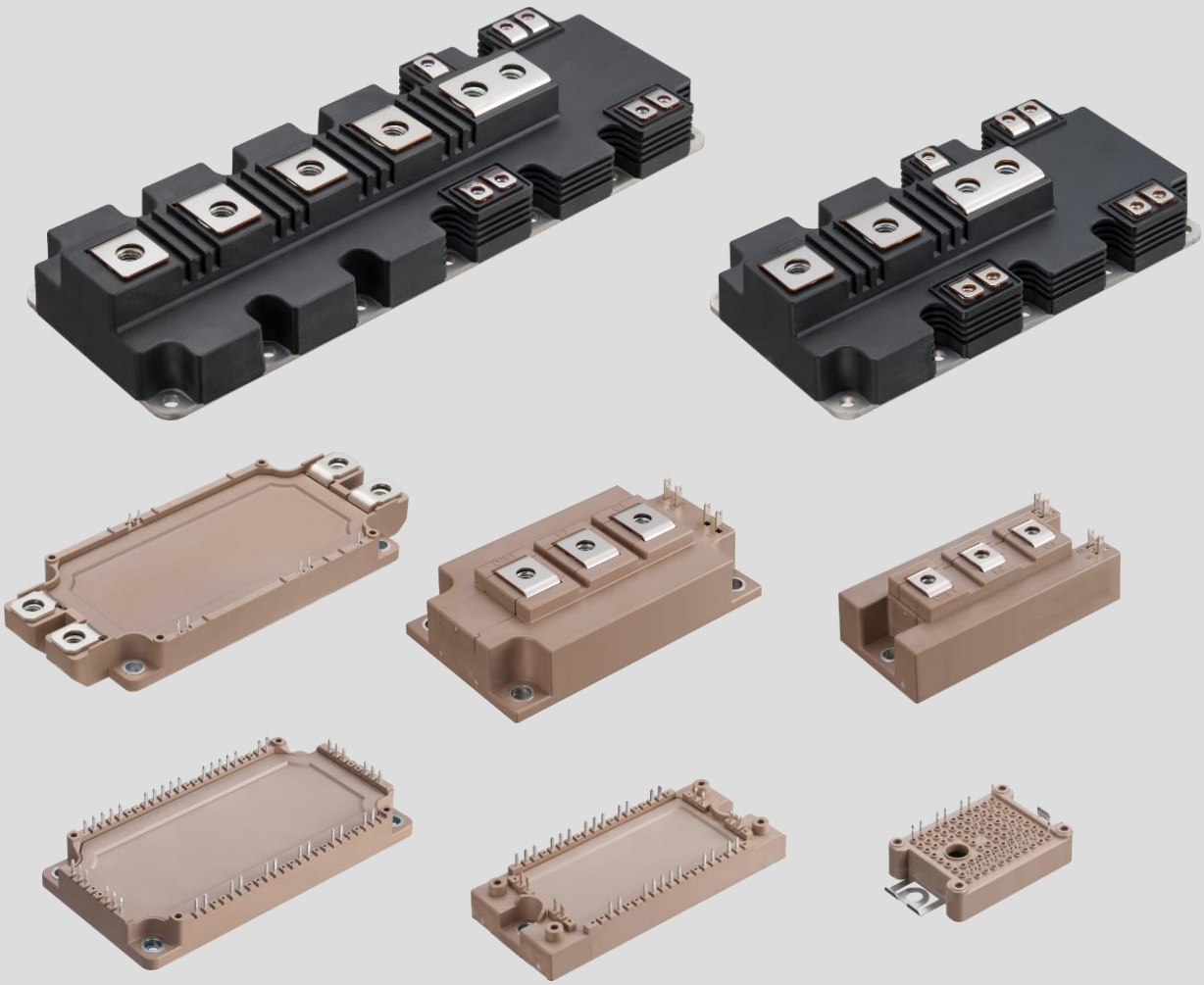

# Fuji IGBT Module

## Application Manual

March, 2023

Fuji Electric Co., Ltd.

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# Chapter 8 Parallel Connections

The IGBT current capacity can be increased by connecting the IGBT modules in parallel. However, in this case, it is necessary to consider the current imbalance between the modules, the temperature distribution, and the increase in noise and surge voltage due to the increase in wiring length.

Note the following points when connecting IGBT modules in parallel.

1. Selection of IGBT modules
2. Main circuit design
3. Gate drive circuit design
4. Cooling design

This chapter describes the details of each point when connecting IGBT modules in parallel. Note that excluding EconoPACK™+*, 6-Pack, PIM, IPM, and Small IPM cannot be used in parallel connection.

*EconoPACK™+ is a registered trademark of Infineon Technologies.

# 1. Selection of IGBT modules

Points to consider when connecting IGBT modules in parallel are $V_{CE(sat)}$ variation ($\Delta V_{CE(sat)}$) and temperature dependent characteristic differences among the IGBTs on the same arm. Due to this $\Delta V_{CE(sat)}$, that is, the difference in the output characteristics of each IGBT, current imbalance occurs in the steady-state. If this current imbalance becomes excessive, the power loss of IGBT with larger current sharing increases, and there is a possibility of thermal destruction. Therefore, when selecting IGBT modules to be connected in parallel, it is necessary to choose IGBT modules with small $\Delta V_{CE(sat)}$. This concept applies to FWD as well.

## 1.1 Current imbalance caused by $\Delta V_{CE(sat)}$

Fig. 8-1 shows the output characteristics of two IGBTs (Q1 and Q2) with different $V_{CE(sat)}$. $\Delta V_{CE(sat)}$ is the $V_{CE(sat)}$ difference between Q1 and Q2. The output characteristics of $Q_1$ and $Q_2$ can be approximated by the following equations.

$$V_{CEQ1} = V_{01} + r_1 \cdot I_{C1}$$
$$r_1 = V_1/(I_{C1} - I_{C2})$$
$$V_{CEQ2} = V_{02} + r_2 \cdot I_{C2}$$
$$r_2 = V_2/(I_{C1} - I_{C2})$$

Based on the above, when collector current $I_{Ctotal}$ ($=I_{C1}+I_{C2}$) flow through a circuit in which $Q_1$ and $Q_2$ are connected in parallel, the voltages across Q1 and Q2 being the same according to Kirchhoff's law, then each collector current can be calculated by the following equations, respectively.

$$I_{C1} = (V_{O2} - V_{O1} + r_2 \cdot I_{Ctotal})/(r_1 + r_2)$$
$$I_{C2} = (V_{O1} - V_{O2} + r_1 \cdot I_{Ctotal})/(r_1 + r_2)$$

If $V_{01}=V_{02}$ in the above equations, $I_{C1}$ is $r_2/r_1$ times larger than $I_{C2}$. As shown in Fig. 8-1, $r_2>r_1$, thus the current sharing of Q1, which is the IGBT with lower $V_{CE(sat)}$ becomes larger.

The ratio of current sharing is called the current imbalance rate, and is determined by $\Delta V_{CE(sat)}$ of each IGBT. Fig. 8-2 shows an example of current imbalance rate for 2 parallel connection of V series IGBTs. It can be seen that the current imbalance rate increases as $\Delta V_{CE(sat)}$ increases. Therefore, when connecting IGBTs in parallel, it is important to combine products with small $\Delta V_{CE(sat)}$.

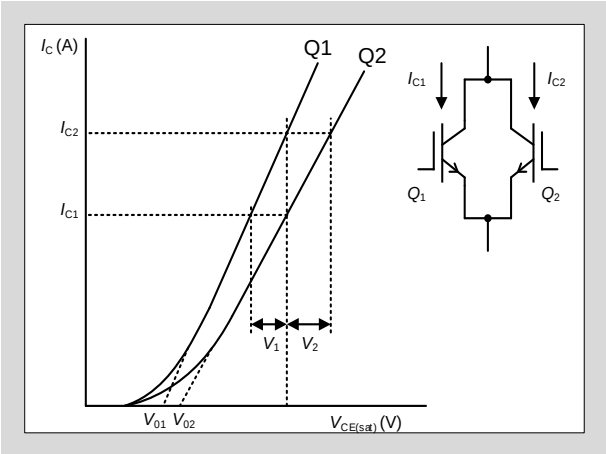



Fig. 8-1 Example of different output characteristics

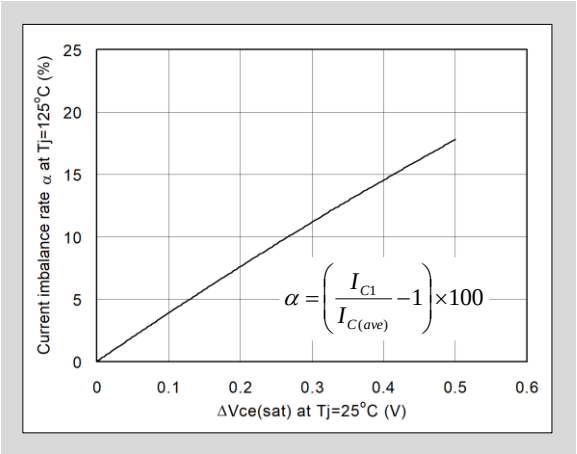



Fig. 8-2 $\Delta V_{CE(sat)}$ and current imbalance rate

### 1.2 $\Delta V_{CE(sat)}$ minimization

$\Delta V_{CE(sat)}$ can be minimized by using IGBT modules from the same product lot. This is because the influence of fabrication process, such as variations in raw materials, manufacturing, and inspection process can be minimized. Therefore, parallel connection with modules from the same product lot is recommended.

In addition, some products have $V_{CE(sat)}$ and $V_F$ values displayed on the product label, and Data Matrix code that allow $V_{CE(sat)}$ and $V_F$ to be read. Using this data, combining products with little variation is recommended. Fig. 8-3 shows the product label, and Fig. 8-4 shows an example of the Data Matrix code. For details, please refer to the specifications of each product.

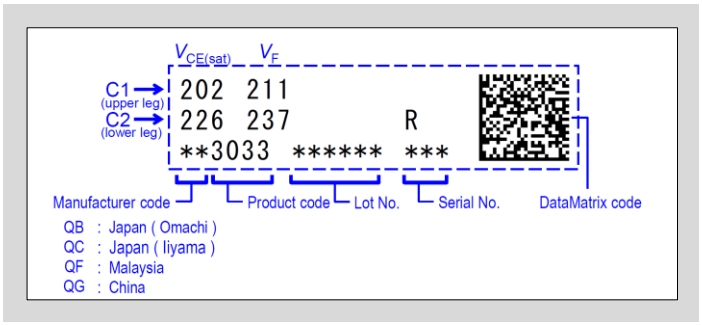



Fig. 8-3 Product label

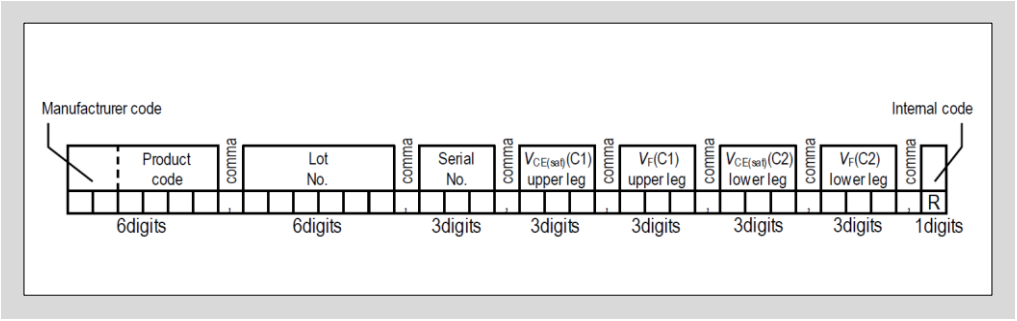



Fig. 8-4 Data Matrix code

### 1.3 $T_{vj}$ dependency of output characteristics and current imbalance

$T_{vj}$ dependency of output characteristics deeply affects current imbalance. Here, output characteristic, whose $V_{CE(sat)}$ is higher and lower with the increase of $T_{vj}$, is defined as the positive and negative $T_{vj}$ dependency, respectively. Using 100A rated IGBT as an example, Fig. 8-5 shows the output characteristics with positive and negative $T_{vj}$ dependency.

As described in section 1.1, when two IGBTs are connected in parallel, the current sharing of the IGBT with lower $V_{CE(sat)}$ increases. Therefore, steady-state power loss is larger for the IGBT with lower $V_{CE(sat)}$, and $T_{vj}$ rises more than the other IGBT. In this case, if the $T_{vj}$ dependency is positive, $V_{CE(sat)}$ increases as $T_{vj}$ increases, and the current sharing decreases accordingly. In this way, in a combination of IGBTs with positive $T_{vj}$ dependency, the current flowing through both IGBTs becomes balance due to temperature rise. On the other hand, in a combination of IGBTs with negative $T_{vj}$ dependency, $V_{CE(sat)}$ decreases as $T_{vj}$ rises, which increases the current imbalance. Therefore, when IGBTs and FWDs whose output characteristics are temperature dependent are connected in parallel, an increase in $T_{vj}$ may affect the current imbalance rate.

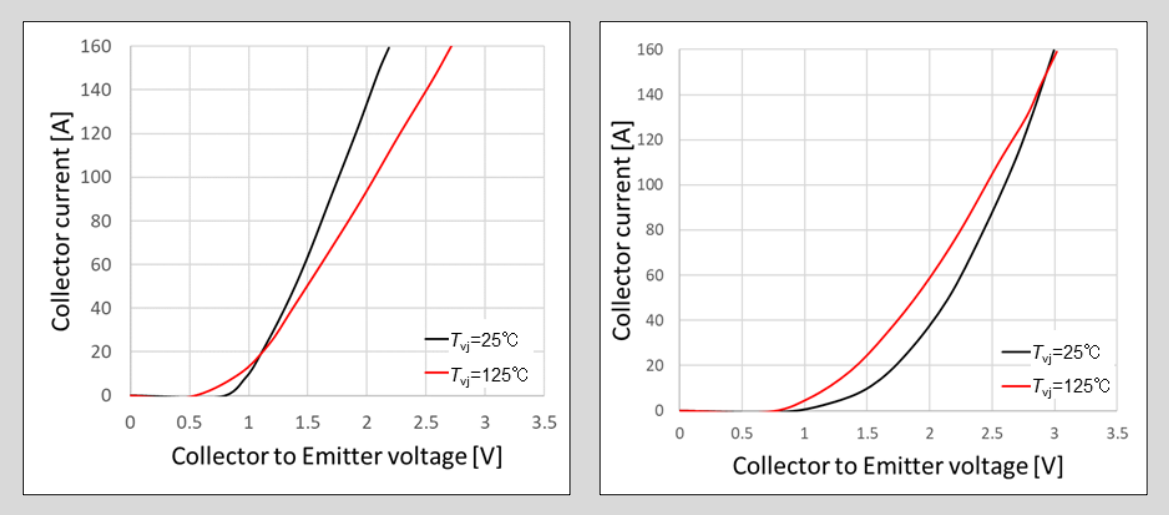



Fig. 8-5 Comparison of IGBT output characteristics
(left: positive $T_{vj}$ dependency, right: negative $T_{vj}$ dependency)

### 1.4 Derating in parallel connection with multiple of IGBTs

When IGBTs are connected in parallel, the current imbalance must be taken into consideration, and the total current (maximum current that can flow) must be derated (decrease of total current) relative to the total rated current. When n-number of IGBTs are connected in parallel, the worst condition is current concentration in the IGBT with the lowest $V_{CE(sat)}$. Therefore, the allowable maximum current Σ*I* when n-number of IGBTs are connected in parallel can be expressed by the following formula, using the current imbalance rate α when two IGBTS are connected in parallel.

$$\sum I = I_{C(max)}\left[1 + (n-1)\frac{\left(1-\frac{\alpha}{100}\right)}{\left(1+\frac{\alpha}{100}\right)}\right] \qquad \alpha = \left(\frac{I_{C1}}{I_{C(ave)}} - 1\right)\cdot 100$$

Here, the current imbalance rate α in the above formula can be obtained from the current value $I_{C1}$ and the average current value $I_{C(ave)}=(I_{C1}+I_{C2})/2$ for two parallel IGBTs as shown in Fig. 8-1. $I_{C(max)}$ is the maximum current for a single IGBT, and Σ*I* is the maximum current of the parallel connection. However, in order to operate with the maximum current Σ*I*, each IGBT connected in parallel must satisfy the RBSOA stated in the specification, and $T_{vj}$ rise caused by power loss must be kept bellow $T_{vj(max)}$ as well. Note that $T_{vj}$ rise varies depending on the operating conditions such as switching frequency, gate drive condition, cooling condition, snubber condition, etc.

The total current Σ*I* in a parallel connection requires derating with respect to the simple sum of currents (n· $I_{C(max)}$). For example, if α=15%, $I_{C(max)}$=200A and n=4, then Σ*I*=643.4A. In this case, derating of 19.6% is required from the simple sum of 200x4=800A.

Fig. 8-6 shows the IGBT derating rate when α=15%. As shown in this figure, derating rate increases as the parallel number increases. Therefore, derate the total current according to the parallel number. Note that derating rate depends on the current imbalance rate.

The derating rate shown in this example is a reference value calculated from the current imbalance rate. Please determine the derating rate after verifying the imbalance rate by actual evaluation.

If it is necessary to replace the paralleled modules due to troubles and/or maintenances, it is recommended that all the paralleled modules be replaced. In this case, it is recommended to use modules from the same production lot.

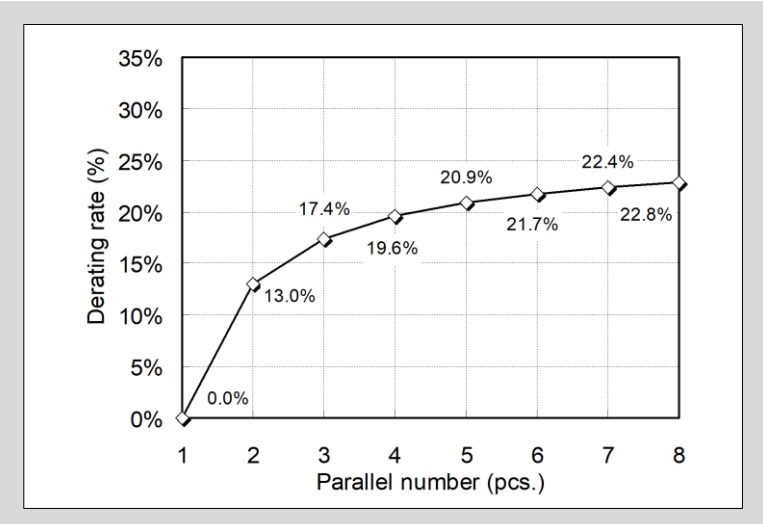



Fig. 8-6 Relationship between derating rate and parallel number

## 2. Main Circuit Design

Variation in the main circuit wiring between each IGBT module in a parallel connection has a large effect on the current imbalance during both steady-state operation and switching operation. Since this may lead to malfunction, it is necessary to keep the following two factors in mind and design the main circuit wiring symmetrically and as short as possible.

(1) Variation in main circuit wiring resistance
(2) Variation in main circuit wiring inductance

### 2.1 Variation in main circuit wiring resistance

Fig. 8-7 shows the simplified equivalent circuit of a two parallel IGBT connection showing the main circuit wiring resistance. The collector side resistance component is omitted.

If the resistance component of the main circuit wiring is large, the total collector current flowing through Q1 and Q2 will decrease compared to when the resistance component is small. The larger the resistance component, the smaller the total collector current.

In this way, the resistance component of the main circuit may cause a decrease in collector current or current imbalance. Therefore, in order to reduce this effect, the wiring on the emitter side must be as short and as symmetric as possible.

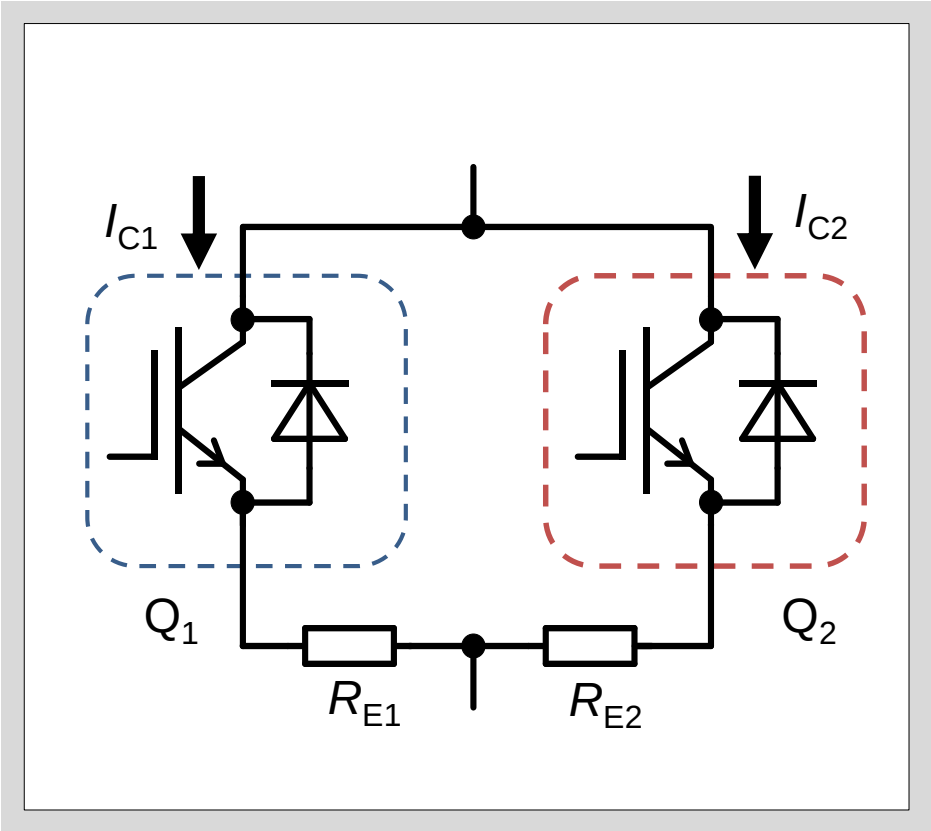



Fig. 8-7 Equivalent circuit of main circuit with wiring resistance component

### 2.2 Variation in main circuit wiring inductance

Fig. 8-8 shows the simplified equivalent circuit of a two parallel IGBT connection showing the main circuit wiring inductance. If the main circuit wiring inductance is uneven, current imbalance will occur between the IGBTs during switching. When collector currents $I_{C1}$ and $I_{C2}$ flow through IGBT Q1 and Q2, respectively, the current sharing is affected by the difference between the wiring inductances of each IGBT $L_{E1}$ and $L_{E2}$. The current sharing is mostly determined by the inductance ratio. Therefore, in order to reduce the current imbalance during switching, it is necessary to design the wiring inductance as even as possible. If the wiring inductances $L_{E1}$ and $L_{E2}$ are different, there will be difference in the induced voltage of $L_{E1}$ and $L_{E2}$ caused by d$i$/d$t$ at turn-on. The difference in induced voltage affects the effective gate voltage of each IGBT and promotes current imbalance. For this reason, in a parallel connection, it is important to design the main circuit so that $L_{E1}$=$L_{E2}$ as much as possible. Also, if the main circuit wiring inductance is large, the surge voltage at IGBT turn-off will increase. Therefore, it is necessary to design the wiring inductance as small as possible.

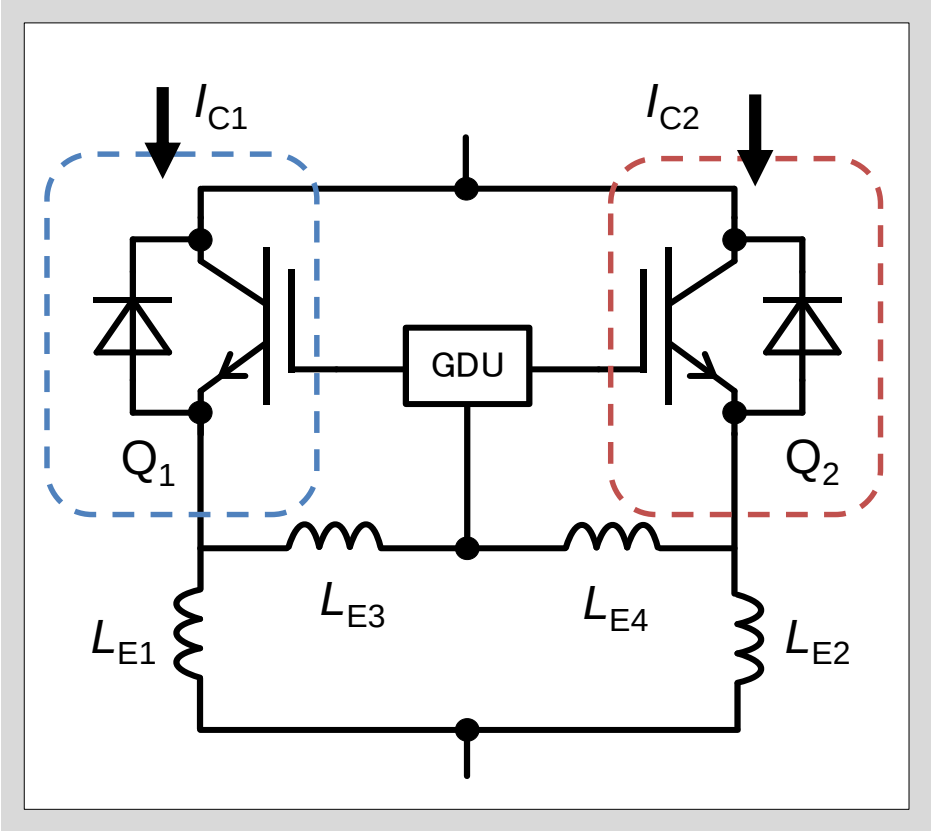



Fig. 8-8 Equivalent circuit of main circuit with wiring inductance component

### 2.3 Wiring example for parallel connection

As described above, care must be taken in the main circuit design of a parallel connection.

Fig. 8-9 shows an example of equivalent circuit when paralleling two 2-Pack modules. As shown in Fig. 8-9, all the wiring to the IGBTs (IGBT1 and IGBT2) are connected symmetrically.

Fig. 8-10 shows the switching waveforms of two 1700V/1000A 2-Pack modules connected in parallel with symmetrical wiring. As shown in this waveform, both the currents $I_{C1}$ and $I_{C2}$ flowing through each IGBT are almost equal, and the current imbalance rate is only 2%. This shows that symmetrical wiring in parallel connection can realize good current balance.

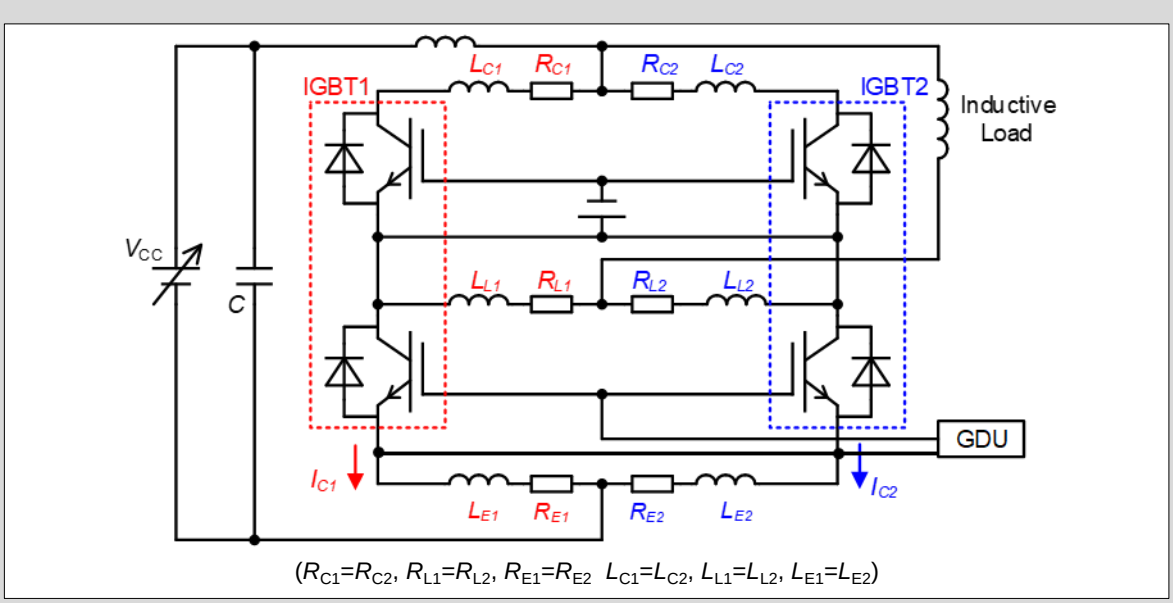



Fig. 8-9 Equivalent circuit when paralleling two 2-Pack modules

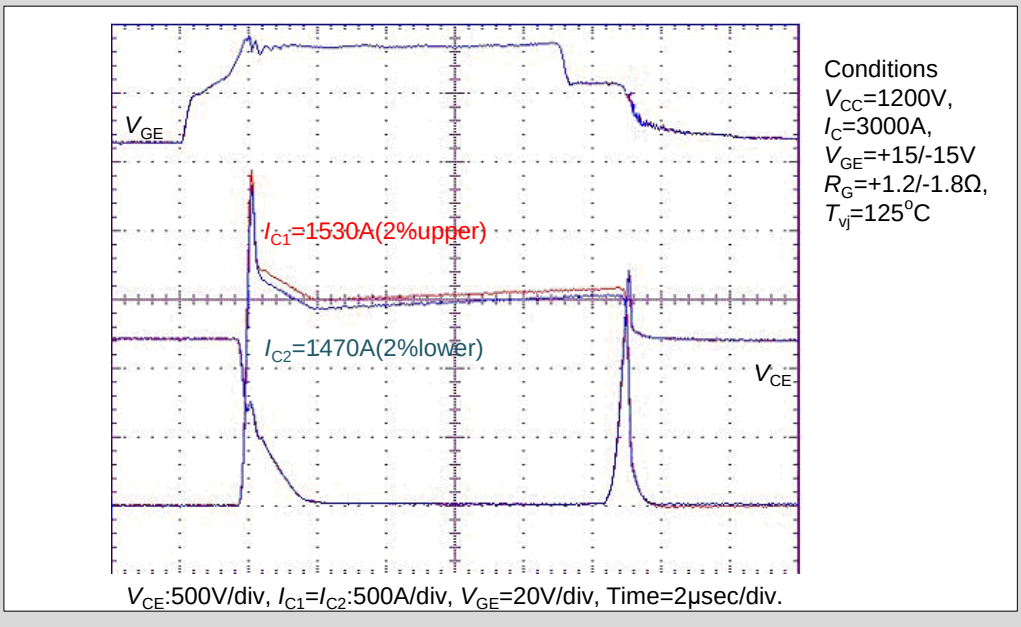



Fig. 8-10 Switching waveforms of two 1700V/1000A 2-Pack modules connected in parallel

# 3. Gate Drive Circuit Design

In addition to the contents of Chapter 7, there are other precautions when designing gate drive circuits for parallel connection of IGBT modules. Also, there are different precautions depending on the gate driver configuration for parallel connection. If these precautions are not taken into consideration, the gate drive circuit may cause current imbalance or malfunction, possibly destroying the IGBT modules. The main precautions when designing gate drive circuits for parallel connections are described as follows.

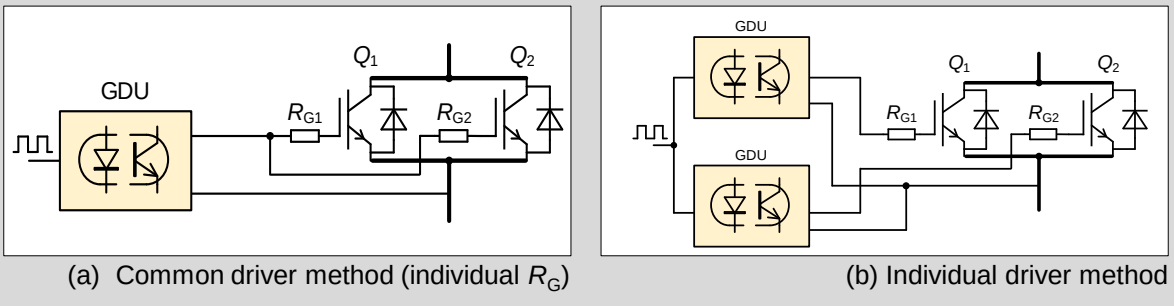
## 3.1 Connection of gate drive circuit to gate-emitter terminal

When driving parallel connected IGBTs, if the IGBT module has auxiliary emitter terminal, use the auxiliary emitter terminal to drive the IGBT. If there is no auxiliary emitter terminal, and the emitter wiring of the gate drive circuit is connected at a position where the wiring inductances $L_{E1}$ and $L_{E2}$ as shown in Fig. 8-8 are uneven, the gate voltage of each IGBT during switching will differ, resulting in unbalanced transient current sharing. Normally, IGBT modules such as 2-Pack have auxiliary emitter terminal for the gate drive circuit. Using this terminal will realize balanced $L_{E1}$ and $L_{E2}$, thus transient current imbalance can be suppressed.

However, even if auxiliary emitter terminal is used to drive the IGBT, if the emitter wiring from the gate drive circuit to each IGBT module is long and uneven, current imbalance will occur. Therefore, it is important to design the gate drive circuit wiring to each IGBT with equal length, as short as possible, and symmetrical. The gate drive circuit wiring should be twisted, and kept as far away from the main circuit wiring as possible and not parallel to each other.

## 3.2 Precautions when designing gate drive circuits for parallel connections

There are several gate drive circuit methods for parallel connection of IGBT modules, and precautions differ depending on the gate driver configuration. As example of gate drive circuit configuration for parallel connection, Fig. 8-11(a) shows the common driver method (a configuration in which one gate driver drives all the IGBTs), and Fig. 8-11(b) shows the individual driver method (a configuration in which each IGBT is driven by individual gate drivers equal to the number of parallel IGBTs). Details of these two types of gate drive circuits and their design considerations are described in the following pages.




(a) Common driver method (individual $R_G$)　　(b) Individual driver method

Fig. 8-11 Gate drive circuit configuration for parallel connection

### 3.2.1 Common driver method

A feature of the common driver method is that the power supply and optocoupler that drive each IGBT can be shared, thus the gate drive circuit can be simplified and the number of components can be reduced. On the other hand, driving multiple IGBTs connected in parallel with a single power supply requires a large power supply capacity.

In addition, the emitters of each parallel IGBT are common within the gate drive circuit, creating a closed loop which may generate gate voltage fluctuations during switching and cause the IGBTs to malfunction. As example, a turn-on waveform with parasitic oscillation is shown in Fig. 8-12, and the mechanism of the parasitic oscillation is shown below. If the wiring inductances $L_{E1}$ and $L_{E2}$ as shown in Fig. 8-8 are uneven, the difference in wiring inductance and the input capacitance of the IGBT will generate a cross current, which will generate electromotive force in $L_{E3}$ and $L_{E4}$, resulting in parasitic oscillation of the gate voltage.

As countermeasures, consider inserting a common mode choke in the gate circuit or a resistor $R_E$ on the emitter side, and confirm that the problem described above does not occur.

Mechanism of parasitic oscillation during turn-on in common driver method

(a) When IGBTs Q1 and Q2 turns on, $I_C$ increases and d$i$/d$t$ occurs in the main circuit. As a result, electromotive forces $V_{LE1}$ and $V_{LE2}$ are generated in the wiring inductances.

(b) When there is a difference in the wiring inductances, the magnitude of electromotive forces $V_{LE1}$ and $V_{LE2}$ will be different, generating a cross current $i_N$ in the closed loop.

(c) Electromotive forces $V_{LE3}$ and $V_{LE4}$ are generated in the wiring inductances between the GDU and the emitter $L_{E3}$ and $L_{E4}$ by this cross current $i_N$, and parasitic oscillation of the gate voltage is generated by the charging and discharging currents to Q1 and Q2.

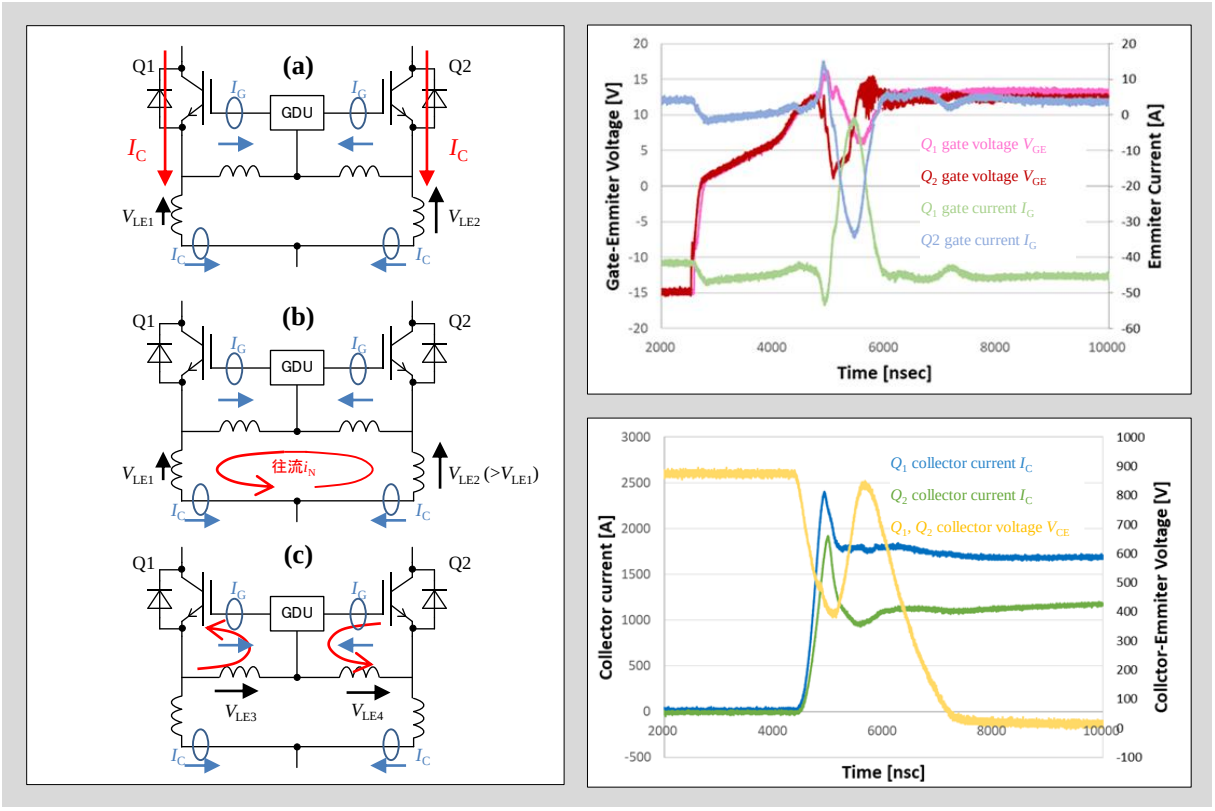



Fig. 8-12 Parasitic oscillation mechanism and turn-on waveforms

### 3.2.2 Individual driver method

A feature of the individual driver method is that the emitters of the parallel IGBTs are not common. In this case, a closed loop is not formed thus there will no cross current at the emitter, and risk of malfunction such as parasitic oscillation shown in Fig. 8-12 is reduced. On the other hand, arranging individual gate drive circuits for each parallel IGBT modules complicates the gate drive circuit. In addition, due to variations in the characteristics of electronic components such as optocouplers, each parallel IGBT has a difference in turn-on/turn-off timing, which may cause current imbalance or malfunction during switching. Therefore, when designing gate drive circuit for the individual driver method, it is necessary to minimize the difference in timing between turn-on and turn-off of each IGBT by considering the characteristics variation of electronic components.

### 3.2.3 Gate resistor configuration in common driver method

As shown in Fig. 8-13, there are three methods for configuring the gate resistor $R_G$ in the common driver method.

In the case of the individual gate resistor method as shown in Fig. 8-13(a), the $R_G$ connected to each IGBT can suppress the parasitic oscillation caused by the circuit inductance of the gate circuit wiring and the input capacitance of the IGBT. However, even if each IGBT is connected to the same driver IC, variations in the $R_G$ can cause differences in the turn-on/turn-off timing of each IGBT during switching, which may cause current imbalance or malfunction.

In the case of the common gate resistor method as shown in Fig. 8-13(b), there will be no difference in the $R_G$ value of each IGBT, so the difference in turn-on/turn-off timing of each IGBT can be minimized. However, due to LC resonance of the gate drive circuit wiring inductance and the input capacitance of the IGBT, parasitic oscillation may occur when the gate voltage rises.

If no parasitic oscillation or IGBT turn-on/turn-off timing difference is observed, it is possible to apply the common gate resistor method or the individual gate resistor method. However, when designing a new gate drive circuit, it is recommended to apply the combination gate resistor method as shown in Fig. 8-13(c), which combines the characteristics of both common gate resistor method and the individual gate resistor method.

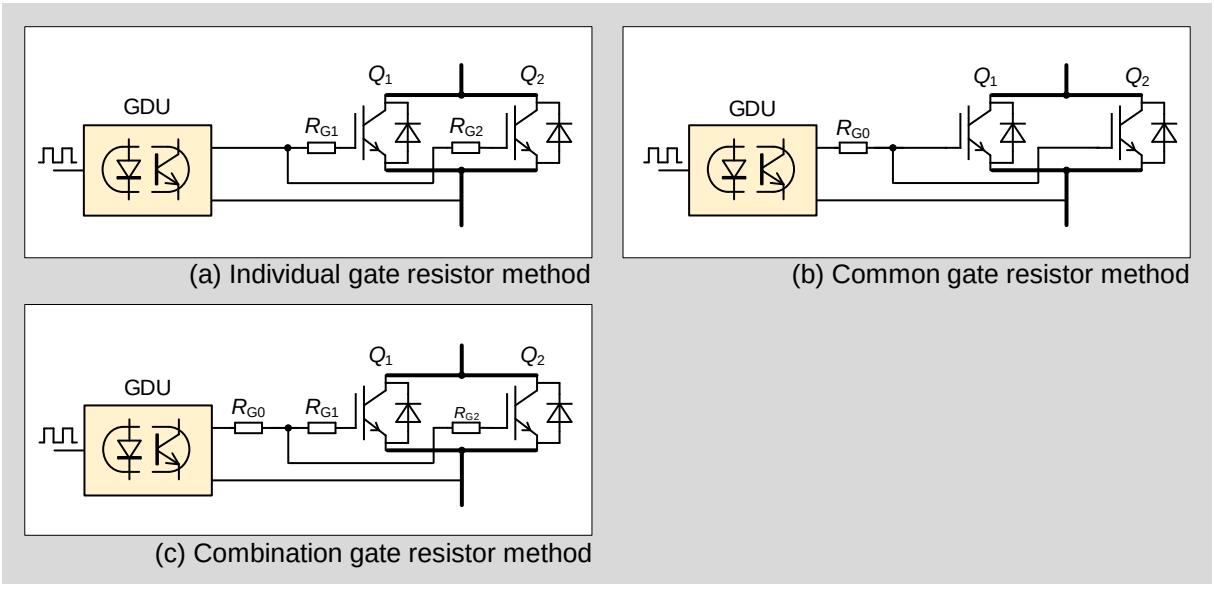



Fig. 8-13 Gate resistor configuration in common driver method

## 4. Cooling Design

When connecting IGBT modules in parallel, it is necessary to consider the thermal interference of each IGBT module. If the junction temperature $T_{vj}$ increases due to thermal interference, the junction temperature absolute maximum rating $T_{vj(max)}$ may be exceeded and cause thermal destruction of the IGBT modules. Therefore, it is necessary to consider the thermal interference between each module and design the modules layout to reduce $T_{vj}$. The points to consider regarding cooling design in parallel connection are shown below.

(1) Layout design considering thermal interference between each module.
(2) Equalize cooling conditions for each module.
(3) Uniform thermal grease thickness applied to each module.

Especially for (1), simulation of thermal interference when adjusting the spacing between two parallel IGBT modules (2MBI1400VXB-170P-50) on the same heat sink is conducted. Fig. 8-14 shows the simulation result. In the case of equidistant layout (where each IGBT module is centered between the centerline and edge of the heatsink), the temperature rise $\Delta T_{v(j-a)}$ is lowest. Therefore, in order to minimize the thermal interference of each IGBT module, it is effective to design a layout in which the heat sink area is evenly divided by the number of IGBT modules, and each module is placed in the center of each area.

On the other hand, if the size of the heat sink is increased as the IGBT module spacing is increased, the thermal interference between each IGBT module can be further reduced. However, in this case, the wiring inductance $L_S$ of the main circuit increases, which increases the surge voltage $V_{CEP}$ at turn-off, and the IGBT module may be destroyed by overvoltage.

Therefore, consider the trade-off between thermal interference of each IGBT module and increase of surge voltage, and design an appropriate cooling system.

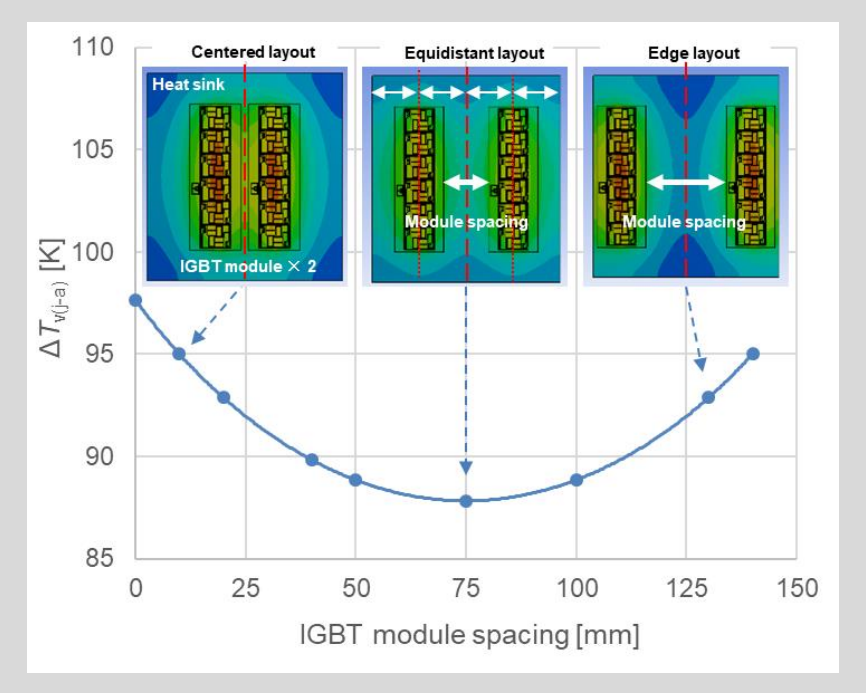



Fig. 8-14 $\Delta T_{v(j-a)}$-IGBT module spacing dependency