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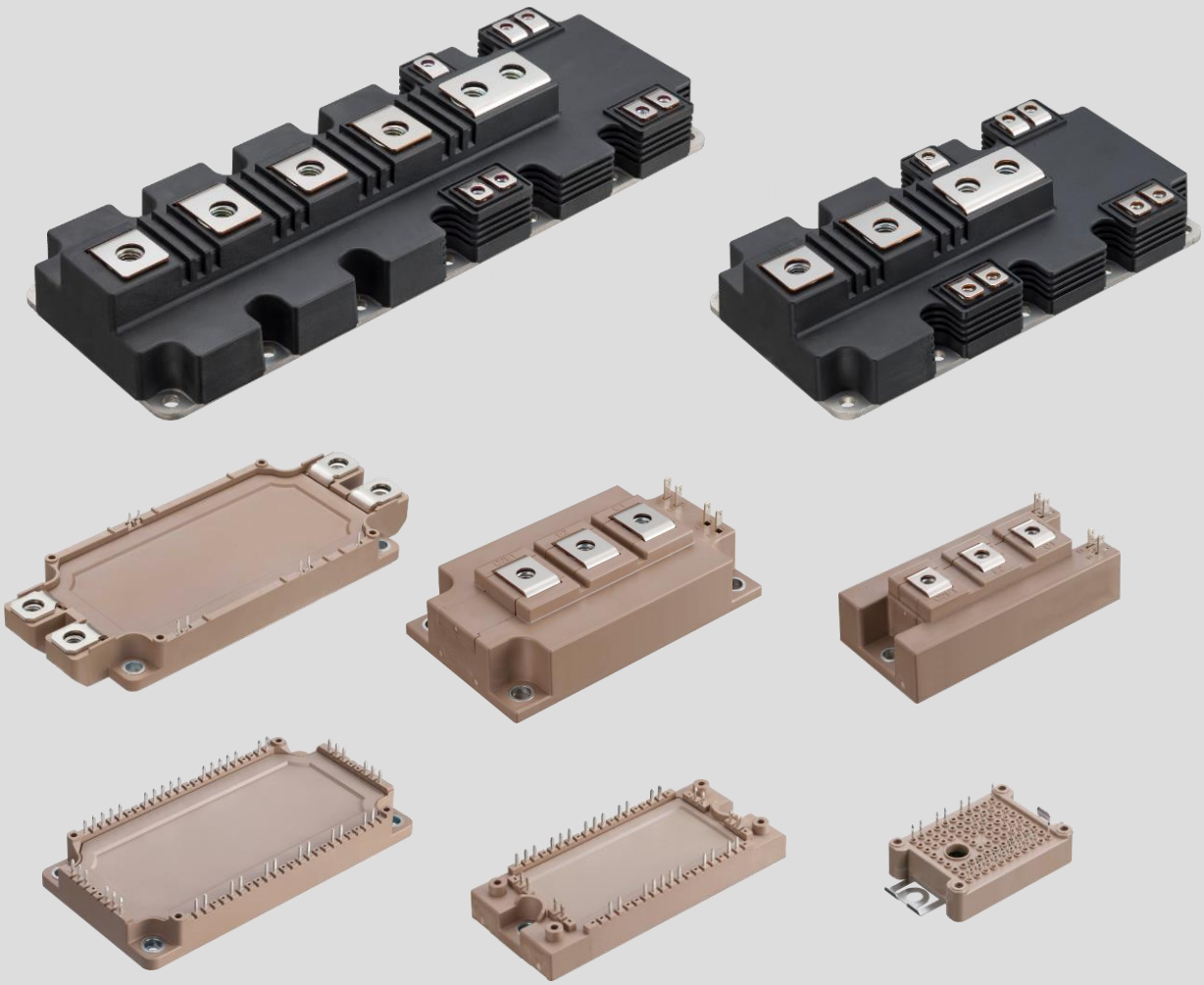

Fuji IGBT Module

Application Manual

March, 2023

Fuji Electric Co., Ltd.

REH984f

⚠ Cautions

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Contents

Chapter 1 Structure and Features

The insulated gate bipolar transistors (IGBTs), applied to equipment such as variable-speed motor drives and uninterruptible power supplies for computers, are developing rapidly in response to the increasing demand for energy saving, weight reduction, and downsizing of equipment in recent years. The IGBT is a switching device designed to have the high-speed switching performance and gate voltage control of a power MOSFET as well as the high-voltage / large-current handling capability of bipolar transistor.

1. History of IGBT Structure

The n-channel IGBT, which forms a n-type inversion layer when positive voltage is applied to the gate, has a structure in which the n+ layer on the drain side of the power MOSFET is replaced with a p+ layer. It is a bipolar device that can reduce on-resistance at large current with conductivity modulation.

The IGBT structure can be roughly divided into the surface gate structure, the bulk structure that forms the n-drift layer, and the backside structure. There are two types of surface gate structures. One is the planar gate structure, in which the gates are formed on the wafer surface, namely the chip surface. The other is the trench gate structure, in which trenches are made to form the gates in the wafer. On the other hand, the bulk structure can be roughly divided into the punch-through type, in which the depletion layer reaches the collector side at turn-off, and the non-punch-through type, in which it does not reach the collector side. The comparison of the n-channel IGBTs is shown in Fig. 1-1.

Fuji Electric has been supplying IGBTs to the market since it commercialized them in 1988. The planar-gate punch-through IGBT was the mainstream IGBT at that time. The punch-through IGBT used the epitaxial wafer and low on-state voltage was achieved by injecting a large amount of minority carriers from the collector layer to obtain conductivity modulation effect. At the same time, the lifetime control technology was used because the excess carriers, which were high-injected into the n-base layer, has to be removed quickly at turn-off. As a result, both low on-state voltage and low turn-off switching loss (E_{off}) were achieved. The lifetime control technology was widely used because it was relatively easy to apply into the IGBT manufacturing process. However, there were problems such as large variations in on-state voltage and the output characteristics showing negative temperature characteristics. Therefore, with the increasing capacity of IGBT modules and the power converters using them, the demand for IGBT characteristics that facilitate parallel connection has increased.

The non-punch-through IGBT was developed to overcome these issues. The non-punch-through IGBT controls the minority carrier injection efficiency by controlling the concentration of impurities in the collector (p-collector layer), and controls the internal electric field and transport efficiency by controlling the thickness and resistivity of the n-drift layer. The non-punch-through IGBTs use the FZ (Floating Zone) wafer instead of the epitaxial wafer. Therefore, the superiority of the FZ wafer compared to the epitaxial wafer can be reflected in the IGBT chip. For example, FZ wafers have less crystal defects and low internal stress, making it easy to manufacture high voltage chips of 1700V and above. In addition, the carrier lifetime of FZ wafers is very long, and the excess carrier distribution control of the IGBT chip only needs to consider minority carrier injection from the p-collector layer. Furthermore, variations in characteristics such as on-state voltage are greatly reduced.

On the other hand, in order to achieve a low on-state voltage, it was necessary to improve the transport efficiency. In particular, IGBT wafers with a withstand voltage of 1200V or less required a special manufacturing technology to thin the n-drift layer. Therefore, Fuji Electric has developed new technologies for production of thinner wafers and improved the characteristics.

To further improve the characteristics, IGBTs with thinner chip thickness are required. However, the thickness of the n-drift layer constitutes most of the chip thickness, and if the thickness is too thin, the specified voltage cannot be maintained. The FS (Field Stop) structure solved this problem that hinder the improvement of the characteristics. In the FS structure, a high concentration FS layer is provided in the n-drift layer. This structure makes it possible to further reduce the thickness of the chip and improve its characteristics.

Fuji Electric has also advanced the miniaturization of the surface structure that is imperative to improve the characteristics of IGBT. The IGBT is formed by arranging many basic structures called cells. The higher the number of IGBT cells, the lower the on-state voltage will be. In order to increase cell density, the surface structure has changed from the planar structure, in which the IGBT cells are formed on the wafer surface two-dimensionally, to the trench structure, in which the trenches are formed on the wafer surface and the gates structure are formed three-dimensionally. In this way, Fuji Electric has improved the characteristics by applying various technologies to the bulk structure and the surface structure.

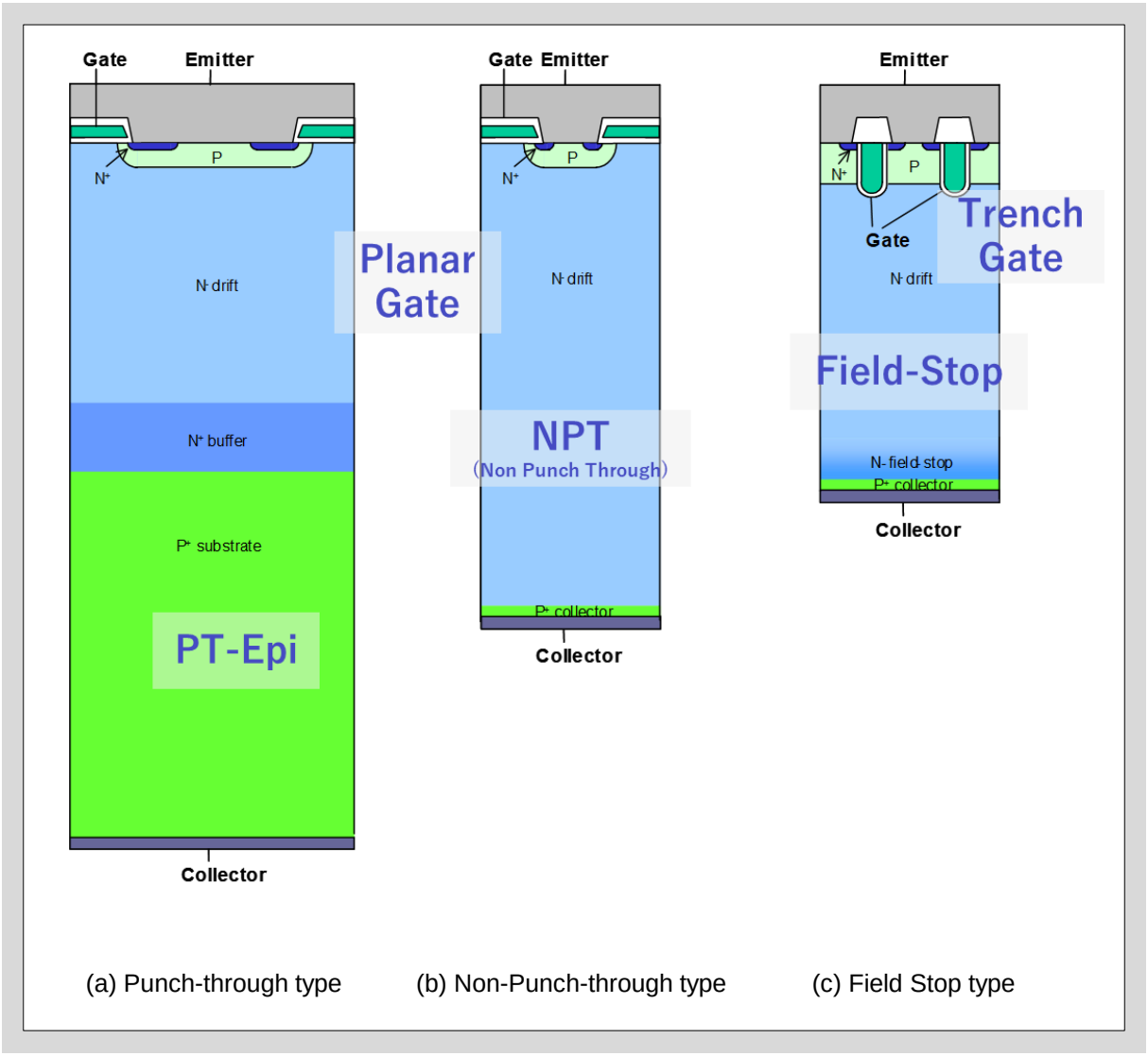


Fig. 1-1 Structure comparison of IGBT

2. Module Structure

Fig. 1-2 and Fig. 1-3 show typical IGBT module structures. The module integrated with terminal block shown in Fig. 1-2 has a case and external electrode terminals molded into a single unit to reduce the number of parts required and the internal wiring inductance. In addition, the use of DCB (direct copper bonding) substrate realizes a high-reliability product that combines low thermal resistance and high bending strength.

The wire terminal connection structure module shown in Fig. 1-3 has main terminals bonded to the DCB substrate by wire. As a result, the package structure has been simplified, made smaller, thinner, lighter, and reduced in assembly time.

Other design considerations implemented include optimal IGBT and FWD chips layout to assure efficient heat distribution, and the equal arrangement of IGBT chips in the upper and lower arms to balance the turn-on transient current and thus prevent the increases in turn-on loss.

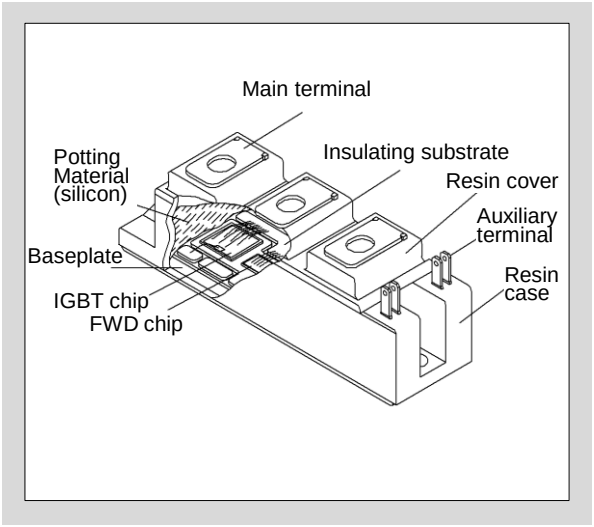


Fig. 1-2 Integrated with terminal block type

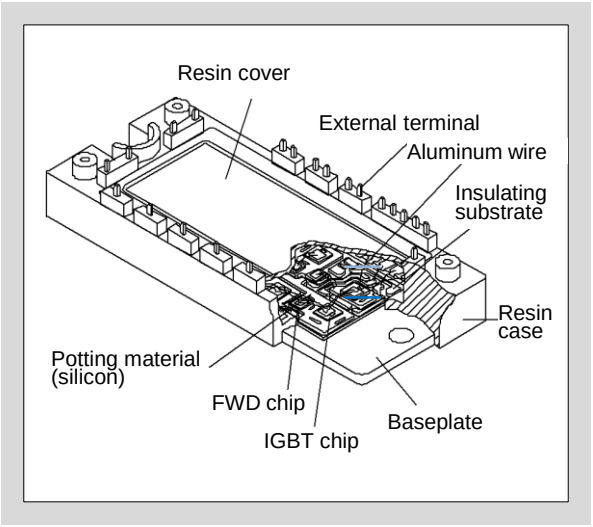
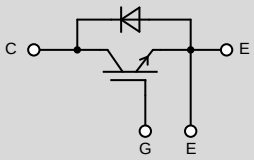
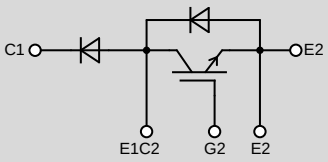
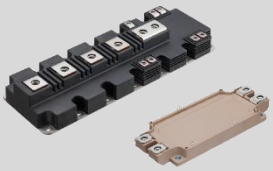
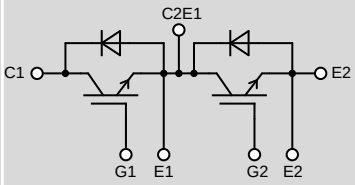
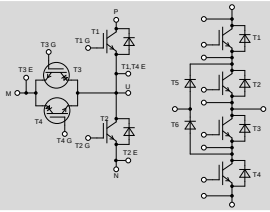
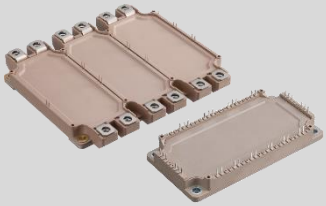
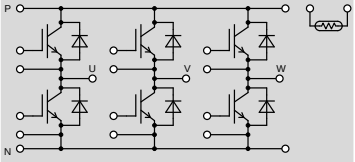
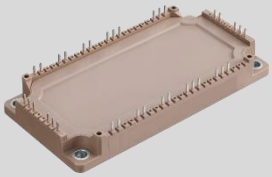
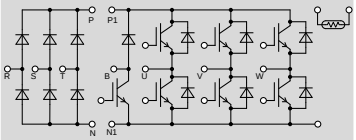


Fig. 1-3 Wire terminal connection structure type

3. Circuit Configuration of IGBT Module

Table 1-1 shows typical circuit configuration of IGBT modules. As shown in Table 1-1, there are basically four types of IGBT modules: 1-Pack, 2-Pack, 6-Pack, and PIM. Each type has its own features. The circuit configuration is also shown. Use them as reference when selecting a module.

Table 1-1 Circuit configuration of IGBT modules

Type	Example of IGBT module		Feature
	External view	Equivalent circuit	
1-Pack			Module which contains one IGBT and one anti-parallel FWD. Modules with high current rating are often connected in parallel in large capacity applications.
Chopper			Module which a FWD is connected in series to an IGBT and its anti-parallel FWD. For application in brake for PWM inverter. I-type 3-level circuit can be configured by combining with 2-Pack.
2-Pack			Module which contains two sets of IGBT and its anti-parallel FWD. Generally 3 modules are used to configure a PWM inverter. Products with high current rating are often connected in parallel in large capacity applications.
3 Level			Module consisting of IGBTs and FWDs arranged in T-type or I-type. It is generally used for solar inverters. Also, modules are often connected in parallel in large capacity applications.
6-Pack			Each module contains six sets of IGBT and its anti-parallel FWD. Module with built-in NTC thermistor for temperature detection is also available. It is common to configure a PWM inverter with a single module.
PIM			A module with built-in converter, inverter, and brake. Module with built-in NTC thermistor for temperature detection is also available.

4. Overcurrent Limiting Feature

During operation, a load short circuit or similar problem may cause overcurrent in the IGBT. If the overcurrent is allowed to continue, the device may quickly overheat and be destroyed. Generally, the time span from the beginning of the overcurrent to the destruction of the device is called the “short circuit withstand capability”. In addition, short circuit withstand capability becomes higher (longer) in condition with lower short circuit current and/or lower power supply voltage. In other words, the smaller the short circuit energy, the higher the short circuit withstand capability.

The short circuit current is dependent on the gate voltage. The IGBT is designed to limit the short circuit current to several times of the device current rating. Thus, in the event of a short circuit, the overcurrent is limited, allowing protection to be applied with a margin after overcurrent is detected.

5. RoHS Compliance

The RoHS (Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) was enacted by the EU (European Union) on July 1, 2006 to restrict the use of certain hazardous substances in electrical and electronic equipment.

The use of the following ten substances are restricted: Pb (lead), Cd (cadmium), Cr6+ (hexavalent chromium), Hg (mercury), PBB (polybrominated biphenyl), PBDE (polybrominated diphenyl ether), DEHP (bis (2-ethylhexyl) phthalate), BBP (butyl benzyl phthalate), DBP (dibutyl phthalate) and DIBP (diisobutyl phthalate).

Products containing these 10 substances above the threshold (0.01% for Cd, 0.1% for others) cannot be sold in the EU.Exemptions are allowed for uses that are technically difficult to replace.

Lead (Pb) contained in the solder used to connect each chip and DCB is particularly relevant to the RoHS compliance of IGBT modules. Fuji Electric uses Pb-free solder to commercialize products that comply with RoHS regulations.

6. Standards for Safety: UL Certification

When using various devices in the market in regions that require compliance with UL safety regulations such as North America, UL certification is required for the parts used in those devices.

Fuji Electric IGBT modules comply with UL1557 and are certified. The approved models can be checked in the following website.

https://productiq.ulprospector.com/en/profile/1972723/qqqx2.e82988?term=E82988&page=1

A list of Fuji Electric products which is currently UL certified is displayed.

Chapter 2 Terms and Characteristics

This chapter describes the terms and characteristics of IGBT modules.

1. Explanation of Terms

Various terms used in the specifications are explained below.

Table 2-1 Maximum ratings

Term	Symbol	Definition explanation (Refer to specifications for test conditions)
Collector-Emitter voltage	V_{CES}	Maximum Collector-Emitter (hereinafter referred to as C-E) voltage with Gate-Emitter (G-E) shorted.
Gate-Emitter voltage	V_{GES}	Maximum G-E voltage with C-E shorted.
Collector current	I_C	Maximum DC collector current of IGBT.
	I_{CRM} I_C pulse	Maximum pulse collector current of IGBT.
Forward current	$-I_C$	Maximum DC forward current of FWD.
	I_{FRM} $-I_C$ pulse	Maximum pulse forward current of FWD.
Total power dissipation	P_{tot} P_C	Maximum power dissipation per IGBT.
Virtual junction temperature	T_{vj} T_j	Maximum junction temperature at which normal operation is possible. You must not exceed this temperature under the worst condition.
Operating virtual junction temperature	$T_{vj(op)}$ T_{vjop}	Junction temperature during continuous operation.
Case temperature	T_C	Case temperature directly below the IGBT chip or FWD chip that generates the most heat inside the IGBT module. (refer to Chapter 6 for details.)
Storage temperature	T_{stg}	Temperature range allowing storage or transportation without being subjected to electrical load.
FWD I^2t	I^2t	Joule-integral value of overcurrent allowed that does not result in diode destruction. The overcurrent is defined by a line frequency half sine wave (50, 60Hz) at one cycle.
FWD surge forward current	I_{FSM}	The maximum value of overcurrent allowed that does not result in diode destruction. The overcurrent is defined by a line frequency half sine wave (50, 60Hz).
Isolation voltage	V_{iso}	Maximum sinusoidal voltage RMS value allowed between all shorted terminals and the heat sink mounting surface.
Screw torque	Mounting	Maximum allowable torque value when mounting the IGBT module on a heat sink with the specified screws
	Terminal	Maximum allowable torque value when connecting external busbar or wires to the terminals with the specified screws

Note 1: Values at T_C = 25 °C unless otherwise specified
Note 2: The values listed as maximum ratings should not be exceeded under any circumstances.

Table 2-2 Electrical characteristics

Term		Symbol	Definition explanation (Refer to specifications for test conditions)
Static characteristics	Zero gate voltage collector current	I_{CES}	Collector current when a specific voltage is applied between C-E with G-E shorted.
	Gate-Emitter leakage current	I_{GES}	Gate current when a specific voltage is applied between G-E with C-E shorted.
	Gate-Emitter threshold voltage	$V_{GE(th)}$	G-E voltage (V_{GE}) at a specified I_C and C-E voltage.
	Collector-Emitter saturation voltage	$V_{CE(sat)}$	C-E voltage at a specified collector current and G-E voltage.
	Input capacitance	C_{ies}	G-E capacitance when a specified voltage is applied between G-E and C-E while C-E is shorted in AC.
	Output capacitance	C_{oes}	C-E capacitance when a specified voltage is applied between G-E and C-E while G-E is shorted in AC.
	Reverse transfer capacitance	C_{res}	C-G capacitance when a specified voltage is applied between G-E and C-E while G-E and C-E are shorted in AC.
	Forward voltage	V_F	Forward voltage of FWD at a specified forward current.
Dynamic characteristics	Turn-on time	t_{on}	The time during IGBT turn-on when V_{GE} rises from 10% of the maximum value until collector current rises to 90% of the maximum value.
	Rise time	t_r	The time during IGBT turn-on when the collector current rises from 10% to 90% of the maximum value.
	Turn-off time	t_{off}	The time during IGBT turn-off when V_{GE} drops from 10% of the maximum value until collector current drops to 10% of the maximum value.
	Fall time	t_f	The time during IGBT turn-off when the collector current drops from 90% to 10% of the maximum value.
	Turn-on loss	E_{on}	Loss generated during IGBT turn-on.
	Turn-off loss	E_{off}	Loss generated during IGBT turn-off.
	Reverse recovery loss	E_{rr}	Loss generated during FWD reverse recovery.
	Reverse recovery time	t_{rr}	Time required for FWD reverse recovery current to disappear.
	Reverse recovery current	I_{rr} (I_{rp})	Peak reverse current during reverse recovery.
Reverse bias safe operating area		RBSOA	Current and voltage range where IGBT can be turned off safely under specified conditions.
Internal gate resistance		r_g $R_{g(int)}$	Built-in gate series resistance.
Gate charge		Q_g	Amount of charge required to turn-on the IGBT.

Note 1: The definition of dynamic characteristics differs between series. For details, refer to the specifications of each product.

Table 2-3 Thermal resistance characteristics

Term	Symbol	Definition explanation (Refer to specifications for test conditions)
Thermal resistance	$R_{th(j-c)}$	Thermal resistance between the chip (junction)and case of IGBT or FWD.
	$R_{th(c-s)}$	Thermal resistance between the case and heat sink when the IGBT module is mounted on a heat sink with the recommended torque and thermal grease.

Table 2-4 Thermistor characteristics

Term	Symbol	Definition explanation (Refer to specifications for test conditions)
Thermistor resistance	R	Thermistor resistance at specified temperature
B value	B	Value indicating the magnitude of thermistor resistance change between any two temperatures in resistance-temperature characteristics.

2. Characteristics of IGBT and FWD

Using the 6MBI100VB-120-50 (1200V/100A, 6th generation IGBT module) as an example, the various characteristics of the IGBT described in the specifications are explained below.

2.1 Static characteristics

Fig. 2-1 and Fig. 2-2 show the V_{GE} dependence of V_{CE}-I_C characteristics (output characteristics). While the IGBT is on, V_{CE} changes in accordance with I_C, V_{GE}, and T_{vj}. V_{CE} represents the C-E voltage drop during the ON state, and is used to calculate the power dissipation loss of the IGBT. The smaller the V_{CE} value, the lower the power dissipation loss.

It is generally recommended to operate at V_{GE}=15V, and the collector current lower than the module current rating.

Fig. 2-3 shows the data in Fig. 2-1 as I_C dependence of V_{CE}-V_{GE} characteristics. From the graph, the V_{GE} value limit where V_{CE} suddenly increases can be read.

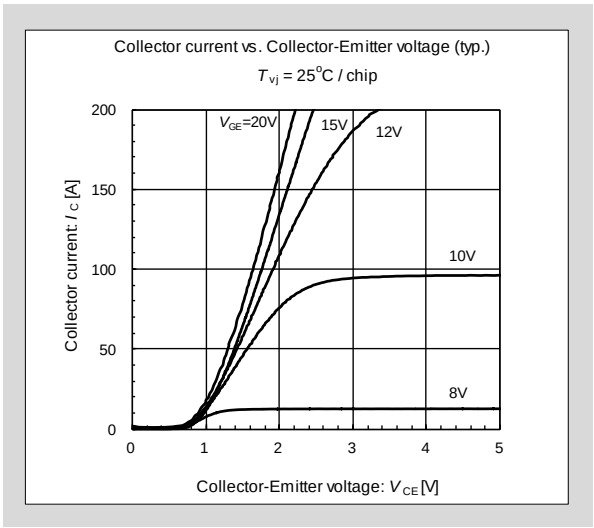


Fig. 2-1 $V_{CE(sat)}$ - I_C characteristics (T_{vj}=25°C)

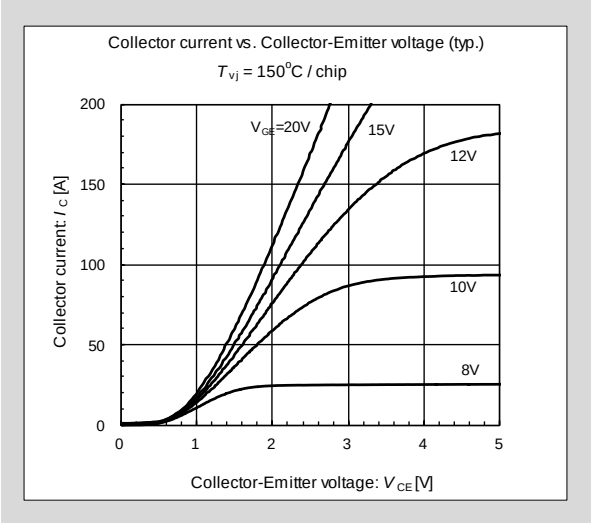


Fig. 2-2 $V_{CE(sat)}$ - I_C characteristics (T_{vj}=150°C)

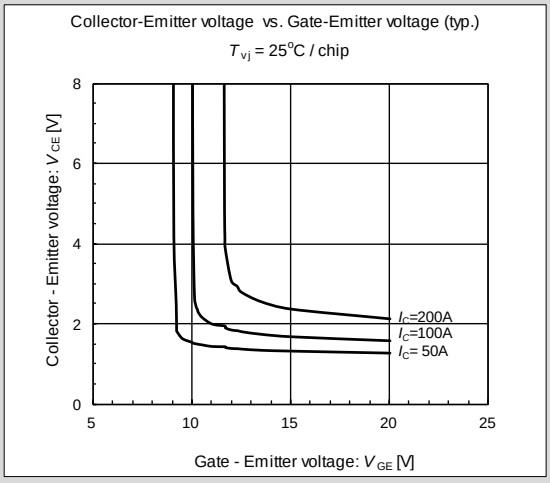


Fig. 2-3 V_{CE} - V_{GE} characteristics (T_{vj}=25°C)

2.2 Switching characteristics

As the IGBT is generally used for switching applications, it is important to fully understand the turn-on and turn-off switching characteristics. Since these characteristics are affected by various parameters, it is necessary to take these into consideration when determining operating conditions.

Switching characteristics can be divided into switching time and switching loss. These switching characteristics can be measured by the chopper circuit shown in Fig. 2-4.

The definitions of switching times are shown in Fig. 2-5.

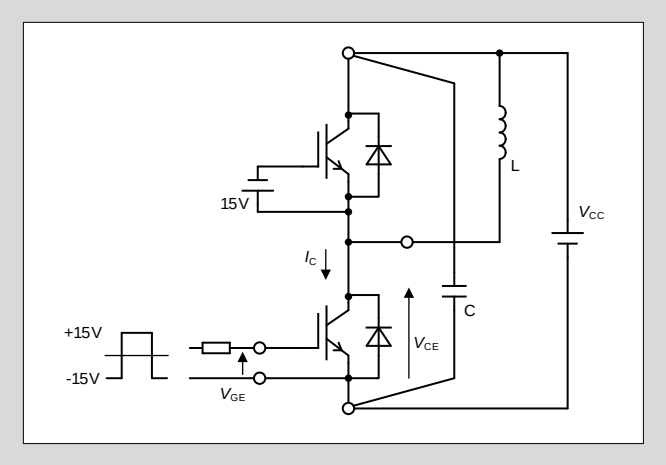


Fig. 2-4 Switching characteristics measuring circuit

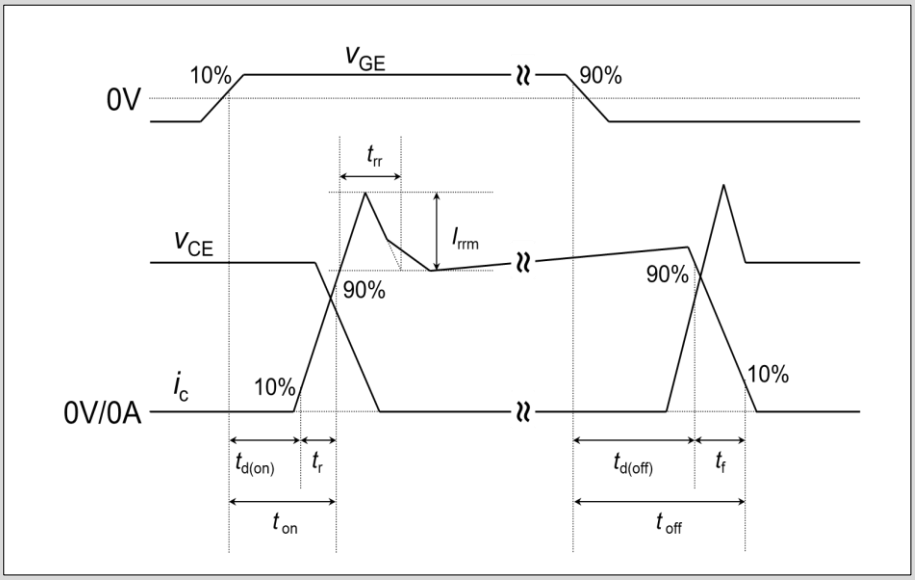


Fig. 2-5 Definition of switching time

The relationship between switching time and collector current I_C is shown in Fig. 2-6 and Fig. 2-7. Fig. 2-8 shows the relationship between switching time and gate resistance R_G. As shown in these figures, the switching time varies depending on I_C, T_{vj}, and R_G, so please take this into consideration when designing equipment.

For example, when the IGBT is used under the condition that t_{off} is too long, it may exceed the dead time and cause a series arm short-circuit.

It is also important to be aware that if the switching time, such as t_f is too short, the transient current change rate dI_c/dt will increase and may cause a high turn-off surge voltage ($=L_S \cdot dI_C/dt$). Since this surge voltage is superimposed on the applied voltage, the resulting voltage might exceed RBSOA and destroy the IGBT (refer to Chapter 2 and 4 for details).

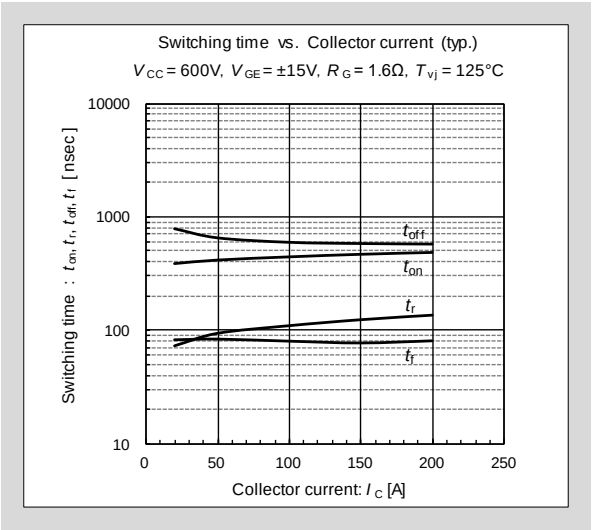


Fig. 2-6 Switching time - I_C characteristics (T_{vj}=125ºC)

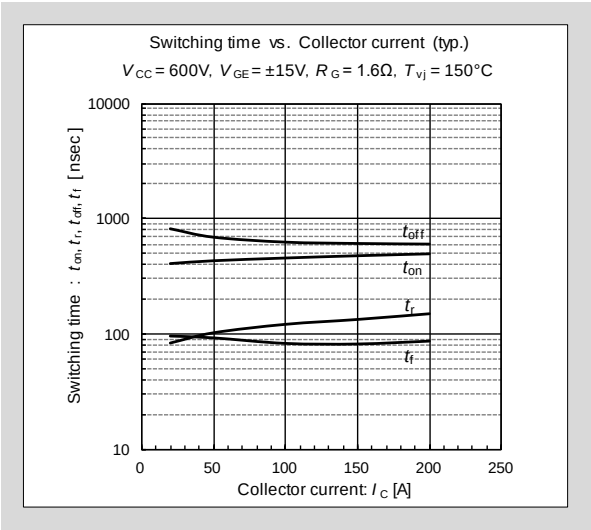


Fig. 2-7 Switching time - I_C characteristics (T_{vj}=150ºC)

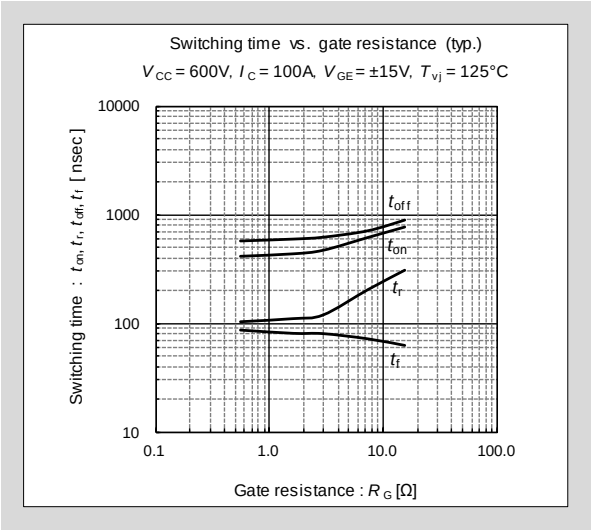


Fig. 2-8 Switching time - R_G characteristics (T_{vj}=125ºC)

Switching loss (E_{on}, E_{off}, E_{rr}) occurs every time an IGBT is turned on or off, therefore it is important to minimize this loss as much as possible. As shown in Fig. 2-9 and 2-10, switching loss changes in accordance with I_C, T_{vj}, and R_G. In particular, the selection of R_G is important. If it is too large, the switching loss will increase, and series arm short circuit due to the aforementioned insufficient dead time will easily occur. Conversely, if R_G is reduced to reduce switching loss, the aforementioned excessive surge voltage ($=L_S \cdot dI_C/dt$) may occur.

As can be seen from this, the value of main circuit inductance L_S has great influence on R_G selection. The smaller the value is, the smaller the surge voltage will be, making it easier to consider R_G selection. Therefore, it is recommended to design the L_S value as small as possible.

When selecting R_G, it is also necessary to consider matching with the capacitance of the IGBT drive circuit. Therefore, please select the R_G after careful consideration using the capacitance characteristics as shown in Chapter 2.3.

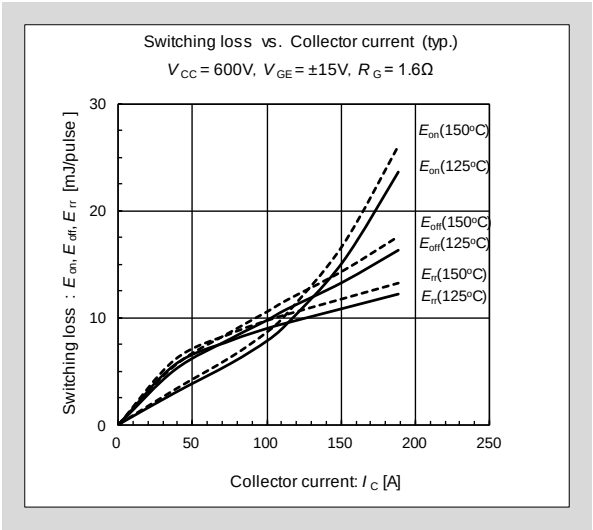


Fig. 2-9 Switching loss - I_C characteristics

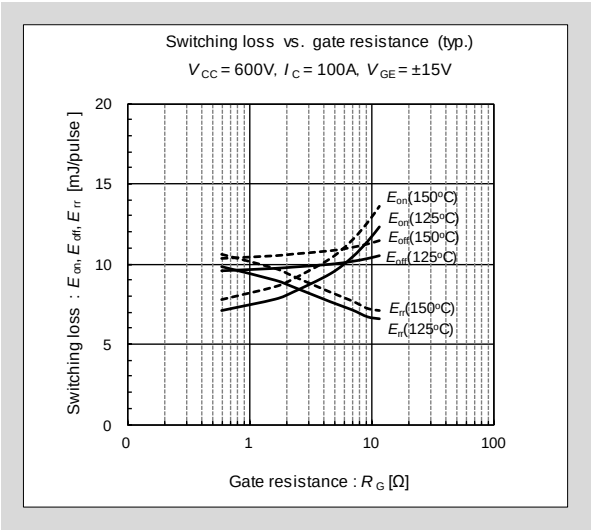


Fig. 2-10 Switching loss - R_G characteristics

2.3 Capacitance characteristics

Fig. 2-11 shows the characteristics of Q_g. This characteristic shows the change of V_{CE}, V_{GE} with respect to Q_g. 'Q_g increases' means 'charging the G-E capacitance of the IGBT', so when Q_g increases, V_{GE} (=Q_g / G-E capacitance) rises and the IGBT turns on. When the IGBT turns on, V_{CE} drops to the saturation voltage. Thus, Q_g indicates the amount of charge required to drive the IGBT. Use this characteristic when determining the power supply capacity of the drive circuit.

Fig. 2-12 shows the IGBT junction capacitance characteristics. Fig. 2-13 shows the junction capacitance C_{ies}, C_{oes} and C_{res}. Use these characteristics along with Q_g to design your drive circuit.

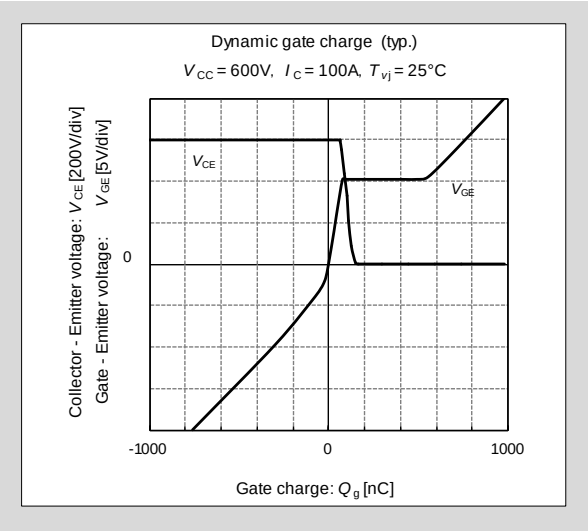


Fig. 2-11 V_{CE}, V_{GE} - Q_g characteristics

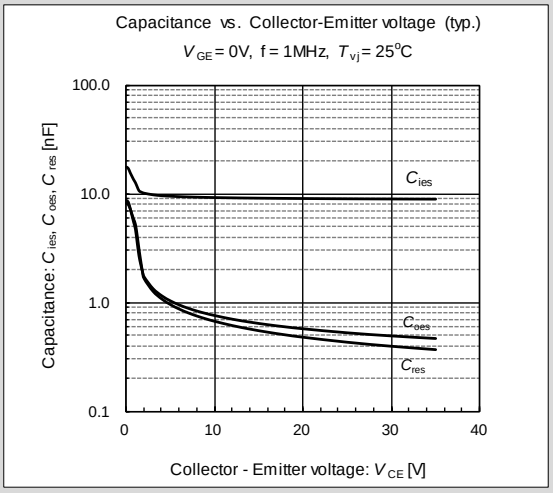


Fig. 2-12 Junction capacitance characteristic

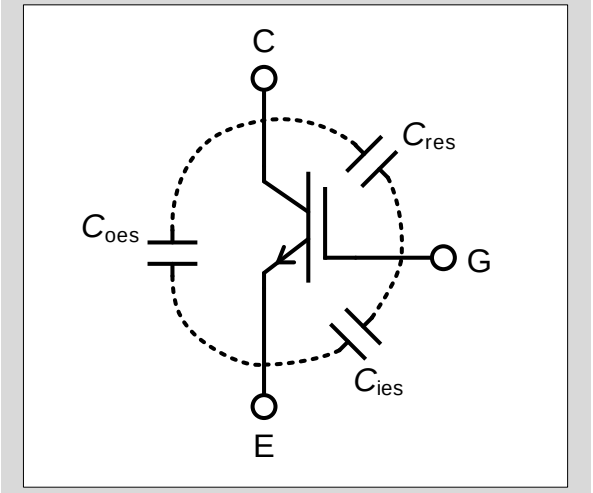


Fig. 2-13 Junction capacitance

2.4 Reverse biased safe operating area

During turn-off, IGBT has a safe operating area defined by V_{CE} an I_C called RBSOA (Reverse Bias Safe Operating Area). Fig. 2-14 shows the area of 1200V/100A IGBT as an example.

It is important to design the snubber circuit that will keep V_{CE} and I_C within the region of RBSOA when the IGBT is turned off. In the case of a short circuit (non-repetitive), the IGBT safe operating area defined by V_{CE} an I_C is called SCSOA (Short Circuit Safe Operating Area). SCSOA is different for each IGBT series, thus refer to the technical data of each series for details.

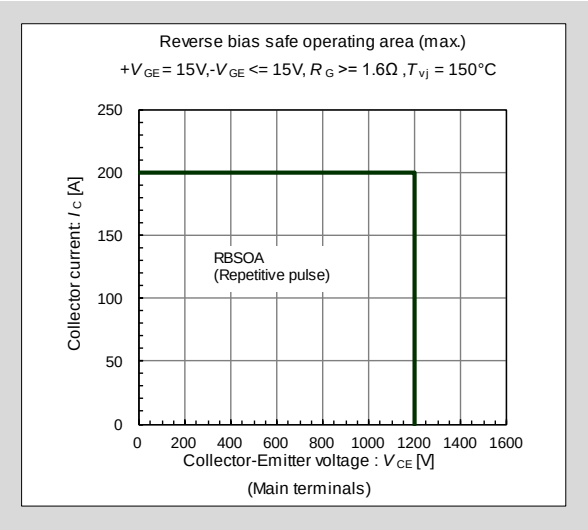


Fig. 2-14 RBSOA

2.5 FWD characteristics

The IGBT module has built-in anti-parallel FWD. Fig. 2-15 shows the FWD V_F-I_F characteristic, and Fig. 2-16 shows the reverse recovery characteristic (t_{rr}, I_{rr}). E_{rr} characteristics are shown in Fig. 2-9 and 2-10. Use these characteristics to calculate the power loss of FWD as well as the IGBT. Note that these characteristics change in accordance with I_F, T_{vj}, and R_G.

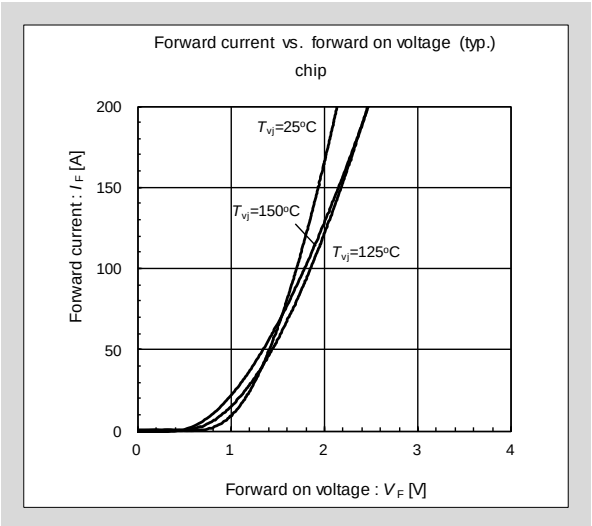


Fig. 2-15 V_F - I_F characteristics

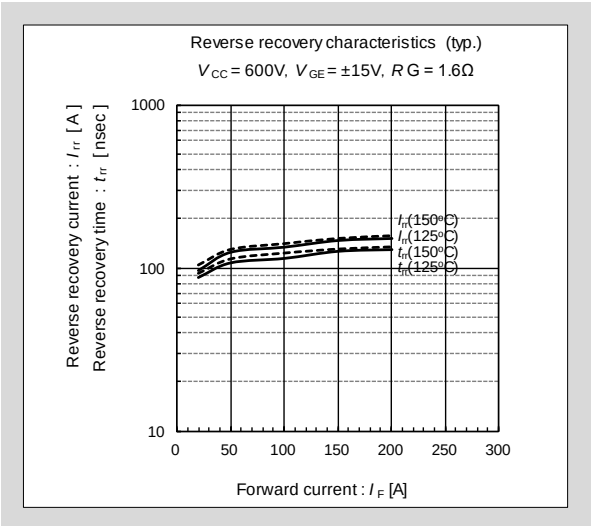


Fig. 2-16 t_{rr}, I_{rr} - I_F characteristics

2.6 Transient thermal resistance characteristics

Fig. 2-17 shows the transient thermal resistance characteristics used for temperature rise calculation and heat sink design (this characteristic is for one arm for both IGBT and FWD).

This thermal resistance is a characteristic often used in thermal analysis, and the formula is very similar to Ohm‘s law of electrical resistance. It is defined as:

Temperature difference ΔT [^{o}C] = Thermal resistance R_{th} [^{o}C / W] x Energy E (loss) [W]

In the IGBT module, the thermal resistance is used when calculating the T_{vj} of the IGBT and FWD. (For details, refer to Chapter 6 ‘Cooling Design’)

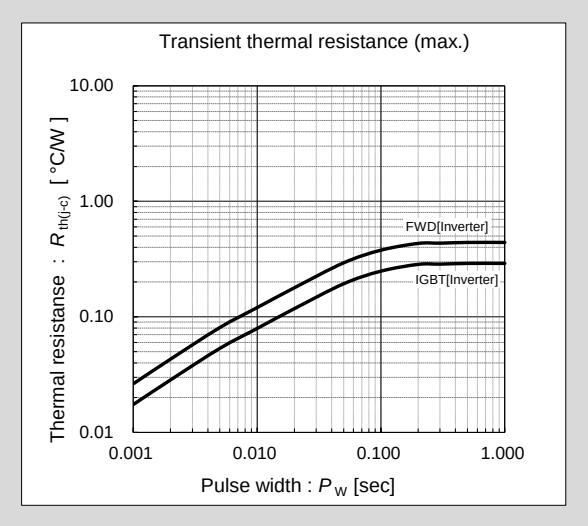


Fig. 2-17 Transient thermal resistance

Chapter 3 IGBT Module Selection and Application Notes

This chapter describes the precautions when using IGBT module and application.

1. Selection of IGBT Module Ratings

When using IGBT modules, it is important to select modules with the voltage and current ratings most suited for the intended application.

1.1 Voltage rating

The IGBT must have voltage rating that is suitable with the input voltage of the system in which it will be installed. Table 3-1 shows the IGBT voltage ratings and applicable input voltages. Use this table as a reference when selecting modules for a particular voltage application.

Table 3-1 IGBT rated voltage and application input voltage

	Area		IGBT rated voltage		
			600V	1200V	1700V
Commercial power supply voltage (input voltage)	Asia	Japan	200VAC	400VAC, 440VAC	690VAC (Industry high voltage power supply, wind power generation, etc.)
		South Korea	200VAC, 220VAC	380VAC	
		China	220VAC	380VAC	
	North America	U.S.A	120VAC, 208V, 240VAC	460VAC, 480VAC	
	Europe	U.K.	230VAC	480VAC	
		France	230VAC	400VAC	
		Germany	230VAC	400VAC	
		Russia	220VAC	380VAC	

1.2 Current rating

When the collector current I_C of the IGBT module increases, the conduction loss and switching loss increase, resulting in an increase in the module temperature. Since the IGBT module must be used with the virtual junction temperature T_{vj} of IGBT and FWD below the maximum virtual junction temperature $T_{vj(max)}$, I_C must be set in order not to exceed $T_{vj(max)}$.

Incorrect selection of current rating may lead to module destruction or deterioration of reliability. Note that in high frequency switching applications, switching loss increases, which increases the module temperature.

As a basic selection criteria, it is common to select a module with current rating higher than √2 times of the AC output current RMS value of the inverter circuit. However, the selection of the current rating depends on the operating conditions and heat dissipation conditions of the equipment, thus it is important to select the current rating after checking the power loss and temperature rise in the equipment.

1.3 Maximum rating

Use the product within the maximum ratings (voltage, current, temperature, etc.) described in the specifications. Using the product beyond the maximum rating may destroy the product. Also, the value described in each item of the absolute maximum rating is specified for that item, not for combination of more than one item.

1.4 RBSOA

Make sure that the IGBT turn-off voltage and current operating trajectories are within the RBSOA specifications. Using the IGBT beyond the RBSOA region may destroy the product.

1.5 Diode inrush current

When using the rectifier diode or FWD for rectifier application, a large inrush current will flow to charge the DC smoothing capacitor when the power is turned on. The guaranteed values for this inrush current are expressed as I_{FSM} (non-repetitive) and I^2t (non-repetitive). However, if inrush current flows frequently into the product, the product may be destroyed due to power cycle destruction by the repetitive current. For applications where such inrush current flows frequently, take measures to suppress the inrush current to prevent power cycle destruction.

Note that inrush current may flow to charge the capacitor too when an instantaneous voltage drop occurs in the power supply system.

On the other hand, if transient surge voltage due to lightning strike, etc. that exceeds the voltage rating of the product is applied to the product, the product might be destroyed. Thus, if surge voltage is expected, insert surge protection devices to suppress the voltage to within the product specifications.

2. Static Electricity Countermeasures

Generally, the absolute maximum rating of $V_{GE,}$ V_{GES} is ±20V. If voltage exceeding V_{GES} is applied to G-E, the IGBT gate may be destroyed. Therefore, ensure that V_{GE} value does not exceed V_{GES}.

If voltage is applied between C-E of IGBT while G-E is open as shown in Fig. 3-1, the IGBT may be destroyed. This is because the current *i* flows from the collector to the gate due to changes in the collector voltage, causing the gate voltage to rise and turn-on the IGBT. As a result, collector current will flow and the IGBT could overheat and be destroyed.

For this reason, after installing an IGBT module, if the gate circuit is malfunctioning or completely inoperative (gate is open), the IGBT may be destroyed when voltage is applied to the main circuit. In order to prevent this, it is recommended to connect a 10kΩ resistor (R_{GE}) between G-E.

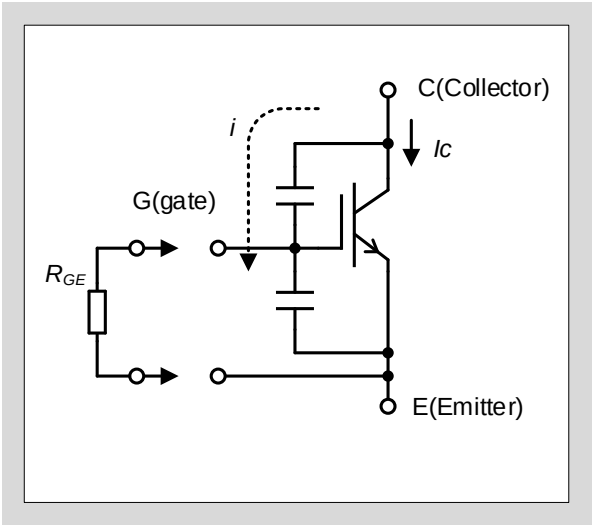


Fig. 3-1 IGBT behavior when G-E is open

Furthermore, the IGBT gate is very sensitive to static electricity. Observe the following precautions when handling the product.

(1) When handling IGBT modules after unpacking, discharge any static electricity from your body and clothes by grounding through a high resistance (1MΩ). Then, any handling of IGBTs should be done while standing on a grounded conductive mat.
(2) The terminals of IGBT modules are not protected against static electricity. When handling, hold them by the module case and do not touch the terminals (especially the control terminals).
(3) When soldering the terminals, ground the tip of the soldering iron through a low resistance to protect the module from static electricity .

3. Protection Circuits Design

Since IGBT modules may be destroyed by overcurrent, overvoltage or other abnormality, it is necessary to design protection circuits.

It is important to fully understand the IGBT modules characteristics when designing these circuits. An inappropriate circuit will not be able to protect the module. For example, the overcurrent cut-off time may be too long, or the capacitance of the snubber capacitor may be too small.

For more details on overcurrent and overvoltage protection methods, refer to Chapter 5 ‘Protection Circuit Design’ of this manual.

4. Cooling Design

IGBT modules have a maximum virtual junction temperature ($T_{vj(max)}$). An appropriate heat sink must be selected to keep the temperature below this value. When designing heat sink, the operating conditions of the IGBT module has to be fully considered.

First, calculate the loss of the IGBT module. Based on that loss, select a heat sink that will keep T_{vj} below the limit. If the heat sink design is insufficient, the temperature may exceed $T_{vj(max)}$ during operation and destroy the module. For more information on IGBT power loss calculation and heat sink selection methods, refer to Chapter 6 ‘Cooling Design’ of this manual.

5. Gate Drive Circuits Design

It is no exaggeration to say that the design of the gate drive circuits ultimately determines the performance of the IGBT. It is also closely related to the protection circuits design.

Gate drive circuits consists of a forward bias circuit to turn-on the IGBT, and a reverse bias circuit to turn-off and keep the IGBT in a stable off state. The characteristics of the IGBT change in accordance with each bias condition.

Insufficient reverse bias gate voltage $-V_{GE}$ may cause false turn-on. Set a sufficient $-V_{GE}$ value to prevent false turn-on. If the dv/dt is high, false turn-on of the opposing arm IGBT, gate overvoltage, or noise propagation to the power supply line may occur. Set the optimum drive conditions ($+V_{GE}$, $-V_{GE}$, R_G, C_{GE}) to avoid these problems.

Also, if the wiring length between the IGBT module and the gate drive circuit is long, the gate voltage at the product terminal may fluctuate and the product may be destroyed by overvoltage.

For more information on how to design the best gate drive circuits, refer to Chapter 7 ‘Gate Drive Circuit Design’ of this manual.

6. Parallel Connection

In high capacity inverters and other equipment that needs to control large currents, it may be necessary to connect IGBT modules in parallel.

In parallel connection, it is important that the circuit design allows an equal flow of current to each of the modules. If the current is not balanced among the IGBTs, a higher current may concentrate in one IGBT and destroy it.

The electrical characteristics of each module as well as the wiring design determines the current balance between parallel modules. Thus, it is necessary to design such that the C-E saturation voltage $V_{CE(sat)}$ of each parallel modules is matched and the main circuit wiring is symmetrical.

For a detailed explanation, refer to Chapter 8 "Parallel Connections“ of this manual.

Note that the 6-Pack, PIM, IPM, and Small IPM are not designed on the premise of using in parallel connections, thus application of these modules in parallel connections are not guaranteed.

7. Mounting Notes

7.1 Mounting to heat sink

When mounting the product to heat sink, it is recommended to apply thermal grease to the module’s base plate to ensure heat dissipation. In order to spread the thermal grease evenly, the flatness and surface roughness of the heat sink should be within the range of the recommended values described in the specifications.

If the amount and application method of the thermal grease are not appropriate, it may prevent the thermal grease from spreading over the entire module’s base plate, resulting in poor heat dissipation and lead to thermal failure. To determine whether the amount of thermal grease applied and the method of application is appropriate, confirm that the thermal grease has spread over the entire base plate of the product. (You can check the extent of spreading by removing the module after mounting)

If the amount of thermal grease near the product mounting hole is excessive, the thermal grease will act as a spacer, hindering the spread of the thermal grease and causing deterioration in heat dissipation.

Also, depending on the properties of the thermal grease and application method, the thermal grease may deteriorate or deplete during high temperature operation and temperature cycles, shortening the product lifetime. Thus, pay attention to the selection and application method of thermal grease.

The surface flatness of the heat sink between the screw mounting holes should be 50μm or less per 100mm, and the surface roughness should be 10μm or less. Excessive convex warpage may cause insulation failure of the product, leading to serious accidents. On the other hand, excessive concave warpage or distortion will create gaps between the IGBT module and the heat sink, which will result in poor heat dissipation and may lead to thermal failure.

Refer to the mounting instruction of each package for details on how to select and apply thermal grease, and how to mount the product to heat sink.

Note that the surface flatness and roughness requirements for heat sinks of PrimePACK™* differ from other products. Refer to the mounting instruction for details.

*PrimePACK™ is a registered trademark of Infineon Technologies

7.2 Terminal connections

During soldering of the IGBT module terminals, note that soldering at an excessively high temperatures may cause deterioration of the package. If reflow soldering method is used, the solder inside the IGBT module may remelt and affect its reliability. In this case, Fuji Electric Co., Ltd. is not responsible for the product performance and appearance.

If the applied bus bars are not suitable, the temperature of the main terminals may rise above the storage temperature. Use the main terminals within the storage temperature range.

Applying excessive stress (tensile, pushing, bending) to the main terminals and control terminals may deform the terminals and crack the case resin, resulting in poor contact and poor insulation. Refer to the mounting instructions of each package for the maximum allowable stress on the main and control terminals.

For screw type terminals, tighten the screws with the specified tightening torque. If the tightening torque is excessive, insulation failure may occur due to cracking of the case. If the tightening torque is small, the contact resistance may increase, resulting in increased heat generation at the terminals. In addition, it is expected that the screws may loosen due to vibration, etc., thus select and use screws that are difficult to loosen, tighten with the appropriate torque, and perform retightening to suppress the occurrence.

Refer to the outline drawing in the specifications and select screws with the appropriate length. If the screw length is longer than the allowable value, the product may be damaged, resulting in ground fault or insulation failure. In such cases, Fuji Electric will not be held responsible.

If the printed circuit board is not suitable, the temperature of the main terminal pins may rise above the storage temperature. Use the main terminal pins within the storage temperature range.

Applying excessive stress (tensile, pushing, bending) to the main terminals and control terminals may deform the terminals and crack the case resin, resulting in poor contact and poor insulation. Refer to the mounting instructions of each package for the maximum allowable stress on the main and control terminals.

Do not apply stress that causes the lid to deform. The internal circuit of the product may be damaged in the pushing direction. In addition, the lid may come off in the pulling direction.

8. Storage and Transportation Notes

8.1 Storage

(1) The products should be stored at an ambient temperature of 5 to 35ºC and humidity of 45 to 75%. If the storage area is very dry, a humidifier may be required. In such case, use only deionized water or boiled water, since the chlorine in tap water may corrode the product terminals.
(2) Avoid exposure to corrosive gases and dust.
(3) Rapid temperature changes may cause condensation on the product surface. Avoid such environment and store products in a place with minimal temperature changes.
(4) Do not apply external force to the products during storage. Unexpected force may be applied to the products when stacked. Do not place heavy objects on the products.
(5) Store the products with unprocessed terminals. Storing after the terminals are processed may cause soldering defects later during product mounting due to rust.
(6) Use only antistatic containers or the same container as shipped for storing the products in order to prevent ESD damage.
(7) Use grounded metal storage shelves.

8.2 Transportation

(1) Avoid extreme forces such as dropping or shock when transporting the products .
(2) When transporting several products in the same box or container, insert padding between the products to protect the terminals and to keep the products from shifting.
(3) Take measures against static electricity from being applied to the gate terminals, such as using antistatic bag or shorting the gate and emitter with aluminum foil when transporting the product.

9. Reliability Notes (Lifetime Design)

Generally, during the operation of power converters such as inverters, the temperature of the IGBT module T_{vj} rises and falls repeatedly. This temperature change ΔT_{vj} causes the IGBT module to be exposed to thermal stress, which may shorten its lifetime depending on the operating conditions. Therefore, it is necessary to design the lifetime of the IGBT module to be longer than that of the power converters.

In most cases, the temperature change of the IGBT module is checked and the lifetime design is performed based on the power cycling (P/C) capability. If the lifetime design is insufficient, the lifetime of the IGBT module may be shorter than the required lifetime, and the module reliability may not be ensured. Therefore, it is important to design the IGBT module lifetime so that it meets the required reliability. For more detailed information on reliability notes, refer to Chapter 11 ‘Reliability of Power Modules’ of this manual.

Please use the IGBT module within the ΔT_{vj} P/C lifetime shown in Fig. 11-5. However, Fig. 11-5 shows the ΔT_{vj} P/C lifetime of the V series IGBT modules. The ΔT_{vj} P/C lifetime of the X series is different. Please refer to the technical data for details. In addition to this ΔT_{vj} P/C, there is another P/C based on the case temperature change of the module, ΔT_C P/C. Since the ΔT_C P/C lifetime depends on the thermal stress caused by the rise and fall of the case temperature, the lifetime of the IGBT module is greatly affected by the cooling design of the equipment. If the case temperature rises and falls frequently, pay sufficient attention to the product lifetime.

If the IGBT module is used beyond its lifetime, product quality deterioration may occur. In the worst case, the IGBT module may be destroyed. Please fully understand the usage environment of the equipment in which the IGBT module is to be installed, and apply the IGBT module after considering whether the target lifetime can be satisfied.

10. Other Precautions

Be sure to install an adequate fuse or circuit breaker between the power supply and the product in case the product is destroyed by an unexpected accident to prevent secondary destruction such as fire, explosion, and spread of fire.

In environments containing acids, alkalis, organic substances, corrosive gases (hydrogen sulfide, sulfurous acid gas, etc.), and corrosive liquids (cutting fluid, etc.), the product may oxidize or corrode, resulting in poor contact, disconnection, short circuit, ground fault, etc. In such cases, do not use the product as it may cause malfunctions. Should a short circuit or ground fault occurs, there is a secondary risk of smoke, fire, or explosion. If the product is used under conditions containing these corrosive substances, Fuji Electric Co., Ltd. is not responsible regardless of the conditions (temperature, humidity, concentration, etc.).

If the product is to be operated after being stored or assembled in a high humidity environment, operate the equipment after removing the moisture sufficiently. If the product is operated in a moisture-absorbed state, it may cause electrical wiring defects or insulation failures inside the product, in which case Fuji Electric Co., Ltd. is not responsible.

The products are not designed for use in dusty environments. If it is used in an environment where dust is generated, heat dissipation may deteriorate due to the heat sink may become clogged, and short circuits or ground faults may occur due to leaks between terminals or creeping discharge. (Even if the dust is an insulating material such as fiber, it may leak due to moisture absorption.)

In general, semiconductor devices have random failure modes due to high-speed particles (cosmic rays) originating from space and radiation. The failure rate in this failure mode varies depending on the installation location (latitude, longitude, altitude), installation environment, and operating conditions (voltage). Please contact Fuji Electric Co., Ltd. when using the product under high altitude or high voltage conditions.

Clearance distance and creepage distance of the products are designed for usage in an environment of 2000m or less above sea level. Fuji Electric Co., Ltd. is not responsible if the product is used in an environment exceeding this or in an environment with low atmospheric pressure.

Chapter 4 Typical Troubles and Troubleshooting

This chapter describes typical troubles and how to deal with them.

1. Troubleshooting

Abnormality such as incorrect wiring or mounting of IGBT modules in inverter circuit, etc., could cause module destruction. Because there are many failure modes, it is important to first determine the cause of the problem, and take the necessary countermeasures. Table 4-1 shows how to determine a module's failure modes as well as the causes by observing the module external abnormalities. First of all, check the estimated failure mode from Table 4-1. If the cause cannot be determined using this table, use the detailed analysis charts in Fig. 4-1. In addition, method to determine whether the module is broken is described in section 4.2, and typical troubles and their countermeasures are described in section 4.3. These can be used to assist in finding the cause.

Table 4-1 Failure mode and cause estimation

External abnormalities		Cause		Failure mode	Checkpoints
Short circuit	Arm short circuit	Surge voltage during short circuit protection exceeds SCSOA.		SCSOA (surge voltage)	Check that short circuit waveform (locus) and device ruggedness match.
	Series arm short circuit	Insufficient dead time	Insufficient $-V_{GE}$ Dead time setting error	Overheating	Check that device t_{off} and dead time match.
		dv/dt malfunction	Insufficient $-V_{GE}$ Gate wiring too long	SCSOA and overheating	Check for false turn-on caused by dv/dt.
		Noise, etc.	Logic or gate drive circuit malfunction		Check for circuit malfunction.
	Output short circuit	Miswiring, abnormal wire contact, or load short circuit.			Check conditions at time of failure. Check that device ruggedness and protection circuit match. Check wiring condition.
	Ground fault	Miswiring, abnormal wire contact			
Overload (overcurrent)		Logic circuit malfunction		Overheating	Check logic circuit.
		Overcurrent protection circuit setting error			Adjust overcurrent protection level.
Overvoltage	Excessive DC voltage	C-E voltage exceeds voltage rating	Excessive input voltage	C-E overvoltage	Adjust overvoltage protection level.
			Overvoltage protection setting error		
	Excessive surge voltage	Surge voltage during turn-off exceeds RBSOA		RBSOA	Check that turn-off waveform (locus) and RBSOA match. Review snubber circuit.
		Surge voltage during FWD reverse recovery exceeds voltage rating		C-E overvoltage	Check that surge voltage and voltage rating match. Review snubber circuit.
		Short on-pulse reverse recovery	Logic or gate drive circuit malfunction due to noise		Check logic circuit.
			Interference to gate signal from the main circuit, etc.		Check gate signal. Use twisted pair wire. Check distance between main circuit and signal wire.
Drive supply voltage drop		V_{GE} drops resulting in increased heat (loss) generation	DC-DC converter malfunction	Overheating	Check for circuit malfunction.
			Drive voltage rise is too slow.		
			Disconnected wire		
Gate overvoltage		Static electricity applied to gate		G-E overvoltage	Check operating conditions (anti-static protection).
		Surge voltage due to excessive length of gate wiring			Check gate voltage.
Driving IGBT with gate open		Applying voltage at C-E with the gate open		Overheating	Check gate voltage.
Overheating	Insufficient heat dissipation	T_{vj} exceeds maximum value	Loose screws	Overheating	Check cooling conditions.
			Insufficient thermal grease		
			Cooling fan stopped		
	Increased loss	Logic circuit malfunction			Check logic circuits.
Stress	Stress	Soldering inside the module disconnected due to stress fatigue	Stress from external wiring	Disconnection of internal circuit (open)	Check the generated stress. Check the mounting condition of the module and other mounting parts.
	Vibration		Stress from vibration of other mounting parts		
Reliability (Lifetime)		The application conditions do not match the reliability of the module		Failure mode is different for each case	Refer to Fig. 4-1.

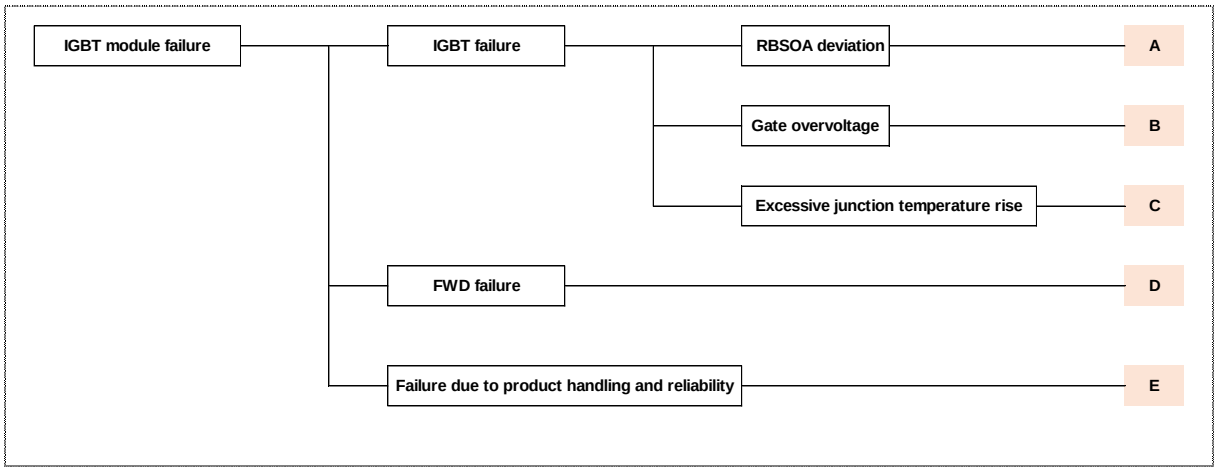


Fig. 4-1(a) IGBT module failure analysis chart (* Symbols A to D are linked to the charts below)

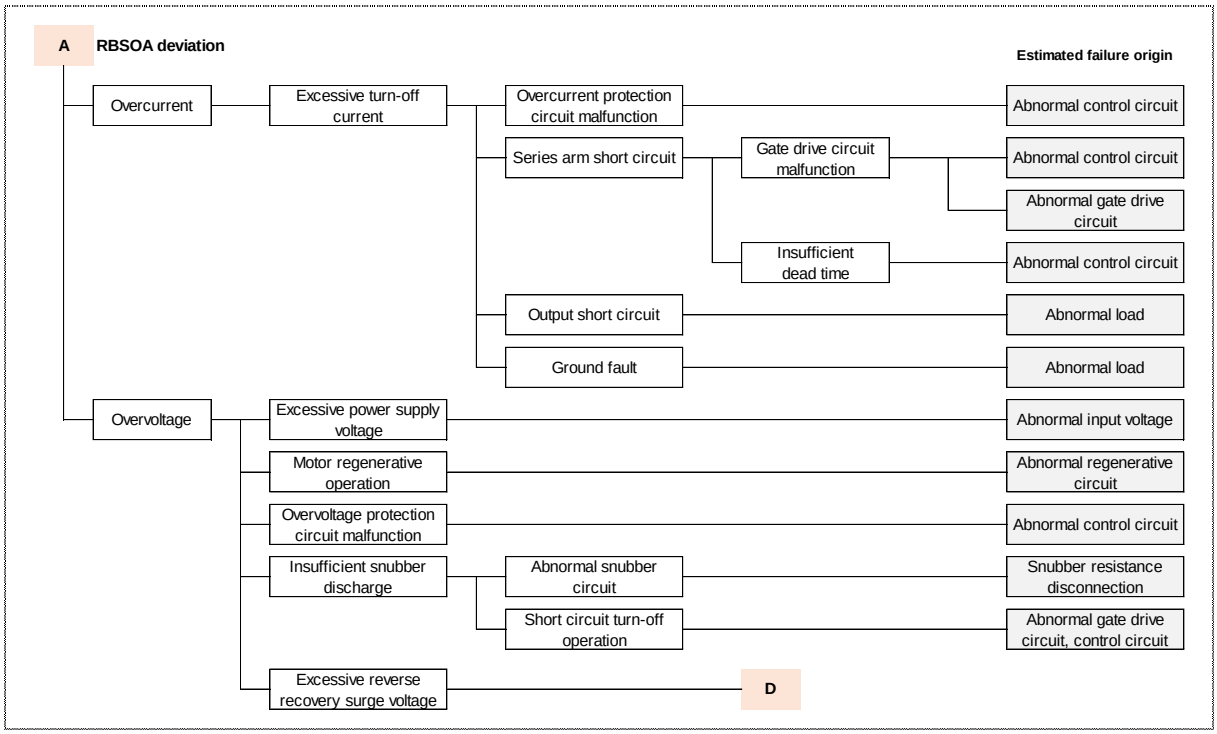


Fig. 4-1(b) Mode A: RBSOA deviation

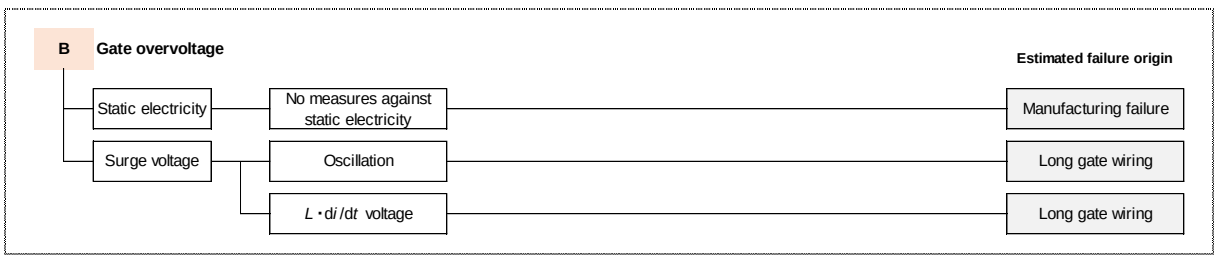


Fig. 4-1(c) Mode B: Gate overvoltage

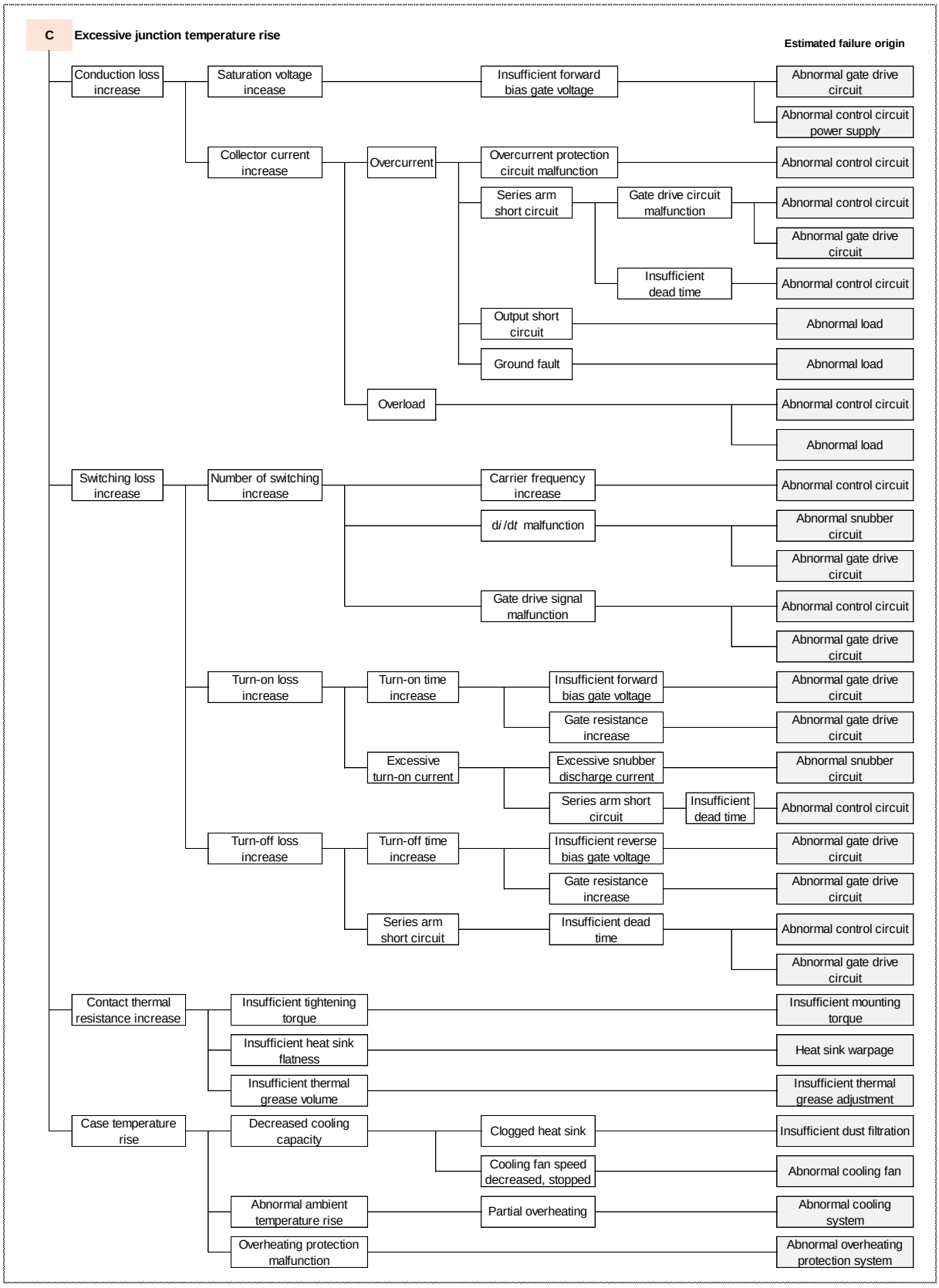


Fig. 4-1(d) Mode C: Excessive junction temperature rise

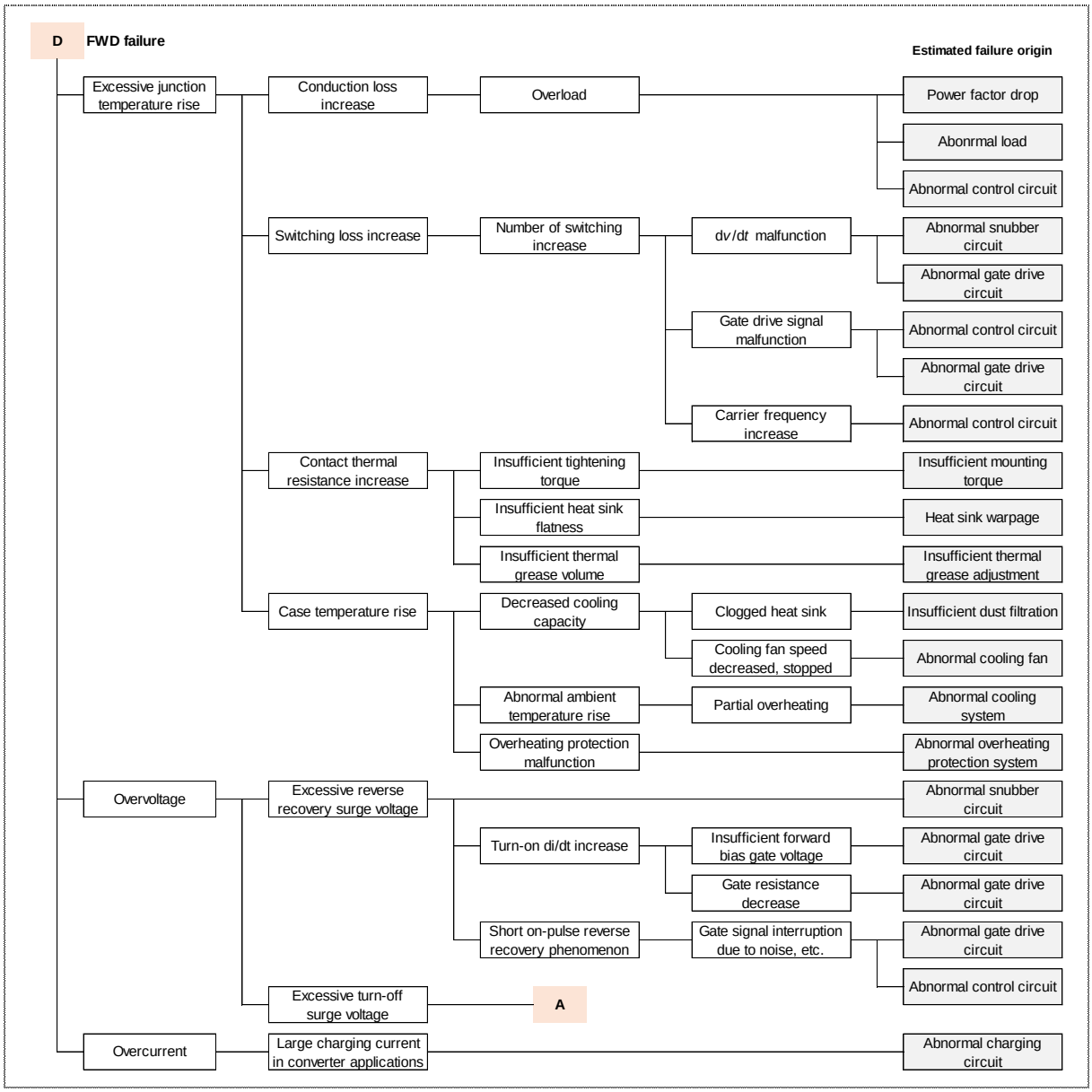


Fig. 4-1(e) Mode D: FWD failure

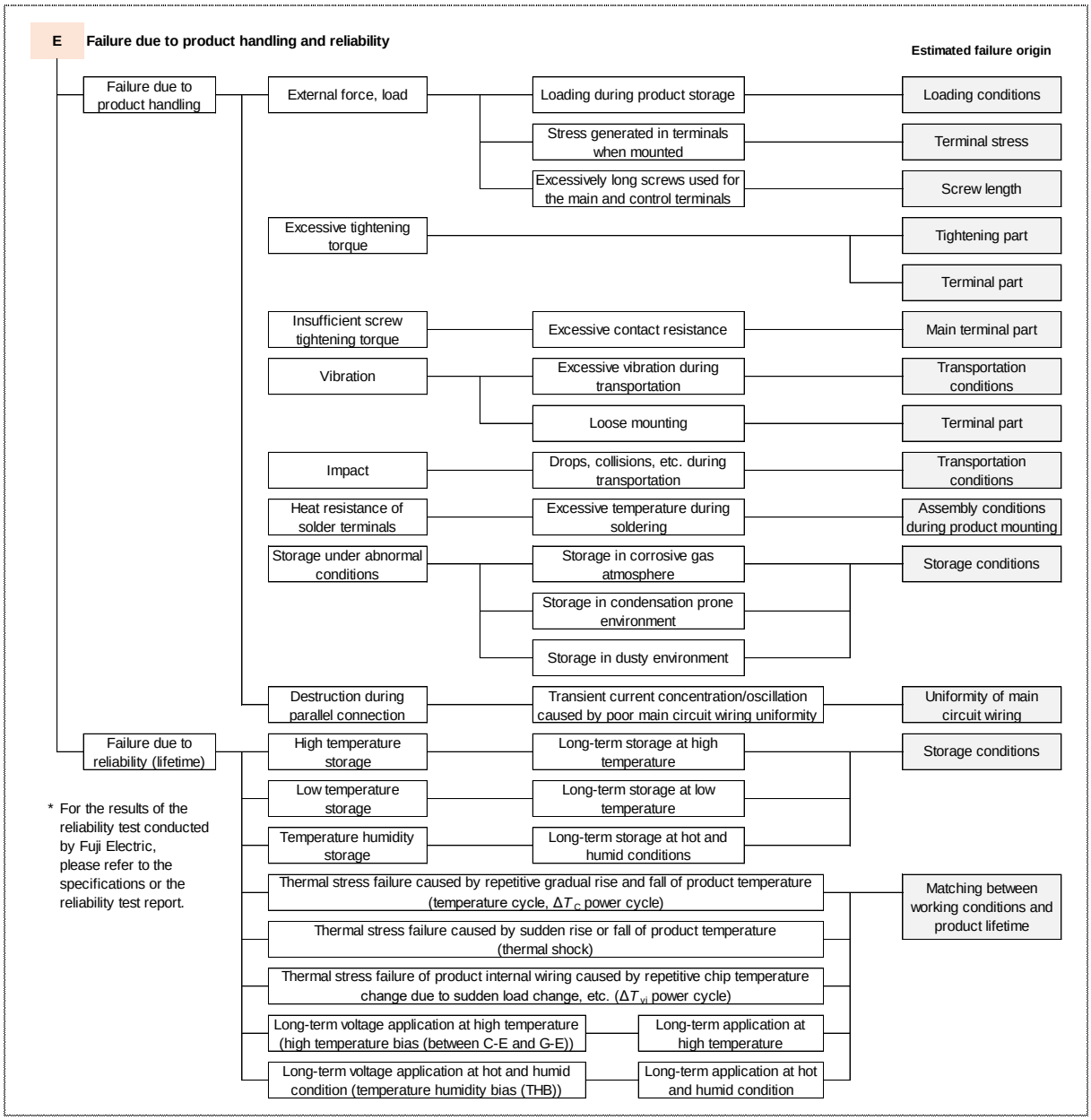


Fig. 4-1(f) Mode E: Failure due to product handling and reliability

2. IGBT Test Procedures

An IGBT module that has been found to be faulty can be checked by using a transistor characteristics measuring device called a 'transistor curve tracer (CT)'.

(1) G-E leakage current

(2) C-E leakage current (short G-E)

If a CT is not available, other test equipment such as a tester that is capable of measuring voltage/resistance can be used to help to diagnose the module.

2.1 G-E leakage current check

As shown in Fig.4-2, measure the leakage current or resistance between G-E, with C-E shorted. (Do not apply a voltage in excess of 20V between G-E. If a tester is used, make sure that the internal battery voltage is less than 20V.)

If the module is normal, the leakage current reading will be on the order of several 100nA (if a tester is used, the resistance reading will be on the order of 10MΩ to infinity). Otherwise, the device has most likely destroyed (generally, if a device is destroyed, G-E will be short-circuited).

2.2 C-E leakage current check

As shown in Fig.4-3, measure the leakage current or resistance between C-E, with G-E shorted. Be sure to connect C to (+) and E to (-). If the polarity is reversed, the FWD will conduct and shorts C-E.

If the module is normal, the leakage current reading should read below the I_{CES} maximum value specified in the datasheet (if a tester is used, the resistance reading will be on the order of 10MΩ to infinity). Otherwise, the device has most likely destroyed (generally, if a device is destroyed, C-E will be short-circuited).

Caution: Never perform withstand voltage measurement between C-G. It might cause the dielectric breakdown of the oxide layer due to excessive voltage.

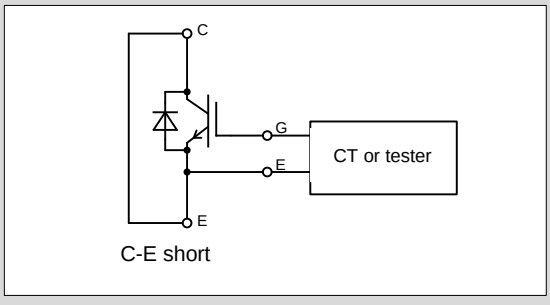


Fig. 4-2 G-E check

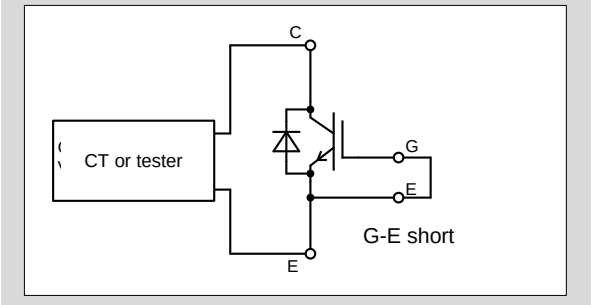


Fig. 4-3 C-E check

3. Typical Troubles and Troubleshooting

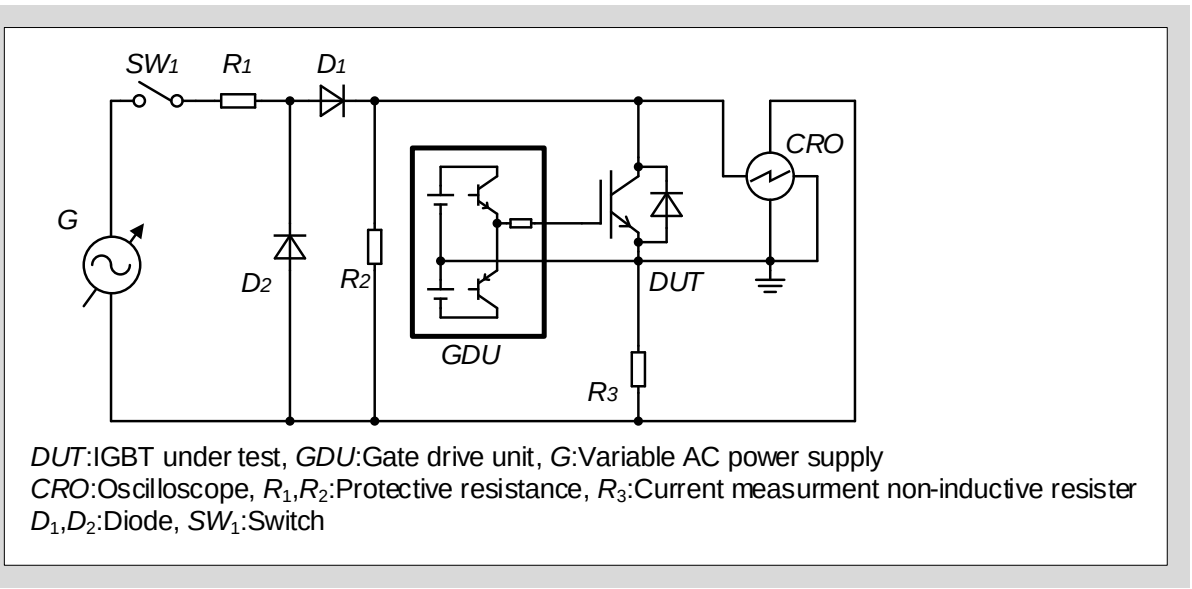
3.1 Main circuit voltage application with G-E open

If main circuit voltage is applied with G-E open, the IGBT would be turned on autonomously, triggering a large current flow and cause device destruction. This phenomenon occurs when the G-E capacitance is charged through the feedback capacitance C_{res} of the IGBT, raising the gate potential and causing the IGBT to be turned on. Take measures such as connecting a resistor of about 10kΩ to G-E to prevent G-E from being opened (refer to Chapter 3, item 2).

If the gate signal line is switched using a mechanical switch, such as a rotary switch during product acceptance testing or on similar occasions, the G-E may open instantaneously at the time of switching, which could cause device destruction if voltage is applied to C-E.

When the mechanical switch chatters, a similar period is generated, leading to device destruction. To prevent this, be sure to discharge the main circuit voltage to 0V before switching the gate signal. Furthermore, when conducting characteristics test, such as acceptance test on a product comprising multiple devices (two or more), be sure to short G-E of the devices other than the one under test.

Fig. 4-4 shows an example of an on-voltage measurement circuit. The measurement procedure is described using this circuit. First, turn off the gate drive unit (GDU) ($V_{GE} \leqq$ 0V), then turn on SW_1 to apply voltage to C-E. Next, apply a predefined forward bias voltage to G-E from the GDU to turn-on the IGBT and measure the on voltage. Finally, turn off the gate circuit and then turn off SW_1. This sequence allows for safe measurement of device characteristics without risking destruction.



DUT:IGBT under test, *GDU*:Gate drive unit, *G*:Variable AC power supply
CRO:Oscilloscope, R_1,R_2:Protective resistance, R_3:Current measurment non-inductive resister
D_1,D_2:Diode, SW_1:Switch

Fig. 4-4 On voltage measurement circuit

3.2 Destruction caused by mechanical stress

If the module terminals are subjected to stress from a large external force or vibration, the internal electrical wiring of the product could be destroyed. Be careful not to apply such stress when mounting the module.

Fig. 4-5 shows an example of mounting a gate drive printed circuit board (PCB) on top of the module. As shown in Fig. 4-5(a), if the gate drive PCB is mounted without fixing it, the PCB might vibrate due to vibration during transportation. This vibration may apply stress to the module terminals, causing internal electrical wiring damage. To prevent this, it is recommended to fix the PCB as shown in Fig 4-5(b). Use a dedicated fixing material with sufficient strength.

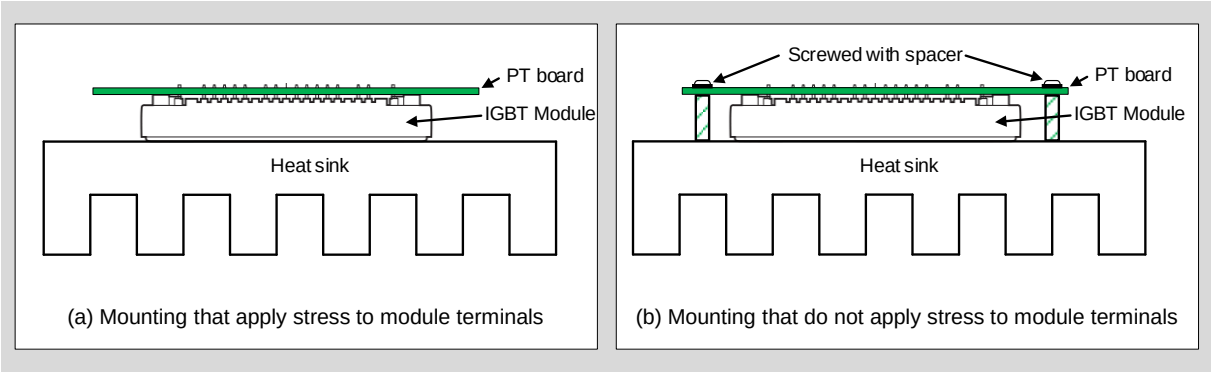


Fig. 4-5 Fixing a PCB

Fig. 4-6 shows an example of main circuit wiring using a laminated bus bar. If there is a step difference between the (+) and (-) conductors as shown in Fig. 4-6(a), the terminals are continually exposed to upward tensile stress, which may cause disconnection of the internal electrical wiring. To prevent this problem, it is recommended to insert a conductive spacer to eliminate the step difference as shown in Fig. 4-6(b). Furthermore, in the PCB structure, if the wiring height is misaligned, large tensile stress or external force will be applied to the terminals, which may cause similar problems. Thus, laminated bus bar or PCB needs to be mounted without tensile stress.

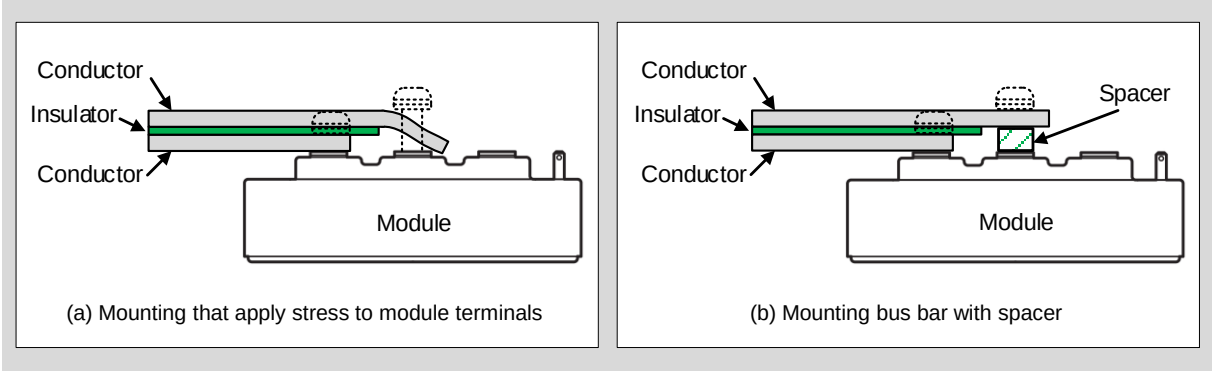


Fig. 4-6 Mounting with laminated bus bar

3.3 False turn-on of the IGBT caused by insufficient $-V_{GE}$

Insufficient reverse bias gate voltage $-V_{GE}$ induces false turn-on of the IGBT, resulting in short circuit of both the upper and lower arm IGBTs. The product may be destroyed by the surge voltage or loss generated when the short circuit current is cut off. Therefore, make sure that false turn-on does not happen when designing the equipment (recommended $-V_{GE}$=15V). In addition, please refer to Chapter 7, section 1.4 for the details of the malfunction occurrence mechanism due to the d*v*/d*t* when $-V_{GE}$ is insufficient.

Fig. 4-7 shows an example of how to check the presence of short circuit current in the upper and lower arms. First, disconnect the output terminals (U, V, W) of the inverter (open, no load). Next, start the inverter and drive each IGBT. At this time, if the current flowing from the power supply line is detected as shown in the figure., the presence of short circuit current can be checked. If $-V_{GE}$ is sufficient, only a very small pulse current (about 5% of the rated current) that charges the junction capacitance of the device will be observed. However, if $-V_{GE}$ is insufficient and short circuit occurs, this current will increase. To make an accurate judgment, it is recommended to perform this current measurement with $-V_{GE}$=15V first, and then measure the current again with the specified $-V_{GE}$. If the current of both cases have the same value, it means that there is no false turn-on.

If false turn-on is confirmed by the above method, countermeasures include increasing $-V_{GE}$ until the short circuit current disappears, or connect a capacitor (C_{GE}) with capacitance of about twice the value of C_{ies} described in the specifications between G-E. Is recommended to connect C_{GE} close to the gate terminals.

However, simply adding C_{GE} will increase the switching time and loss. In order to have equivalent switching time and loss before C_{GE} addition, it is recommended to decrease the R_G value to about half of that before C_{GE} addition.

Another cause of short circuit through the upper and lower arms is insufficient dead time. When this happens, short circuit current will be observed in the test. If the short circuit current does not decrease even when $-V_{GE}$ is increased, increasing the dead time is necessary. Please refer to Chapter 7, section 3 for a detailed explanation of dead time.

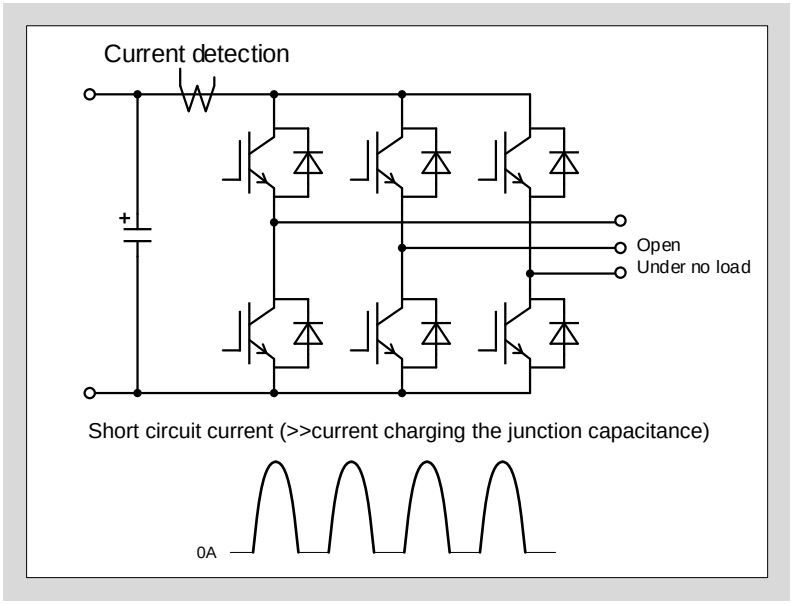


Fig. 4-7 Short circuit current measuring circuit

3.4 Diode reverse recovery from a transient on state (short on-pulse reverse recovery)

The IGBT module contains built-in FWD. Paying close attention to the behavior of this FWD is very important for designing a reliable equipment. This section describes the short on-pulse reverse recovery phenomenon, which is likely to lead to module destruction.

The short on-pulse reverse recovery phenomenon is a phenomenon in which the gate signal is interrupted due to noise, etc. when driving the IGBT, resulting in a very large reverse recovery surge voltage. Fig. 4-8 shows the waveforms of short on-pulse reverse recovery. If a very short off-pulse (T_w) with respect to the on period (T_{ON}) of IGBT is generated, the FWD on the opposite arm will enter reverse recovery in a very short time after it is turned on. Normally, reverse recovery starts after sufficient carriers are accumulated in the FWD, whereas in the short on-pulse reverse recovery, reverse recovery starts without sufficient carrier accumulation in the FWD. As a result, the depletion layer of FWD expands at a rapid speed, causing steep d*i*/d*t* and d*v*/d*t*. This causes a very large reverse recovery surge voltage to occur between C-E (K-A). If the surge voltage exceeds the module rated voltage, it may lead to module destruction.

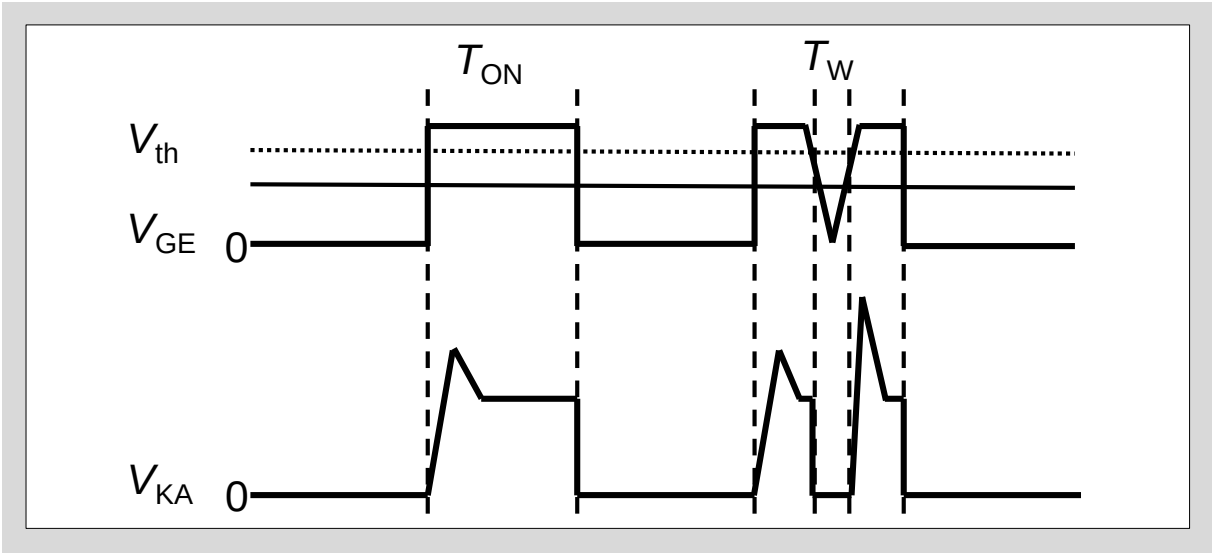


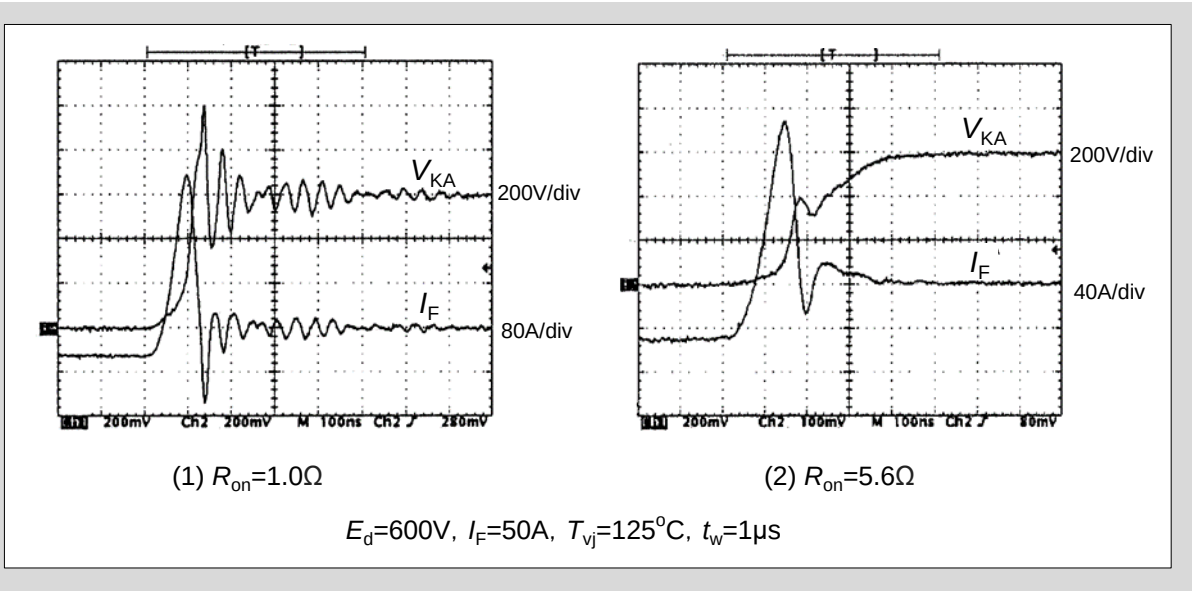
Fig. 4-8 Waveforms at short on-pulse reverse recovery

Our tests confirmed that a surge voltage increases sharply when T_w < 1μs. Be sure not to design a circuit that will generate such short gate signal off pulses.

For equipment with operation mode of T_w < 1μs, verify that the surge voltage at minimum T_w does not exceed the module rated voltage. If the surge voltage exceeds the module rated voltage, take countermeasures to reduce surge voltage as follows.

- Increase R_G
- Reduce circuit inductance
- Enhance snubber circuit
- Add C_{GE}
- Add active clamping circuit

Fig. 4-9 shows the waveforms of short on-pulse reverse recovery of 6MBI450U-120 (1200V, 450A). As shown in the waveforms, surge voltage can be decreased by increasing R_G from 1.0Ω to 5.6Ω.



(1) R_{on}=1.0Ω (2) R_{on}=5.6Ω

E_d=600V, I_F=50A, T_{vj}=125°C, t_w=1μs

Fig. 4-9 Waveforms of short on-pulse reverse recovery

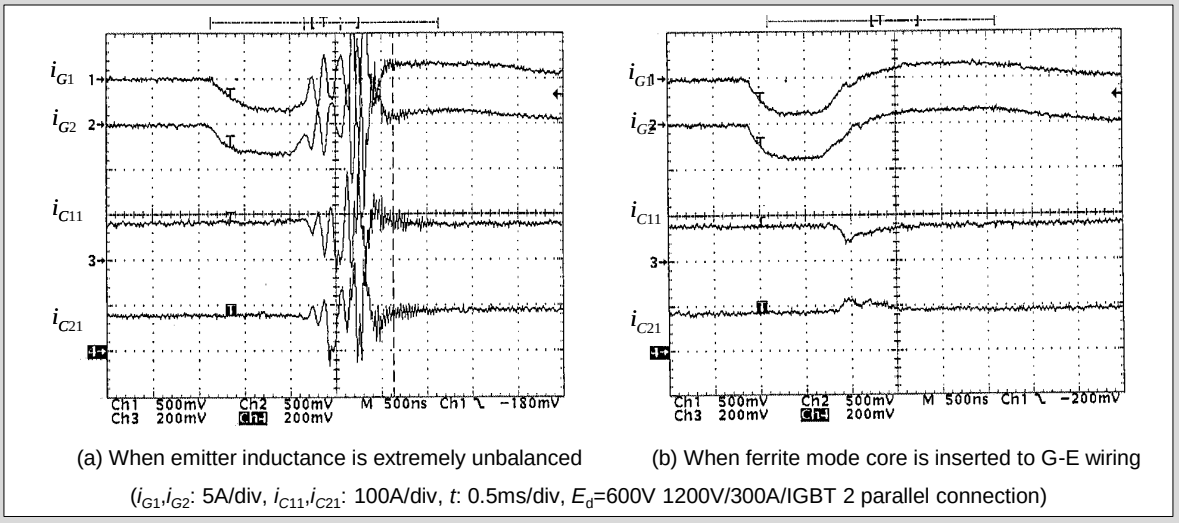
3.5 Oscillation during parallel connection

When connecting modules in parallel, the uniformity of the main circuit wiring is very important. If the wiring is unbalanced, current will concentrate on the module with a shorter wiring, which could lead to module destruction or deterioration of long-term reliability.

Also, if the main circuit wiring is not uniform, the overall main circuit inductance will also be unbalanced for each devices. Consequently, d*i*/d*t* during switching generate voltages of varied potentials in the individual wiring inductances, producing abnormal oscillating current such as a loop current, which could lead to module destruction.

Fig. 4-10(a) shows the oscillation phenomenon when the wiring inductance of the emitter is made extremely unbalanced. This oscillation happens due to oscillating current flows through the wiring loop of emitters connected in parallel, causing the IGBT gate voltage to oscillate, resulting in IGBT turn-on and turn-off at high speed. A ferrite core (common mode) can be inserted in each G-E wiring to suppress or eliminate the emitter loop current. Fig. 4-10(b) shows the waveforms with ferrite core inserted to each G-E wiring. As shown in the waveforms, oscillation is suppressed.

It is necessary to maintain circuit uniformity when designing the main circuit wiring of parallel connection.



(a) When emitter inductance is extremely unbalanced (b) When ferrite mode core is inserted to G-E wiring

(i_{G1},i_{G2}: 5A/div, i_{C11},i_{C21}: 100A/div, *t*: 0.5ms/div, E_d=600V 1200V/300A/IGBT 2 parallel connection)

Fig. 4-10 Waveforms of 2 parallel connection

3.6 Notes on the soldering process

When soldering the gate drive circuit or control circuit to the terminals of the module, if the solder temperature is excessively high, problems such as melting of the case resin material may occur. Avoid soldering process that exceeds the heat resistance test conditions defined in the specifications.

Terminal heat resistance test conditions in the general product specifications documents are shown below for reference.

Solder temperature: 260±5°C
Time: 10±1s
Cycles: 1

3.7 Using IGBT Module in converter application

Diodes used in the IGBT modules have I^2t rating. I^2t is the limit of the forward, non-repetitive overcurrent capability of current pulses with a very short duration (less than 10ms). For a sinusoidal half-wave pulse current, I denotes the RMS current, and t indicates the pulse duration. If the IGBT module is used in a rectifier circuit or converter circuit, an inrush current flows at startup. Do not exceed the I^2t limits. If I^2t is exceeded, take measures such as connecting a starter circuit with resistor and conductor connected in parallel between the AC power supply and the IGBT module.

3.8 EMC noise countermeasures

Amid the ongoing effort to comply with European CE marking for IGBT module-based converters, such as inverters and UPS, and with VCCI regulations in Japan, electromagnetic compatibility (EMC), suppressing EMI noise (conductive and radiating noises emitted from devices during operation) below the specifications has become an essential aspect of circuit design.

As IGBT modules continue to offer enhanced characteristics with each generation, including faster switching and lower loss, high dv/dt and di/dt during switching can cause radiation noise. Radiation noises are primarily associated with harmonic LC resonance between stray capacitances, such as semiconductor device junction capacitances, and wiring stray inductances, triggered by high dv/dt and di/dt generated from the IGBTs during turn-on (reverse recovery of the opposing arm FWD).

In order to decrease the radiation noise, it is effective to soften (lower speed) the switching characteristics, especially the turn-on characteristics, by changing the drive conditions. Refer to Chapter 7 for explanation of drive conditions.

Fig. 4-11 shows example of radiation noise characteristics when switching speed is changed with R_G. In this case, the standard R_G is 5.6Ω, but the radiation noise can be decreased by more than 10dB by doubling the R_G value (12Ω).

However, softening the switching characteristics to decrease radiation noises tends to increase the switching loss. Thus, it is important to design the drive conditions while considering the balance with the equipment operating conditions, module cooling conditions and other relevant conditions.

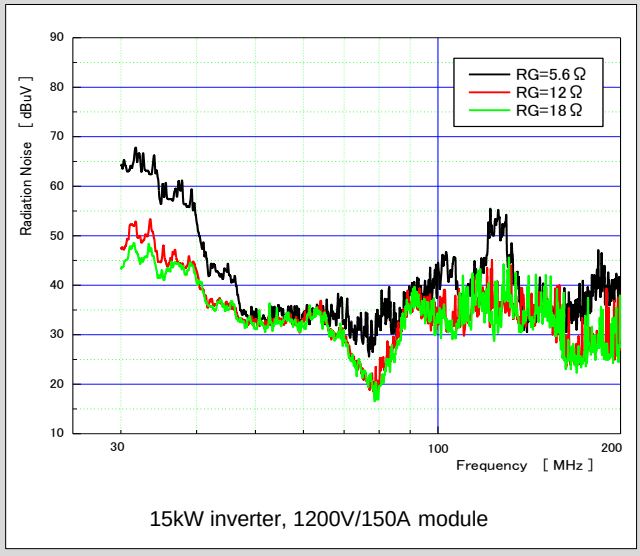


Fig. 4-11 Radiation noise (R_G dependence)

Table 4-2 shows example of general countermeasures against radiation noise. Because the cause and noise level are different according to the wiring structure, material and the circuit configuration of the equipment, it is necessary to verify which of the countermeasures is effective.

Table 4-2 Countermeasures of radiation noise

Countermeasure	Description	Remarks
Review drive conditions (reduce d*v*/d*t* and d*i*/d*t*)	Increase the R_G (particularly, turn-on side).	Switching time and switching loss increase.
	Connect a capacitor between G-E (C_{GE}).	Switching time and switching loss increase.
Connect the snubber capacitor as near as possible with the IGBT module	Minimize the wiring between the snubber capacitor and the IGBT module (connect snubber capacitor directly on module terminals).	Effective in suppressing surge voltage and d*v*/d*t* during switching.
Reduce wiring inductances	Use laminated bus bars to reduce inductances.	Effective in suppressing surge voltage and d*v*/d*t* during switching.
Filtering	Connect noise filters to the input and output of the equipment.	Various filters are commercially available
Cable shielding	Shield the input/output cables to reduce radiation noise from the cables.	
Metalize the equipment case	Metalize the equipment housing to suppress noise emitted from the device	

Chapter 5 Protection Circuit Design

This chapter describes about the protection circuit design.

1. Short Circuit (Overcurrent) Protection

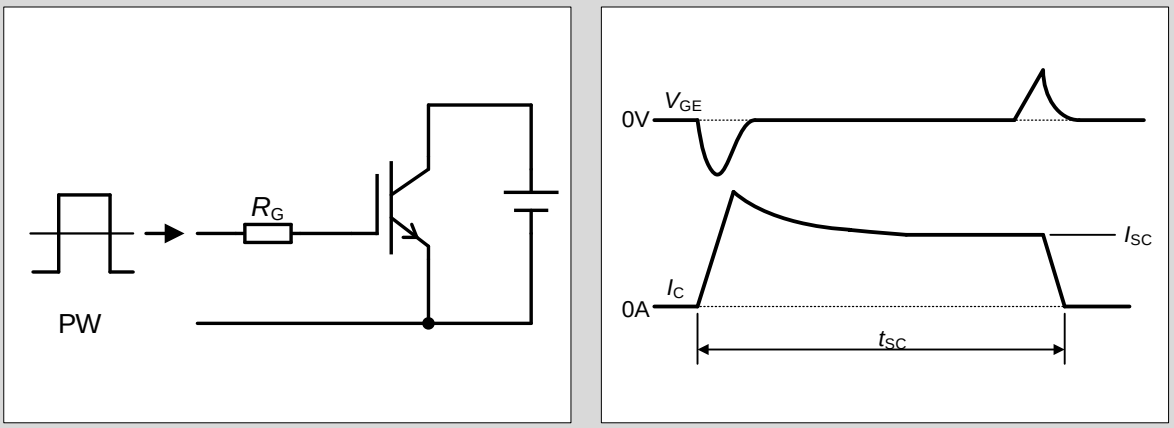
1.1 Short circuit withstand capability t_{sc}

In the event of a short circuit, the IGBT's collector current I_C will rise, and if it exceeds a certain level, the C-E voltage V_{CE} will increase sharply. Due to this characteristic, the I_C can be kept at or below a certain level during short circuit. However, the IGBT will still continue to be subjected to a heavy load of high voltage and high current. If this abnormal state continues, the IGBT will be destroyed. The time that the IGBT can withstand a short circuit without destruction is specified as short circuit withstand capability t_{sc}. The gate drive circuit must be designed so that the delay time from short circuit detection until the short circuit current cut off is shorter than t_{sc}.

The concept of short-circuit withstand capability for arm short circuit and output short circuit is explained below.

(1) Arm short circuit

Fig. 5-1 shows an arm short circuit test circuit and waveform example. As for the arm short circuit, the I_C rises sharply at the start of the short circuit and drops slightly after saturation. The short circuit (saturation) current value I_{SC} is determined by V_{GE}, device output characteristics, and T_{vj}, and is almost independent of V_{DC}, R_G, and P_W. The short circuit withstand capability is expressed by the energization time P_W and is specified after specifying the V_{GE}, T_{vj}, and V_{DC} conditions. Design the protection circuit so that when a short circuit occurs, it will be cut off within the specified short circuit withstand capability.



(a) Arm short circuit test circuit (b) Arm short circuit waveform example

Fig. 5-1 Arm short circuit test circuit and waveform

(2) Output short circuit

Fig. 5-2 shows the output short circuit test circuit and waveform example. In the output short circuit, the short circuit wire has inductance component, thus the current waveform at the start of the short circuit is different from that in the case of the arm short circuit. In this case, the current rise rate d*i*/d*t* can be expressed as follows.

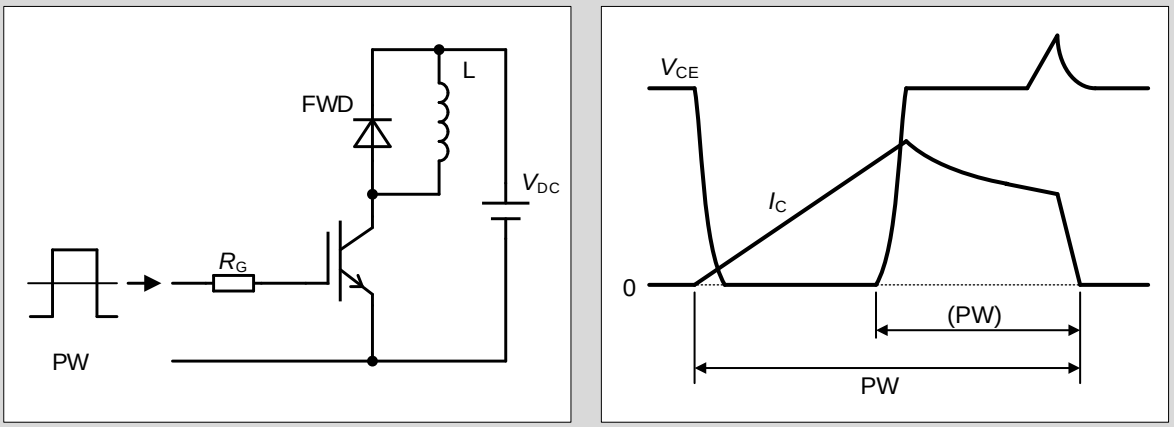
$$d_i/d_t = V_{DC}/L \ \ (A/sec)$$

If the time from the start of the short circuit is given as *t* (sec), I_C can be expressed as follows.

$$I_C = d_i/d_t \cdot t \ (A)$$

The I_C peak value depends on the inductance and the drive circuit (transient V_{GE} rise). After reaching the peak value and saturating, V_{CE} rises sharply. From here, it becomes the same situation with an arm short circuit.

The short circuit withstand capability in the case of output short circuit is shown in Fig. 5-2(b) as (P_w). During I_C rise, V_{DC} is applied to the inductance L, and the voltage across the IGBT is about $V_{CE\ (sat)}$, thus the load on the IGBT is extremely low compared to the arm short circuit. Therefore, this period is not included in the short circuit withstand capability.



(a) Output short circuit test circuit (b) Output short circuit waveform example

Fig. 5-2 Output short circuit test circuit and waveform

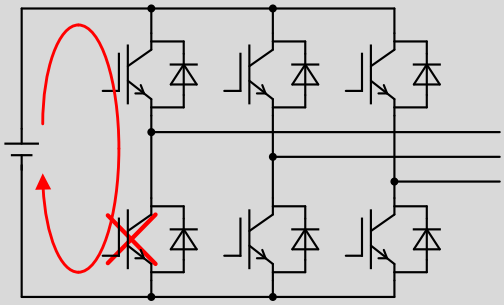
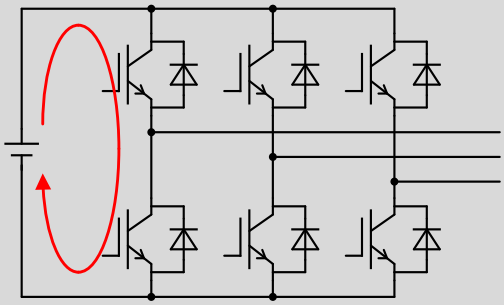
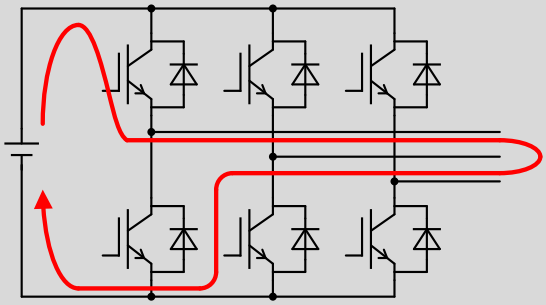
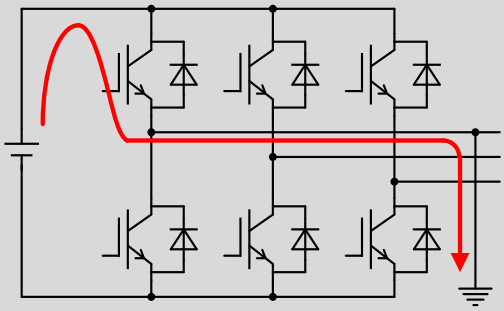
Short circuit withstand capability depends on conditions such as V_{CE}, V_{GE}, and T_{vj}. Generally, the higher the V_{DC} and the higher the T_{vj}, the shorter the short circuit withstand capability.

Also, please note that V_{GE} may rise during short circuit. Please refer to the application manual or technical document for the short circuit capability of each IGBT series.

1.2 Short circuit modes and causes

Table 5-1 shows the short circuit modes and causes that occur in inverters.

Table 5-1 Short circuit modes and causes

Short circuit mode	Cause
Arm short circuit 	IGBT or diode destruction.
Series arm short circuit 	Control circuit / drive circuit failure or malfunction due to noise.
Output short circuit 	Miswiring or dielectric breakdown of load
Ground fault 	Miswiring or dielectric breakdown of load

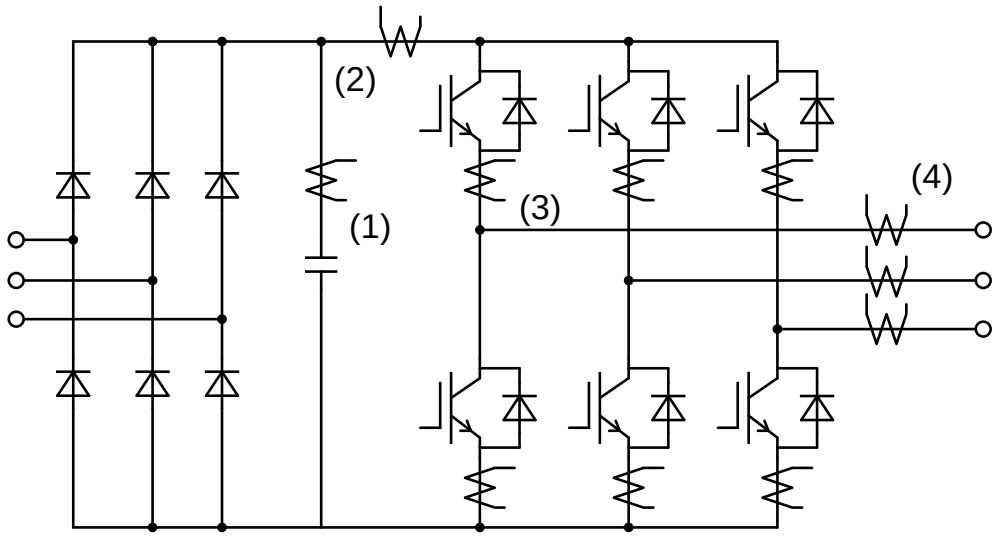
1.3 Short circuit (overcurrent) detection method

(1) Detection by overcurrent detector

As mentioned, in the event of a short circuit, the IGBT must be turned off as soon as possible. Therefore, the time from short circuit detection to the completion of turn-off must be as short as possible.

Since the IGBT turns off very fast, if the short circuit is turned off with a normal gate drive signal, a large surge voltage will be generated, and the IGBT may be destroyed by overvoltage (RBSOA destruction). Therefore, it is recommended to turn off the IGBT slowly (soft turn-off).

Fig. 5-3 shows the overcurrent detectors position in an inverter circuit, and Table 5-2 shows the features and the types of short circuit that can be detected by each method. Consider what kind of protection is necessary, and select the most appropriate form of detection.



Overcurrent detector position	Types of short circuits that can be detected
(1), (2), (3)	・Arm short circuit ・Series arm short circuit ・Output short circuit ・Ground fault
(4)	・Output short circuit ・Ground fault

Fig. 5-3 Overcurrent detector position

Table 5-2 Overcurrent detector positions and their features

Overcurrent detector position	Feature	Types of short circuits that can be detected
In series with smoothing capacitor Fig. 5-3/(1)	• AC current transducer can be used • Low detection precision	• Arm short circuit • Series arm short circuit • Output short circuit • Ground fault
At inverter input Fig. 5-3/(2)	• DC current transducer is required • Low detection precision	• Arm short circuit • Series arm short circuit • Output short circuit • Ground fault
In series with each IGBT Fig. 5-3/(3)	• DC current transducer is required • High detection precision	• Arm short circuit • Series arm short circuit • Output short circuit • Ground fault
At inverter output Fig. 5-3/(4)	• AC current transducer can be used for equipment with high frequency output • High detection precision	• Output short circuit • Ground fault

(2) Detection by $V_{CE(sat)}$

This method can protect against all types of short circuit shown in Table 5-1. Since the operations from overcurrent detection to protection are done on the drive circuit side, this method offers the fastest protection possible. Fig. 5-4 shows an example of short circuit protection circuit using $V_{CE(sat)}$ detection method.

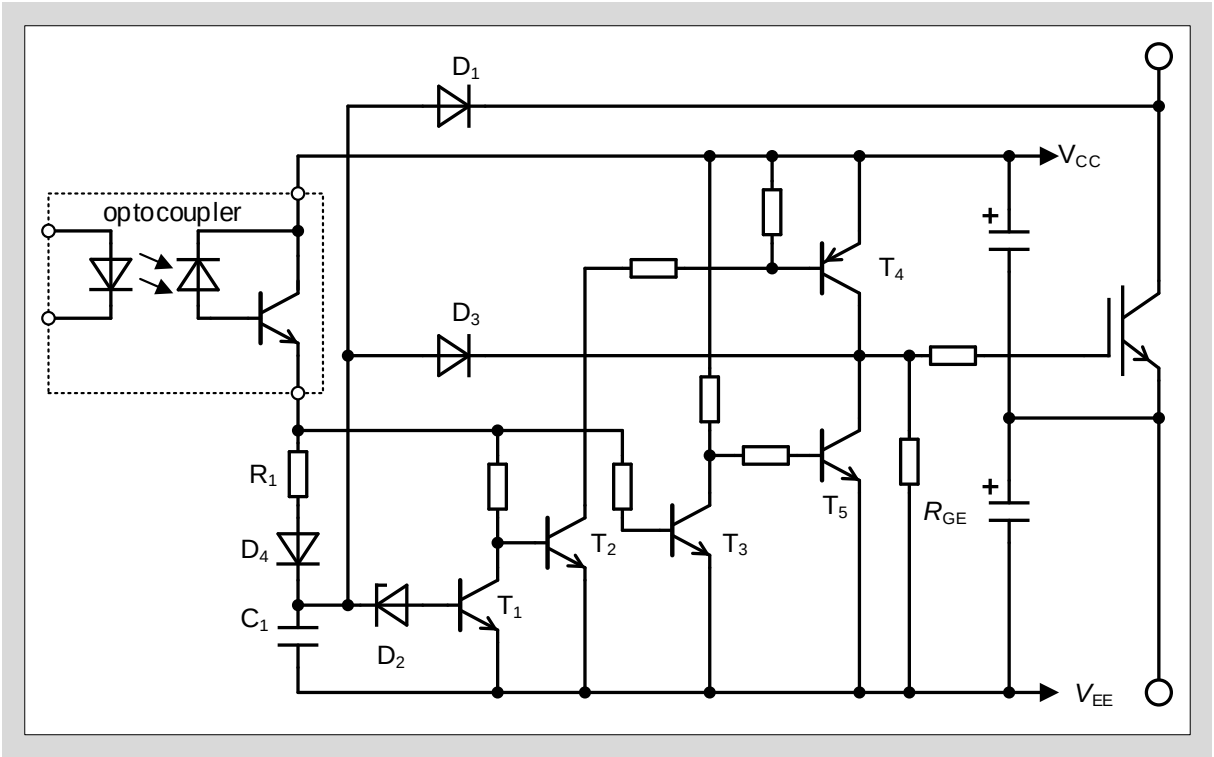


Fig. 5-4 Short-circuit protection circuit using $V_{CE(sat)}$ detection method

This circuit uses diode D_1 to constantly monitor the C-E voltage.

When the optocoupler is turned on, transistors T_2 and T_4 are turned on and a positive gate voltage is applied to the IGBT. Also, the capacitor C_1 is charged through the resistor R_1 and diode D_4. The operation changes depending on the voltage of capacitor C_1.

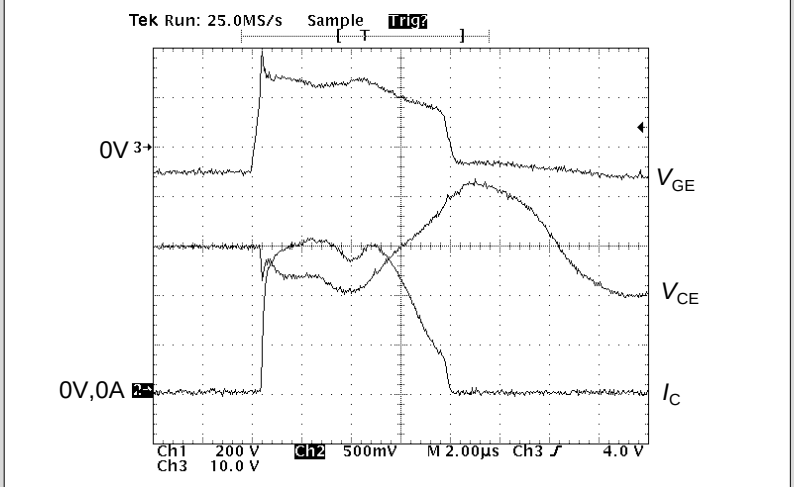
【Short circuit protection operation】

If a short circuit occurs after the IGBT is turned on, the V_{CE} of the IGBT rises. When V_{CE} becomes higher than the voltage of [C_1 - D_1 (V_F - V_{EE})], diode D_1 is turned off and the voltage of capacitor C_1 rises again. When the voltage of capacitor C_1 becomes higher than [V_Z of Zener diode D_2 + V_{BE} of transistor T_1], short circuit protection operates.

In the short circuit protection operation, a current flows through Zener diode D_2 to the base of transistor T_1, turning it on. When transistor T_1 is turned on, transistors T_2 and T_4 are turned off, and the applied positive gate voltage is cut off. Since the optocoupler is on, the transistor T_3 is on and transistor T_5 is off. Since the transistors T_4 and T_5 are turned off at the same time, the gate accumulated charge is slowly discharged through the R_{GE}. This effect can suppress the generation of excessive surge voltage when the IGBT turns off. Fig. 5-5 shows an example of the short circuit protection waveform.

【Normal operation】

After the IGBT is turned on, the IGBT is kept on by keeping the voltage of capacitor C_1 below [V_Z of the Zener diode D_2 + V_{BE} of transistor T_1]. When the optocoupler is turned off, the transistors T_2, T_4 turn off, transistor T_3 turns off, and transistor T_5 turns on, applying a negative gate voltage to the IGBT. The charge on capacitor C_1 is discharged through diode D_3 and transistor T_5 and reset to 0V. As can be seen from the above operation sequence, short circuit protection is monitored on each pulse.



E_d=600V, V_{GE}=+15V/-5V, R_G=3.3Ω, T_{vj}=125°C

V_{CE}=200V/div, I_C=250A, V_{GE}=10V/div, t=2µs/div

Fig. 5-5 Waveforms during short circuit protection

2. Overvoltage Protection

2.1 Cause of overvoltage and suppression methods

(1) Cause of overvoltage

Due to the high switching speed of IGBTs, during turn-off or FWD reverse recovery, the current change rate d*i*/d*t* is very high. Therefore, the circuit wiring inductance around the module L_S can generate a high surge voltage $V_{CEP}=L_S \cdot (di/dt)$.

Fig. 5-6 shows a chopper circuit for measuring the turn-off surge voltage, and Fig. 5-7 shows the switching waveforms.

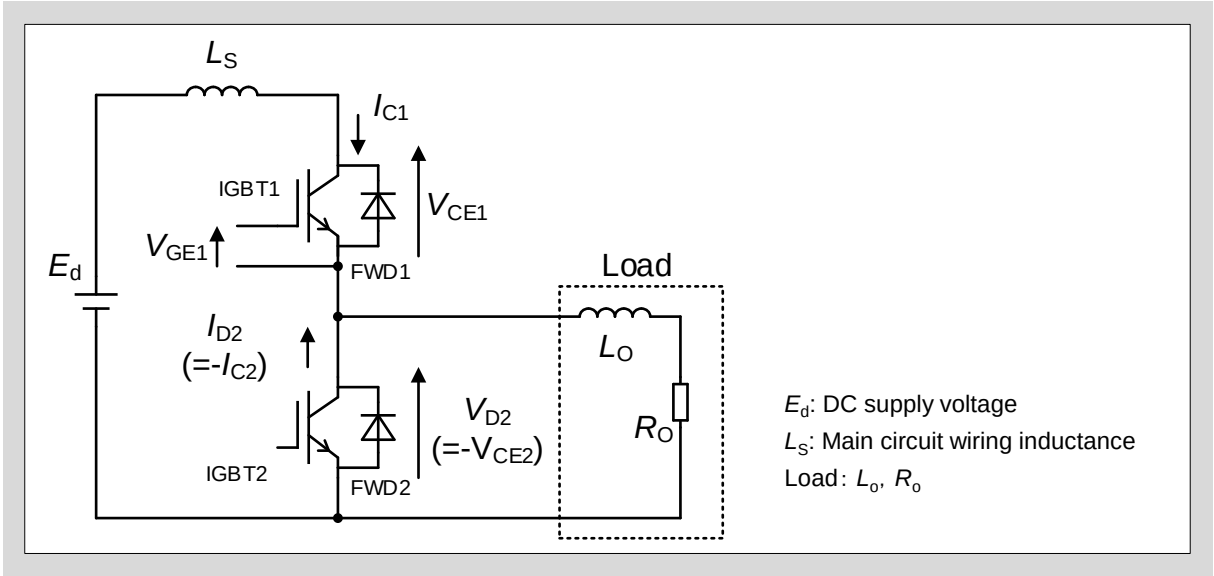


Fig. 5-6 Chopper circuit

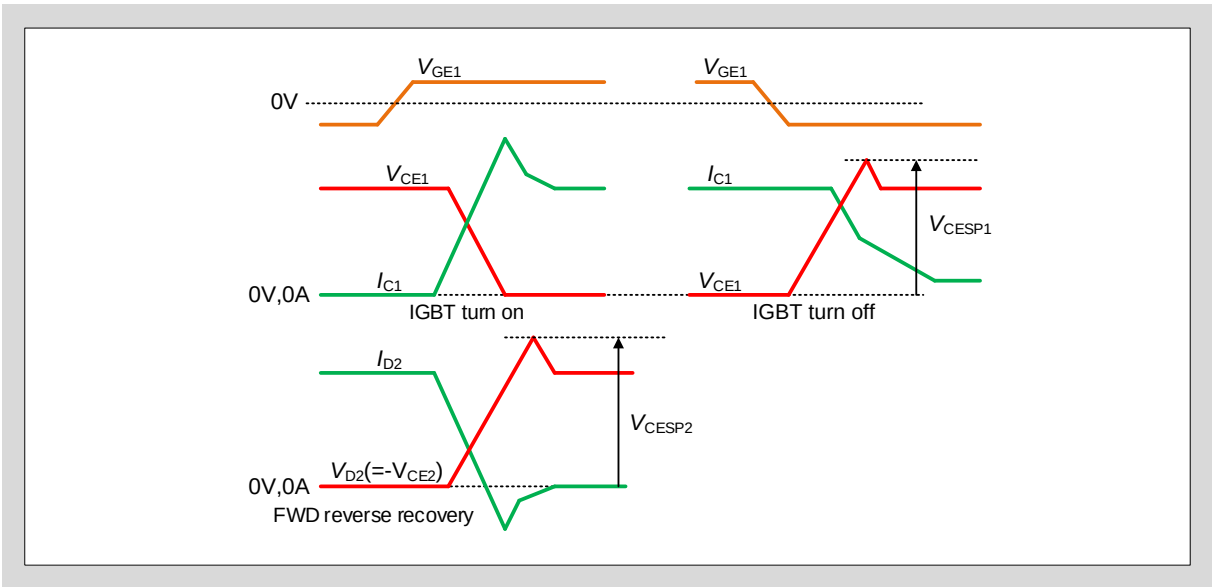


Fig. 5-7 Switching waveforms

The peak value of turn-off surge voltage V_{CESP} can be calculated as follows.

$$V_{CESP} = E_d + (-L_S \cdot \frac{dI_C}{dt})$$

dI_C/dt: Maximum I_C change rate at turn-off

If V_{CESP} exceeds the V_{CES} rating, the module will be destroyed.

(2) Overvoltage suppression methods

The following methods are available for suppressing turn-off surge voltage.

a. Suppress the surge voltage by adding a protection circuit such as a snubber circuit to the IGBT. Use a film capacitor and place it as close as possible to the IGBT in order to suppress high frequency surge voltage.
b. Adjust the $-V_{GE}$ and R_G of the drive circuit in order to reduce the d*i*/d*t*. (For details, refer to Chapter 7, 'Gate Drive Circuit Design')
c. Place the DC capacitor as close as possible to the IGBT in order to reduce L_S. Use a low impedance type capacitor.
d. Reduce the L_S of the main circuit and snubber circuit by using thicker and shorter wires. It is also very effective to use laminated bus bars.
e. Use an active clamp circuit. The surge voltage is suppressed to approximately equal to the Zener voltage of the Zener diode.

2.2 Types of snubber circuits and their features

Snubber circuits can be classified into two types: individual snubber circuit and lump snubber circuit. Individual snubber circuits are connected to each IGBT, while lump snubber circuits are connected between the DC power supply bus and the ground for centralized protection.

(1) Individual snubber circuits

Examples of typical individual snubber circuits are as follows.

a. RC snubber circuit
b. Charge-discharge RCD snubber circuit
c. Discharge-suppressing RCD snubber circuit

Table 5-3 shows the schematic and features of each type of individual snubber circuit.

(2) Lump snubber circuits

Examples of typical lump snubber circuits are as follows.

a. C snubber circuit
b. RCD snubber circuit

Lump snubber circuits are becoming increasingly popular due to circuit simplification.

Table 5-4 shows the schematic and features of each type of lump snubber circuit. Table 5-5 shows the guideline for determining lump C snubber capacitance. Fig. 5-8 shows an example of turn-off waveforms of IGBT with lump C snubber circuit.

Table 5-3 Individual snubber circuits

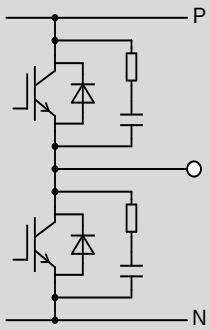
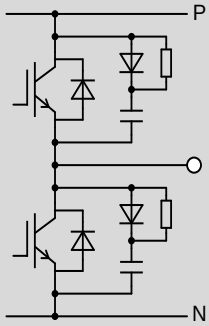
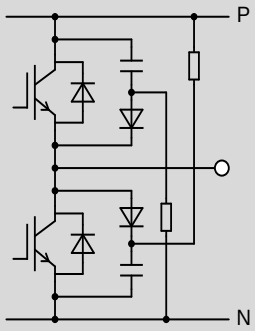
Snubber circuit schematic	Features (Notes)
RC snubber circuit 	• The surge voltage suppression effect is greater than that of a lump snubber circuit. • When applied to large capacity IGBTs, the snubber resistance must be low. As a result, the current at turn-on increases and increase the IGBT load.
Charge-discharge RCD snubber circuit 	• Unlike the RC snubber circuit, a snubber diode is added. Thus, snubber resistance can be increased, and decrease the IGBT load at turn-on . • The power dissipation loss by the snubber resistance of this circuit can be calculated as follows. $P = \frac{L_S \cdot I_o^2 \cdot f}{2} + \frac{C_S \cdot E_d^2 \cdot f}{2}$ L_S: Wiring inductance of main circuit I_O: Collector current at IGBT turn-off C_S: Capacitance of snubber capacitor E_d: DC power supply voltage f: Switching frequency
Discharge-suppressing RCD snubber circuit 	• Power dissipation loss of snubber circuit is small. • The power dissipation loss by the snubber resistance of this circuit can be calculated as follows. $P = \frac{L_S \cdot I_o^2 \cdot f}{2}$ L_S: Wiring inductance of main circuit Io: Collector current at IGBT turn-off f :Switching frequency

Table 5-4 Lump snubber circuits

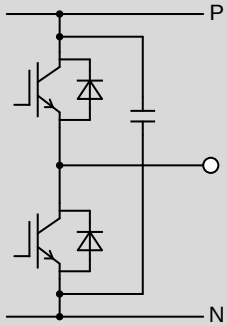
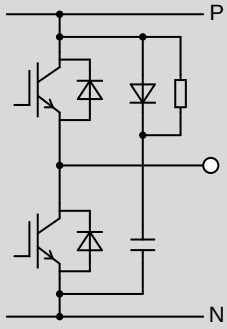
Snubber circuit schematic	Features (Notes)
C snubber circuit 	• This is the simplest snubber circuit. • The LC resonance circuit, which consists of main circuit inductance and snubber capacitor, may cause the C-E voltage to oscillate.
RCD snubber circuit 	• If the snubber diode is selected incorrectly, a high surge voltage will be generated or the voltage may oscillate during reverse recovery of the snubber diode.

Table 5-5 Guideline for determining lump C snubber capacitance

Item / Module rating		Gate drive conditions *1		Main circuit inductance (μH)	Snubber capacitance C_S (μF)
		$-V_{GE}$ (V)	R_G (Ω)		
600V	50A	≦15	≧43	-	0.47
	75A		≧30		
	100A		≧13		
	150A		≧9	≦0.2	1.5
	200A		≧6.8	≦0.16	2.2
	300A		≧4.7	≦0.1	3.3
	400A		≧6	≦0.08	4.7
1200V	50A	≦15	≧22	-	0.47
	75A		≧4.7		
	100A		≧2.8		
	150A		≧2.4	≦0.2	1.5
	200A		≧1.4	≦0.16	2.2
	300A		≧0.93	≦0.1	3.3

*1: Standard gate drive conditions of V series IGBT is shown

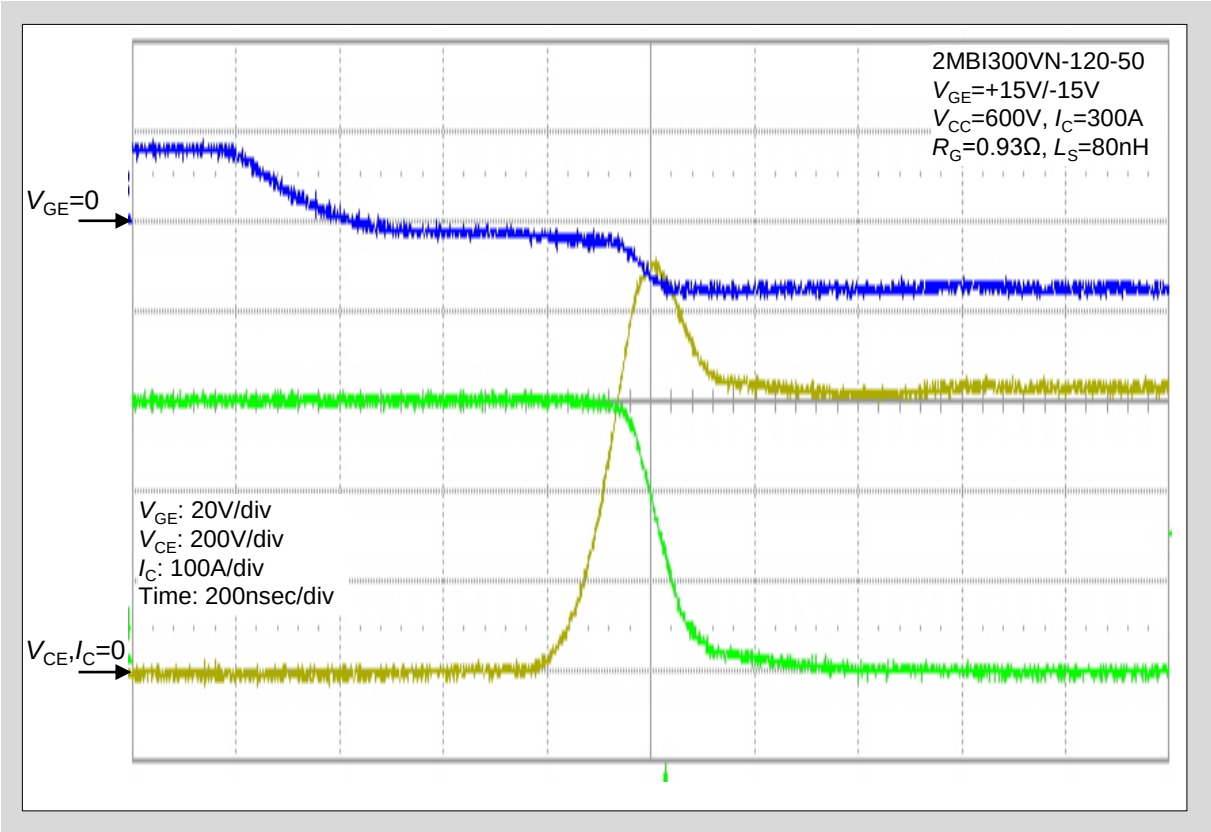


Fig. 5-8 Turn-off waveforms of IGBT with lump C snubber circuit

2.3 Discharge-suppressing RCD snubber circuit design

The discharge-suppressing RCD snubber circuit is considered the most suitable snubber circuit for IGBT. The basic design method of this circuit is as follows.

(1) Study of applicability

Fig. 5-9 shows the turn-off locus of IGBT with discharge-suppressing RCD snubber circuit. Fig. 5-10 shows the IGBT turn-off waveform.

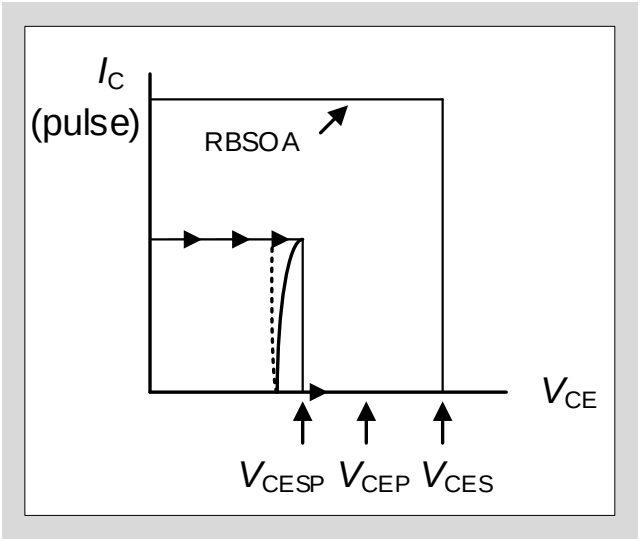


Fig. 5-9 Turn-off locus of IGBT

In the discharge-suppressing RCD snubber circuit operates after V_{CE} of the IGBT exceeds the DC power supply voltage. The ideal operation trajectory is shown by the dotted line.

However, in actual equipment, there is surge voltage at turn-off due to the wiring inductance of the snubber circuit and the transient forward voltage of the snubber diode, thus the actual waveform is as shown by the solid line.

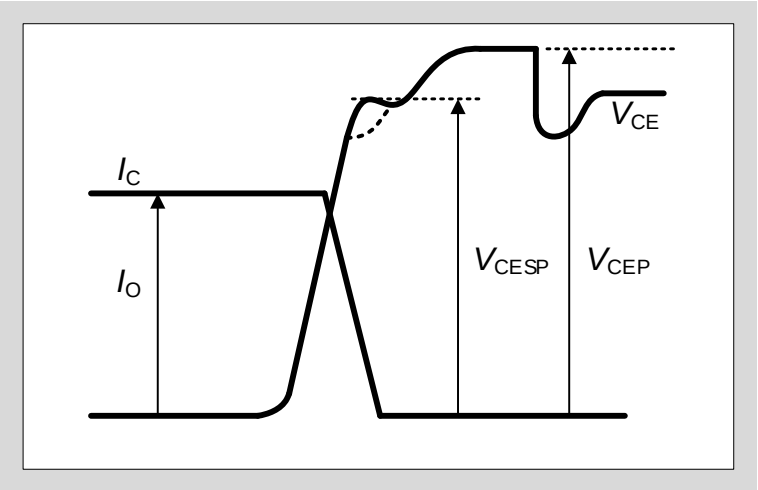


Fig. 5-10 Turn-off waveform with discharge-suppressing RCD snubber circuit

The discharge-suppressing RCD snubber circuits applicability is decided by whether the turn-off locus after applying the snubber circuit is within the RBSOA.

The surge voltage at IGBT turn-off is calculated as follows.

$$V_{CESP} = E_d + V_{FM} + (-L \cdot \frac{dI_c}{d_t})$$

E_d :DC power supply voltage
V_{FM} :Transient forward voltage of snubber diode
The reference values are as follows.
600V class: 20 to 30V
1200V class: 40 to 60V
L :Snubber circuit wiring inductance
dI_c/d_t :Maximum I_C change rate at IGBT turn-off

(2) Calculating the snubber capacitance (C_S)

The capacitance of the snubber capacitor is calculated as follows.

$$C_S = \frac{L_S \cdot I_O^2}{(V_{CEP} - E_d)^2}$$

L_S :Main circuit wiring inductance
I_o :Collector current at IGBT turn-off
V_{CEP} :Snubber capacitor peak voltage
E_d :DC power supply voltage

V_{CEP} must be limited to less than V_{CES} of the IGBT. Use a snubber capacitor with good high-frequency characteristics such as a film capacitor.

(3) Calculating the snubber resistance (R_S)

The function of the snubber resistor is to discharge the accumulated charge in the snubber capacitor before the next IGBT turn-off. To discharge 90% of the accumulated charge by the next IGBT turn-off, the snubber resistance is calculated as follows.

$$R_S \leq \frac{1}{2.3 \cdot C_S \cdot f}$$

R_S :Snubber resistance
C_S :Snubber capacitance
f :Switching frequency

If the snubber resistance is set too low, the snubber circuit current will oscillate and the peak collector current at the IGBT turn-off will increase. Therefore, set the snubber resistance as high as possible within the calculated range.

Irrespective of the resistance value, the power dissipation of the snubber resistor $P(R_S)$ is calculated as follows.

$$P(R_S) = \frac{L_S \cdot I_O^2 \cdot f}{2}$$

$P(R_S)$:Power dissipation of snubber resistor
L_S :Main circuit wiring inductance
I_o :Collcetor current at IGBT turn-off
f :Switching frequency

(4) Snubber diode selection

The transient forward voltage of the snubber diode is one of the cause of surge voltage at IGBT turn-off. If the reverse recovery time of the snubber diode is too long, the power dissipation loss of the snubber diode will also be much higher during high frequency switching. Also, if the reverse recovery of the snubber diode is too hard, then the IGBT C-E voltage will oscillate greatly.

Therefore, select a snubber diode that has a low transient forward voltage, a short reverse recovery time, and asoft reverse recovery.

(5) Snubber circuit wiring precautions

The snubber circuit wiring inductance is one of the main cause of surge voltage, therefore it is important to reduce the wiring inductance, as well as considering the layout of circuit components.

2.4 Example of surge voltage characteristics

Surge voltage characteristics depend on the operation, drive conditions, circuit conditions, etc. Generally, surge voltage tends to increase when V_{CE} is higher, the circuit inductance is larger, and I_C is larger.

As an example, the current dependency of surge voltage during IGBT turn-off and FWD reverse recovery is shown in Fig. 5-11. As shown in this figure, the surge voltage at IGBT turn-off becomes higher when current is higher, but the surge voltage during FWD reverse recovery tends to increases at the low current region. Generally, the surge voltage during reverse recovery increases at low current that is about 1~10% of the rated current.

The surge voltage shows various characteristics depending on the operation, drive conditions, circuit conditions, etc. Therefore, it is necessary to confirm that the current and voltage are within the RBSOA described in the specification under all operating conditions of the system.

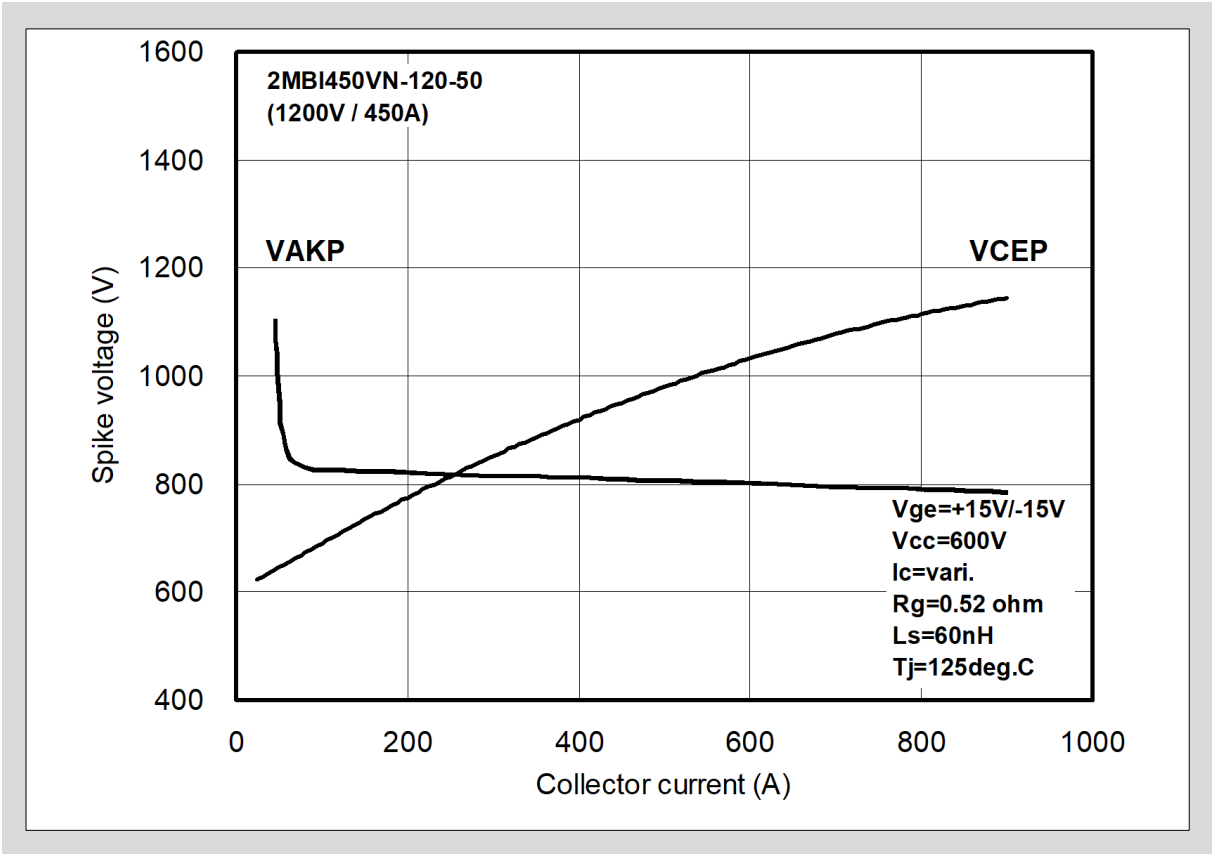


Fig. 5-11 Current dependency of surge voltage during IGBT turn-off and FWD reverse recovery

2.5 Overvoltage suppression circuit -example of clamp circuit configuration-

In general, surge voltage can be suppressed by means of decreasing the stray inductance or installing a snubber circuit. However, it may be difficult to suppress the surge voltage under depending on the operating conditions of the equipment. For such cases, it is effective to use active clamp circuits.

Fig. 5-12 shows an example of active clamp circuit. The circuit configuration adds a Zener diode at C-G of the IGBT, and connect a diode in anti-series with the Zener diode.

When voltage exceeding the Zener voltage of the Zener diode is applied on C-E, the Zener diode breakdown and current flows from collector to the IGBT gate. Positive voltage is added to V_{GE} by this current flowing through R_G. When V_{GE} exceeds the gate threshold voltage $V_{GE(th)}$, I_C flows through the IGBT, and V_{CE} is clamped to approximately equal to the Zener voltage of the Zener diode. In thi s way, surge voltage can be suppressed.

On the other hand, since the active clamp circuit turn on the IGBT, the d*i*/d*t* at turn-off becomes slower than before the addition of the clamp circuit, resulting in a longer turn-off time (refer to Fig. 5-13). As this will increase the switching loss, make sure to apply the clamp circuit after verifying if this has no problem with the design of the equipment.

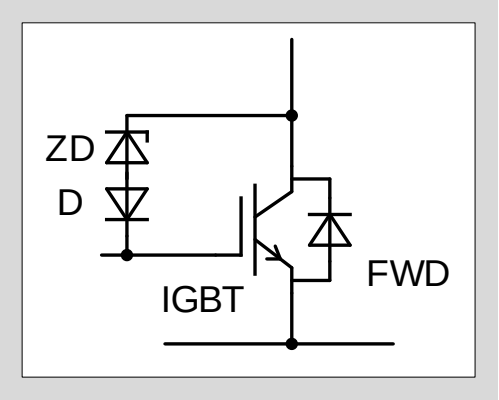


Fig. 5-12 Active clamp circuit

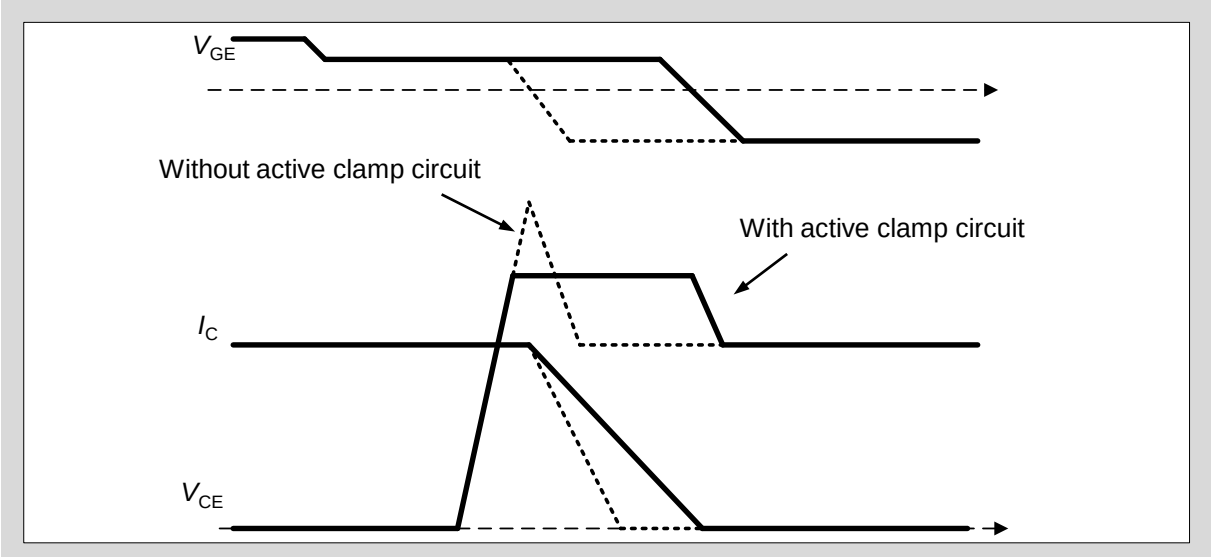


Fig. 5-13 Waveform example when active clamp circuit is applied

Chapter 6 Cooling Design

1. Power Loss of IGBT Module

The IGBT module consists of IGBT and FWD, and the sum of power loss of each chip is the total power loss of the IGBT module. As shown in Fig. 6-1, the power loss include conduction loss and switching loss. The types of power loss is summarized in Fig. 6-2.

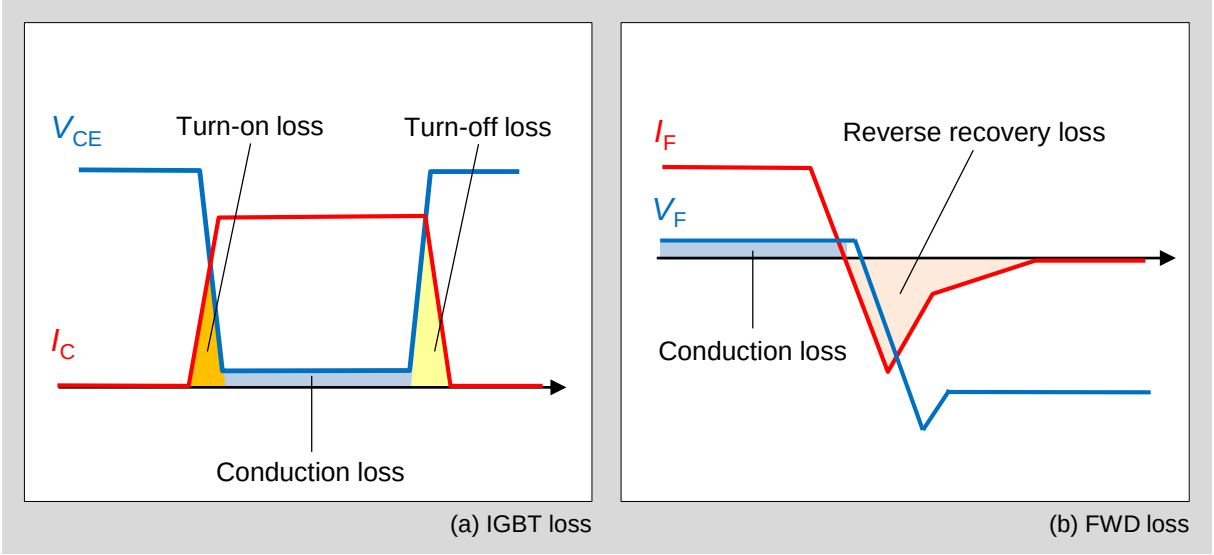


Fig. 6-1 Switching waveform and power loss of IGBT and FWD

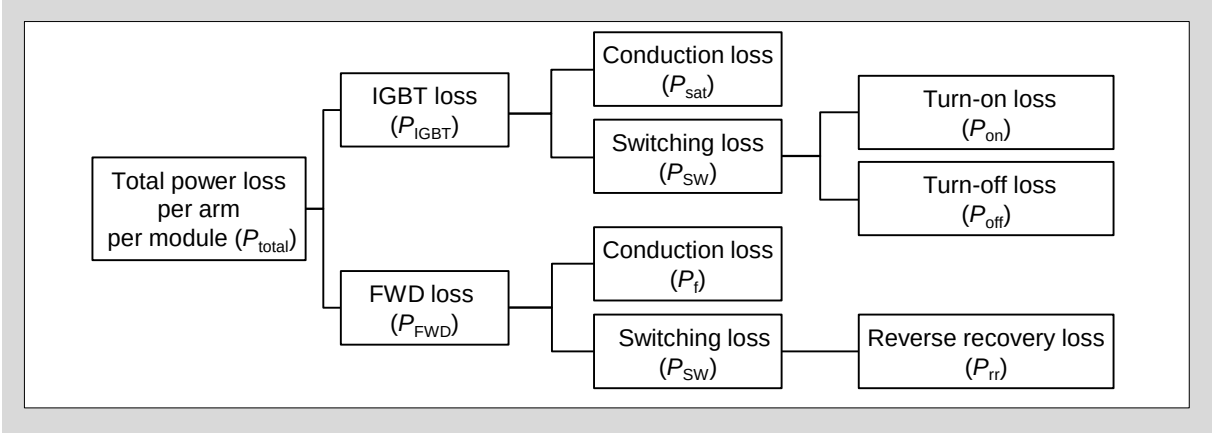


Fig. 6-2 Classification of IGBT module power loss

For RC-IGBT, although the RC-IGBT combines IGBT and FWD in one chip, by considering the power loss generated at IGBT part and FWD part, the concept of power loss is the same as that of a normal IGBT module. For RB-IGBT, although the RB-IGBT does not have FWD part, there are cases where RB-IGBT is operated as FWD, which causes P_{sat} and P_{rr}.

The conduction loss of the IGBT part is calculated from the $V_{CE(sat)}$ -I_C characteristic, and the conduction loss of the FWD part is calculated from the V_F-I_F characteristic shown in the datasheet. In addition, each switching loss is calculated from the E_{on}-I_C, E_{off}-I_C, E_{rr}-I_F characteristics. Heat dissipation design is performed based on these power loss so that the T_{vj} of the IGBT and FWD do not exceed the temperature rating. Therefore, calculate the power loss using the data when T_{vj} is high.

2. Power Loss Calculation Method of Boost Chopper Circuit

In the case of a boost chopper circuit as shown in Fig. 6-3, if the current flowing through the IGBT (T_1) and FWD (D_1) is considered to be a continuous rectangular waveform, the power loss per unit time of T_1 and D_1 (unit: W) can be approximated by the following formulas.

P_{IGBT} = Conduction loss + Turn-on loss + Turn-off loss

$$= V_{CE(sat)} \cdot I_C \cdot d + (E_{on} + E_{off}) \cdot f_C \cdot (\frac{V_{cc}}{V_{cc0}})^{\alpha} \quad \text{.....(1)}$$

P_{FWD} = Conduction loss + Reverse recovery loss

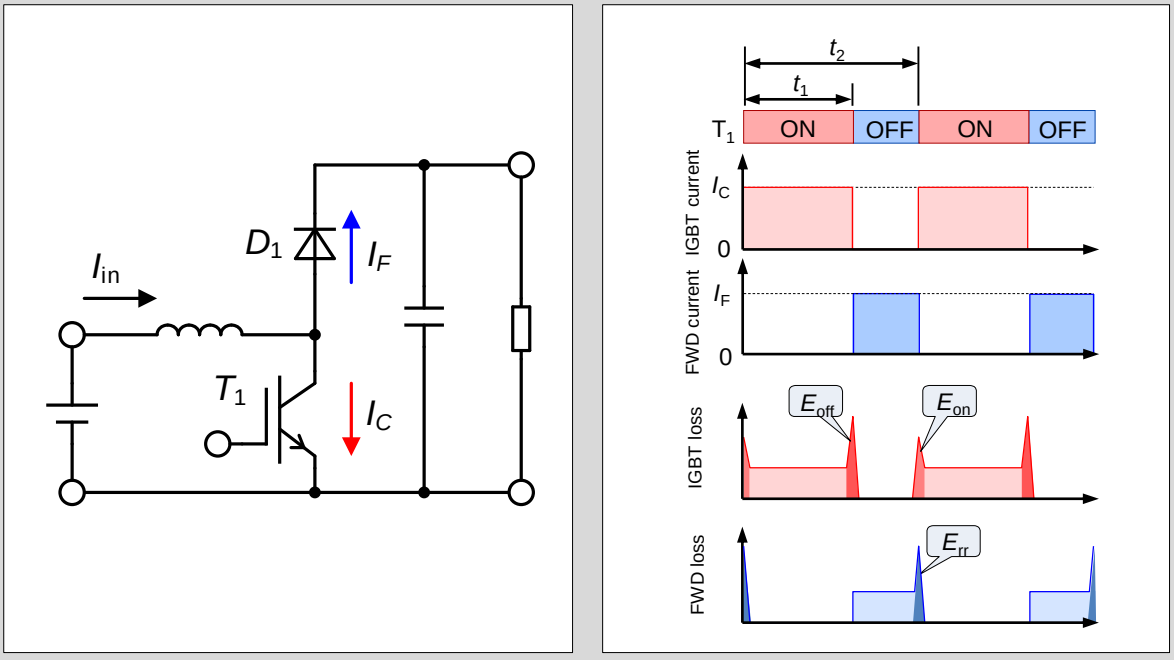
$$= V_F \cdot I_F \cdot (1 - d) + E_{rr} \cdot f_C \cdot (\frac{V_{CC}}{V_{CC0}})^{\alpha} \quad \text{.....(2)}$$

where

d	:IGBT ON duty= t_1 / t_2
f_c	:Switching frequency = 1 / t_2
V_{CC}	:Switching voltage
V_{CC0}	:Switching voltage of switching loss data in datasheet
α	:Coefficient of switching voltage dependence to switching energy

If we consider the switching energy to be proportional to the switching voltage, then we can set α=1.

On the other hand, the values of $V_{CE(sat)}$, V_F, E_{on}, E_{off}, and E_{rr} depend on the junction temperature T_{vj} of the device. Thus, if the T_{vj} is different from the T_{vj} described in the datasheet, refer to the T_{vj} dependency graphs in the datasheet for conversion. The values of E_{on}, E_{off}, and E_{rr} also depend on the gate resistance value R_G, so refer to the R_G dependency graph in the datasheet for conversion.



(a) Boost chopper circuit (b) Waveforms, power loss of boost chopper circuit

Fig. 6-3 Power loss in boost chopper circuit

3. Power Loss Calculation Method of 3-phase 2-level PWM Inverter Circuit

As shown in Fig. 6-4, the current values of the IGBT and FWD in a 3-phase 2-level PWM inverter are constantly changing. Thus, an accurate calculation of the power loss requires complex calculations. Here, we introduce a simple method for calculating the power loss of the IGBT and FWD in an inverter circuit using the characteristic curve approximation formula of the IGBT module.

The following conditions are assumed for the calculation.

- The inverter is a PWM controlled 3-phase 2-level inverter
- PWM is triangle wave comparison sinusoidal modulation method
- The output current should be an ideal sine wave

Assuming that the RMS value of the output phase current of the inverter is I_o, the current waveform of the sine wave is expressed by the following formula.

$$i_O(\theta) = \sqrt{2} \cdot I_O \cdot \sin\theta \qquad \text{.....(3)}$$

The on-duty waveform $d(\theta)$ of the IGBT is expressed by the following formula, where m is the modulation factor and φ is the delay power factor of the current.

$$d(\theta) = \frac{1 + m \cdot \sin(\theta + \varphi)}{2} \qquad \text{.....(4)}$$

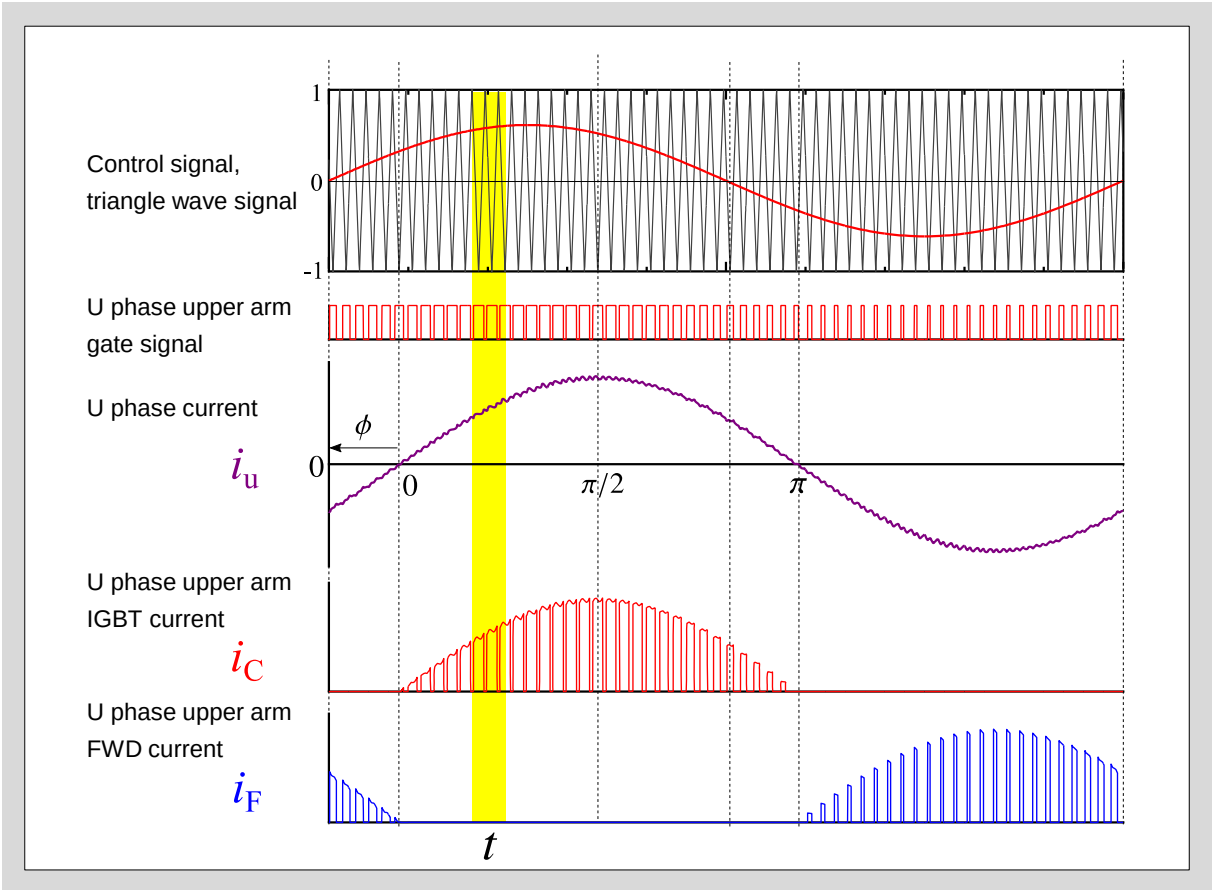


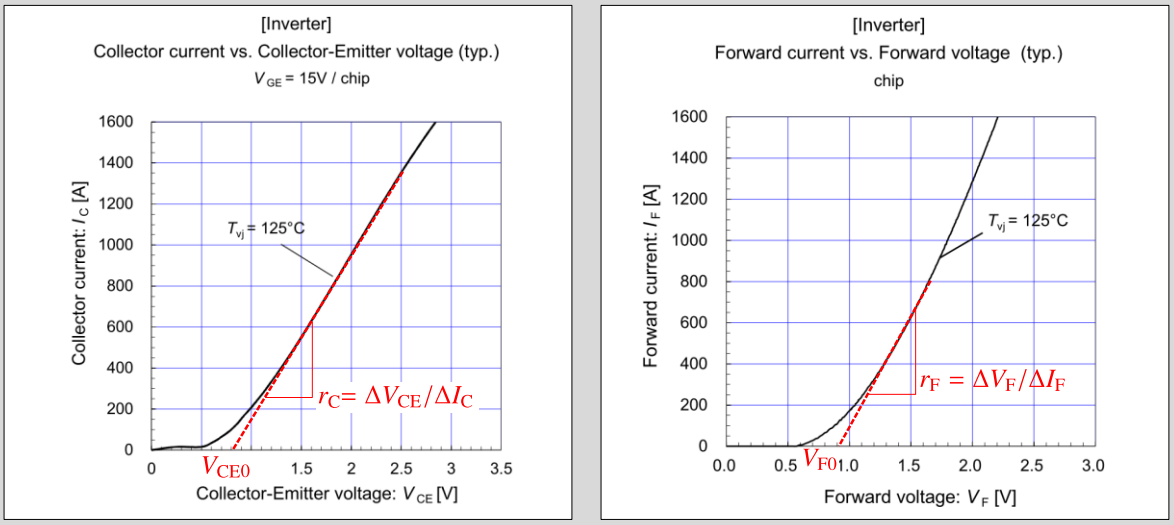
Fig. 6-4 Operating waveform of a 3-phase 2-level PWM inverter

When I_C flows through the IGBT, Collector-Emitter saturation voltage $V_{CE(sat)}$ is generated. $V_{CE(sat)}$ value depends on I_C, and the $V_{CE(sat)}$- I_C graph is shown in the datasheet. In order to calculate the conduction loss of the IGBT, the I_C dependence of $V_{CE(sat)}$ is linearly approximated as shown in Fig. 6-5, and is expressed by the following formula.

$$V_{CEsat} = r_C \cdot I_C + V_{CEO} \quad \text{.....(5)}$$

Similarly, the I_F dependence of FWD forward voltage V_F is expressed by the following formula when linearly approximated.

$$V_F = r_F \cdot I_F + V_{FO} \quad \text{.....(6)}$$



(a) IGBT output characteristics (b) FWD output characteristics

Fig. 6-5 Linear approximation of output characteristics

From formula (3), (4) and (5), the IGBT conduction loss P_{sat} per arm is calculated as follows.

$$P_{sat} = \frac{1}{2\pi}\int_0^{\pi} \{i_O(\theta) \cdot V_{CEsat}(\theta) \cdot d(\theta)\} d\theta$$
$$= 2I_O^2 \cdot rc\left(\frac{1}{8} + \frac{m}{3\pi}\cos\varphi\right) + \sqrt{2} \cdot I_O \cdot V_{CEO}\left(\frac{1}{2\pi} + \frac{m}{8}\cos\varphi\right) \quad \text{.....(7)}$$

Similarly, the FWD conduction loss P_f per arm is calculated as follows.

$$P_f = \frac{1}{2\pi}\int_{\pi}^{2\pi} \{-i_O(\theta) \cdot V_F(\theta) \cdot d(\theta)\} d\theta$$
$$= 2I_O^2 \cdot r_F\left(\frac{1}{8} - \frac{m}{3\pi}\cos\varphi\right) + \sqrt{2} \cdot I_O \cdot V_{FO}\left(\frac{1}{2\pi} - \frac{m}{8}\cos\varphi\right) \quad \text{.....(8)}$$

Next, in order to calculate the switching loss, the approximate expression of the I_C dependence graph of E_{on}, E_{off}, and E_{rr} described in the datasheet are obtained. As shown in Fig. 6-6, if the I_C dependence curve of the switching energy is linearly approximated, and the coefficient of switching voltage dependence is set as α = 1, E_{on}, E_{off}, and E_{rr} can be expressed by the following formulas, respectively.

$$E_{on}(I_C) = k_{on} \cdot I_C \cdot \left(\frac{V_{CC}}{V_{CC0}}\right) \quad \text{.....(9)}$$

$$E_{off}(I_C) = k_{off} \cdot I_C \cdot \left(\frac{V_{CC}}{V_{CC0}}\right) \quad \text{.....(10)}$$

$$E_{rr}(I_F) = k_{rr} \cdot I_F \cdot \left(\frac{V_{CC}}{V_{CC0}}\right) \quad \text{.....(11)}$$

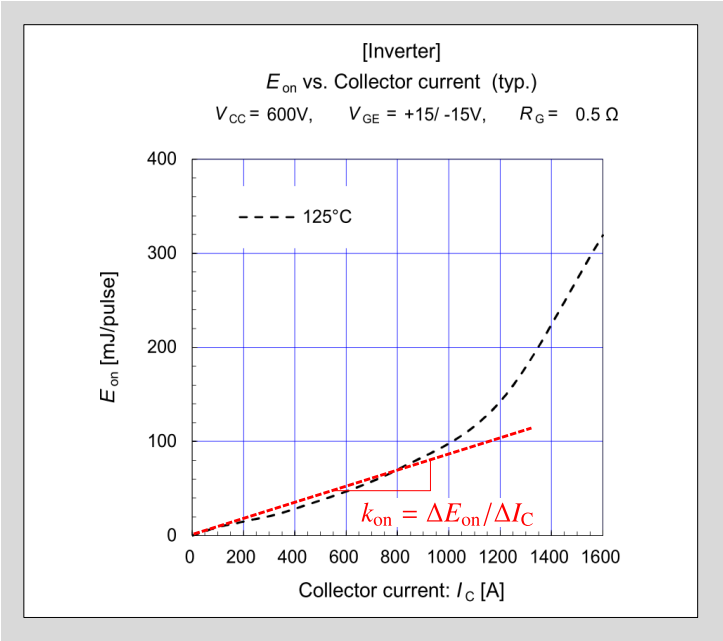


Fig. 6-6 Approximation of I_C dependence of switching energy

Using formula (9), the IGBT turn-on loss P_{on} per arm can be calculated by the following formula.

$$P_{on} = \frac{1}{2\pi}\int_0^{\pi}\left\{k_{on}(\sqrt{2}\cdot I_o\cdot\sin\theta)\cdot\frac{V_{CC}}{V_{CC0}}\cdot f_{SW}\right\}d\theta$$

$$= \frac{\sqrt{2}}{\pi}k_{on}\cdot I_O\cdot\frac{V_{CC}}{V_{CC0}}\cdot f_{SW} \quad \text{.....(12)}$$

Similarly, the IGBT turn-off loss P_{off} and the FWD reverse recovery loss P_{rr} can be calculated by the following formulas, respectively.

$$P_{off} = \frac{\sqrt{2}}{\pi}\cdot k_{off}\cdot I_O\cdot\frac{V_{CC}}{V_{CC0}}\cdot f_{SW} \quad \text{.....(13)}$$

$$P_{rr} = \frac{\sqrt{2}}{\pi}\cdot k_{rr}\cdot I_O\cdot\frac{V_{CC}}{V_{CC0}}\cdot f_{SW} \quad \text{.....(14)}$$

From the above calculation, the IGBT power loss P_{IGBT} and the FWD power loss P_{FWD} per arm can be calculated as follows, respectively.

$$P_{IGBT} = P_{sat} + P_{on} + P_{off} \quad \text{.....(15)}$$

$$P_{FWD} = P_f + P_{rr} \quad \text{.....(16)}$$

As mentioned, since the values of $V_{CE(sat)}$, V_F, E_{on}, E_{off}, and E_{rr} change depending on T_{vj} and R_G, refer to the T_{vj} and R_G dependency graphs in the datasheet for conversion when calculating.

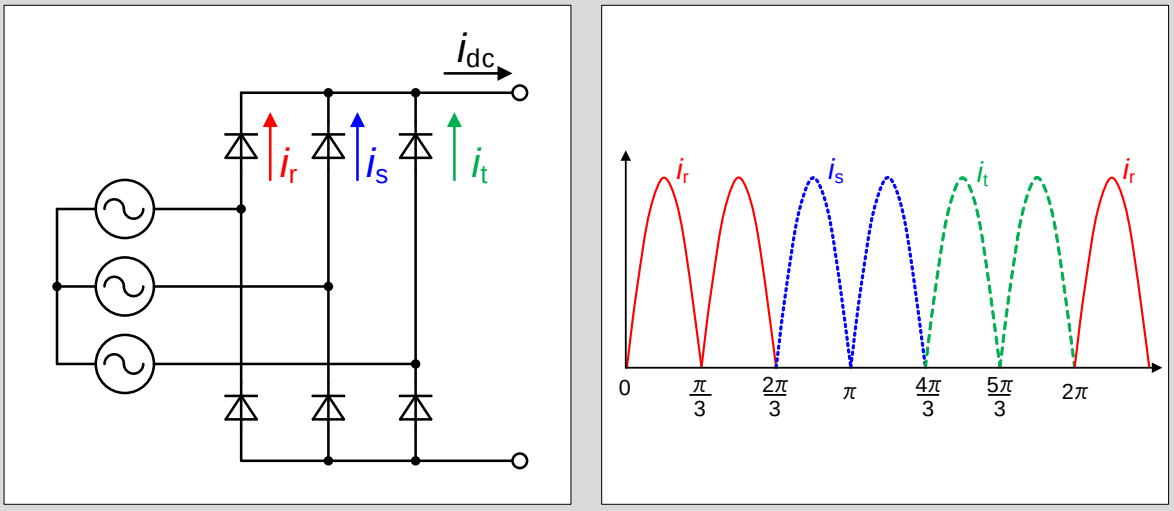
In addition, the FUJI IGBT Simulator performs calculation by approximating the characteristic curves of the data sheet more accurately, and the calculation is performed in consideration of T_{vj} dependence. Therefore, please note that the simulator result may not match the value calculated from the above formula.

* Fuji IGBT Simulator : https://www.fujielectric.com/products/semiconductor/model/igbt/simulation/

4. Power Loss Calculation Method of 3-phase Diode Rectifier Circuit

Since the diode used in the rectifier circuit does not have reverse recovery operation, there is no need to consider switching loss. Therefore, it is only necessary to calculate the conduction loss of the diode.

Fig. 6-7 shows the current waveform of a 3-phase diode rectifier circuit. Although the diode current waveform changes depending on the circuit conditions, here the calculation is performed assuming the diode current as a continuous half sine wave.



(a) 3-phase diode rectifier circuit (b) Current waveform of 3-phase diode rectifier

Fig. 6-7 3-phase diode rectifier circuit and current waveform

Assuming the RMS value of the rectified current I_{dc} shown in Fig. 6-7 as I_d, and the output characteristics of the diode is expressed by the linear approximation formula (3), the loss per diode P_{di} can be calculated by the following formula.

$$P_{di} = \frac{1}{2\pi} \cdot 2 \int_0^{\frac{\pi}{3}} \{r_F \cdot i_F(\theta) + V_{FO}\} \cdot i_F(\theta) d\theta$$

$$= \frac{1}{2\pi} \cdot 2 \int_0^{\frac{\pi}{3}} \{r_F \cdot \sqrt{2} I_d \sin(3\theta) + V_{FO}\} \cdot \{\sqrt{2} I_d \sin(3\theta)\} d\theta$$

$$= \frac{2\sqrt{2}}{3\pi} \cdot V_{FO} \cdot I_d + \frac{1}{3} r_F \cdot I_d^2$$

5. Selecting Heatsink

Most power modules such as power diodes, IGBTs, transistors are designed with insulation between the electrodes and mounting bases, thus multiple modules can be mounted on a single heat sink, resulting in easy mounting and compact wiring. However, in order to ensure safe operation, the power loss (heat) generated by each module must be dissipated efficiently, and the heat sink selection is very important. The basic concept of heat sink selection is explained in this section.

5.1 Thermal equations for steady-state

The heat conduction in semiconductors can be calculated with a thermal resistance equivalent circuit. As example, with only one IGBT module mounted on the heat sink, the equivalent circuit is shown in Fig. 6-8.

From this equivalent circuit, the T_{vj} can be calculated by the following thermal equation.

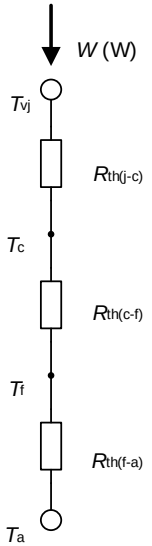
$$T_{vj} = W \cdot \{R_{th(j-c)} + R_{th(C-f)} + R_{th(f-a)}\} + T_a$$

Note that the case temperature T_c and the heat sink temperature T_f represent the temperatures at the positions directly below the chip as shown in Fig. 6-15. As shown in Fig. 6-9, temperatures at different points (B,C) are lower and depend on the heat dissipation capability of the heat sink, thus care must be taken during design.

Fig. 6-10 shows the equivalent circuit in which an IGBT module (2-Pack) and a diode bridge module are mounted on a heat sink. The thermal equations in this case are as follows.

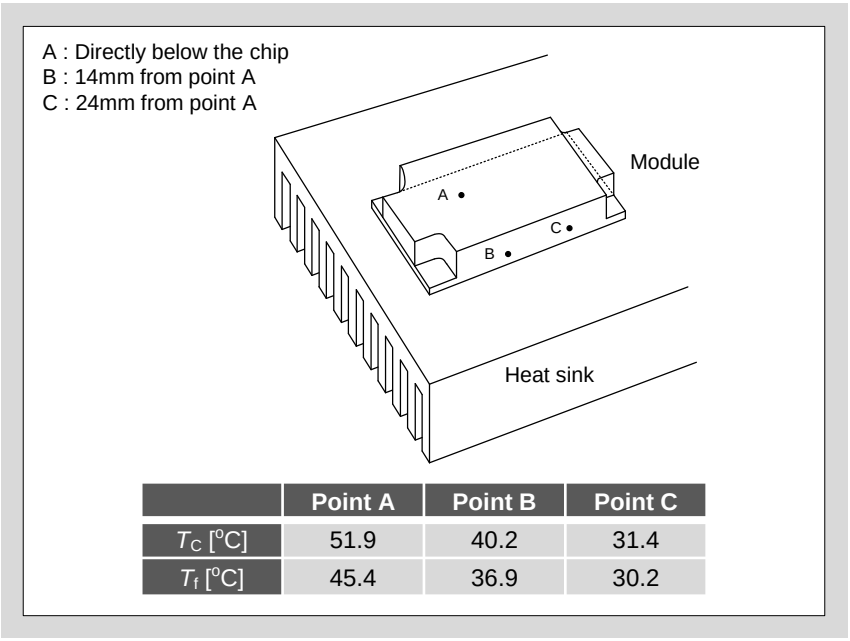
$$T_{vj(d)} = W_d \cdot [R_{th(j-c)d} + R_{th(c-f)d}] + [(W_d + 2W_T + 2W_D) \cdot R_{th(f-a)}] + T_a$$
$$T_{vj(T)} = W_T \cdot R_{th(j-c)T} + [(W_T + W_D) \cdot R_{th(c-f)T}] + [(W_d + 2W_T + 2W_D) \cdot R_{th(f-a)}] + T_a$$
$$T_{vj(D)} = W_D \cdot R_{th(j-c)D} + [(W_T + W_D) \cdot R_{th(c-f)T}] + [(W_d + 2W_T + 2W_D) \cdot R_{th(f-a)}] + T_a$$

Use the above equations to select a heat sink that can keep the T_{vj} below $T_{vj(max)}$.



W	:Power loss
T_{vj}	:Chip virtual junction temperature
T_C	:Case temperature
T_f	:Heat sink surface temperature
T_a	:Ambient temperature
$R_{th(j-c)}$	:Thermal resistance between junction and case
$R_{th(c-f)}$	:Thermal resistance between case and heatsink
$R_{th(f-a)}$	:Thermal resistance between heatsink and ambient

Fig. 6-8 Thermal resistance equivalent circuit



	Point A	Point B	Point C
T_C [°C]	51.9	40.2	31.4
T_f [°C]	45.4	36.9	30.2

Fig. 6-9 Example of case and heatsink temperature measurement

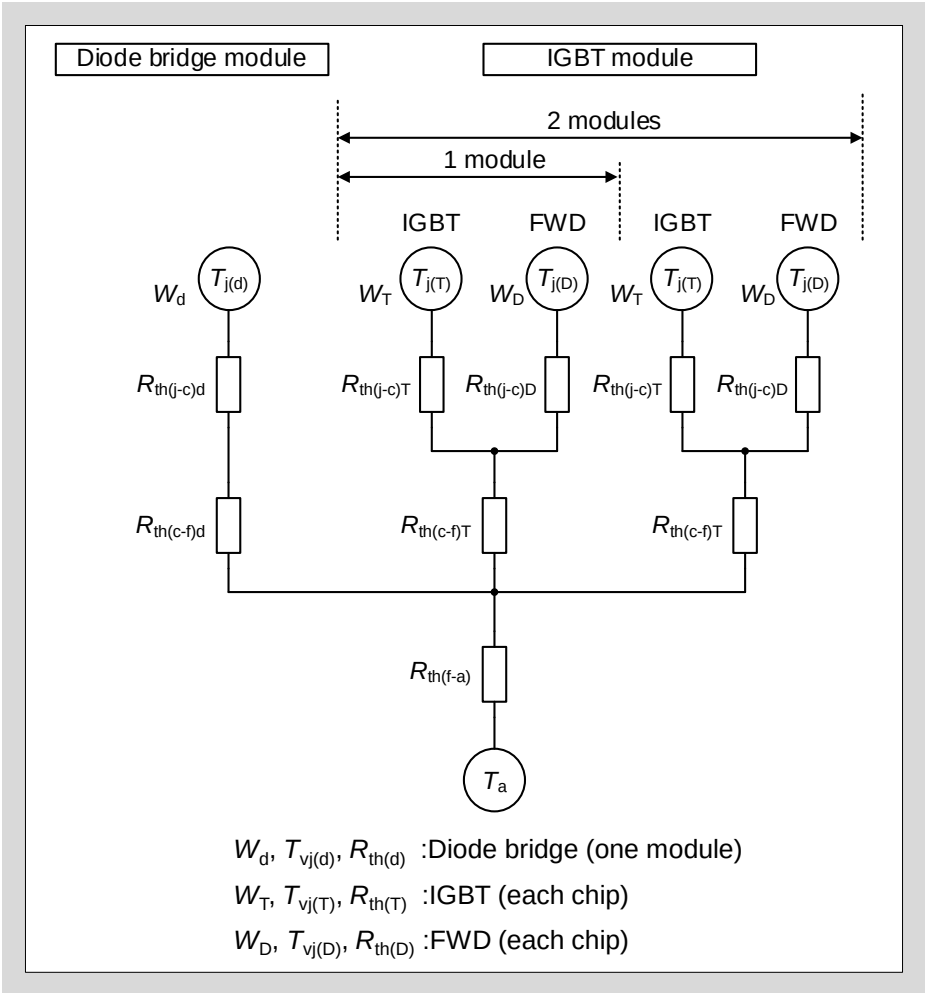


Fig. 6-10 Thermal resistance equivalent circuit

5.2 Thermal equations for transient state

In general, it is sufficient to consider the steady-state T_{vj} from the average power loss. However, in reality, repetitive switching operation generates power loss in pulse and cause temperature ripples as shown in Fig. 6-12. In this case, if the power loss is considered as a continuous rectangular wave with constant period and constant peak value, the peak value of the temperature ripples T_{vjp} can be approximated with the following formula using the transient thermal resistance curve described in the datasheet (Fig. 6-11).

Select a heat sink by confirming that T_{vjp} does not exceed $T_{vj\ (max.)}$.

$$T_{jp} - T_C = P \cdot \left[R(\infty) \cdot \frac{t1}{t2} + \left(1 - \frac{t1}{t2}\right) \cdot R(t1+t2) - R(t2) + R(t1) \right]$$

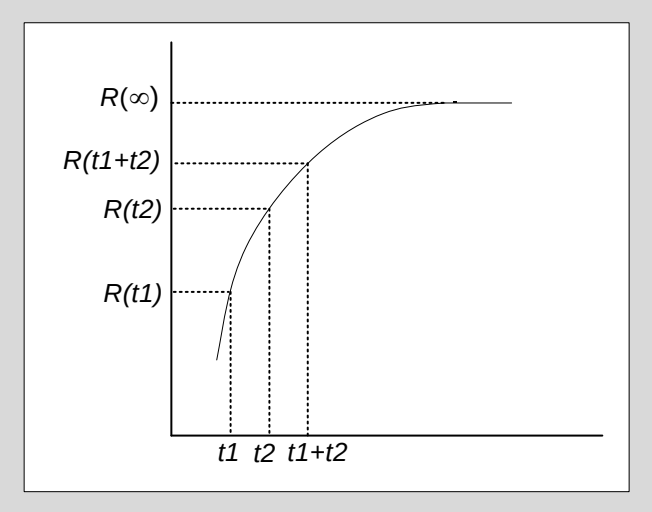


Fig. 6-11 Transient thermal resistance curve

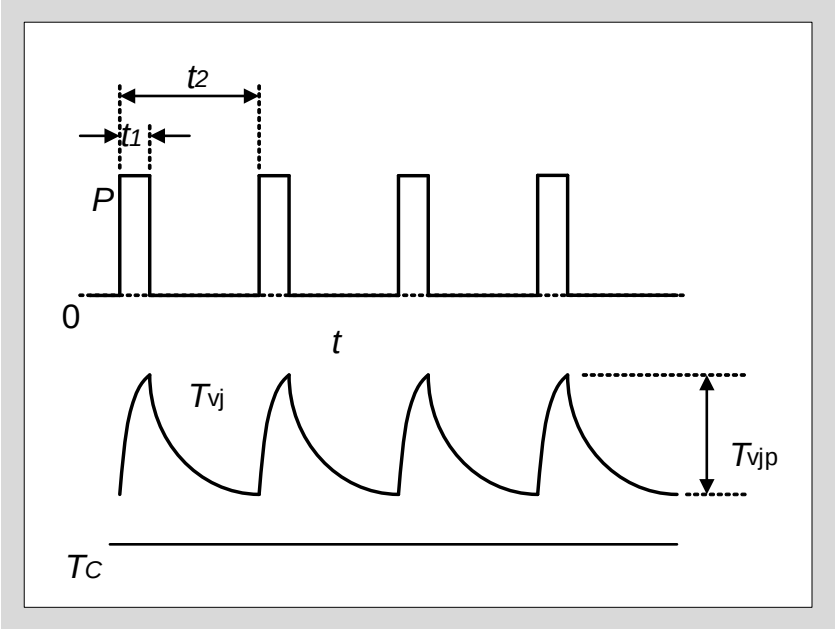


Fig. 6-12 Thermal ripples

6. Mounting Precautions

6.1 Mounting to heat sink

Since the thermal resistance varies according to the IGBT's mounting position, pay attention to the following points.

- When mounting a single IGBT module, position it in the center of the heat sink in order to minimize thermal resistance.
- When mounting several IGBT modules, determine each module position according to the power loss generated by each module. Allow more room for modules that generate more power loss.

6.2 Surface conditions of heat sink

The mounting surface roughness of the heat sink should be 10μm or less, and the surface flatness should be within +50μm (-50μm) per 100mm, taking the straight line connecting the center points of the two screw mounting holes as reference. If the roughness and flatness do not satisfy the conditions, it may cause an increase in contact thermal resistance $R_{th(c\text{-}f)}$, or insulation failure due to cracking of insulating substrate when stress is applied during mounting.

The flatness and surface roughness requirements for heat sink differ for each product. Please refer to the mounting instructions of each product for details.

6.3 Thermal grease application

To reduce contact thermal resistance, apply thermal grease between the heat sink and the mounting surface of the IGBT module.

There are several methods of applying thermal grease such as using a roller or a stencil mask.

Thermal grease improves heat dissipation from IGBT modules to heat sink, but it also has thermal capacity. Therefore, if the applied thermal grease is too thick, it will hinder heat dissipation, causing the chip temperature to rise. On the other hand, if the applied thermal grease is too thin, there is possibility that the contact thermal resistance will increase due to air gap between thermal grease and heat sink. Therefore, thermal grease must be applied with suitable thickness, else the heat dissipation to the heat sink will be poor. In the worst case, the chip temperature may exceed $T_{vj(max)}$, leading to destruction.

From these reasons, thermal grease application using a stencil mask is recommended to apply thermal grease with a uniform thickness. Fig. 6-13 shows the schematic diagram of thermal grease application using a stencil mask. The aim is to apply a specified weight of thermal grease to the module base plate using a stencil mask. After that, fix the IGBT module to the heat sink by tightening the screws with the recommended torque for respective products. In this way, the thermal grease can be applied uniformly. Fuji Electric can provide the recommended stencil mask design upon request.

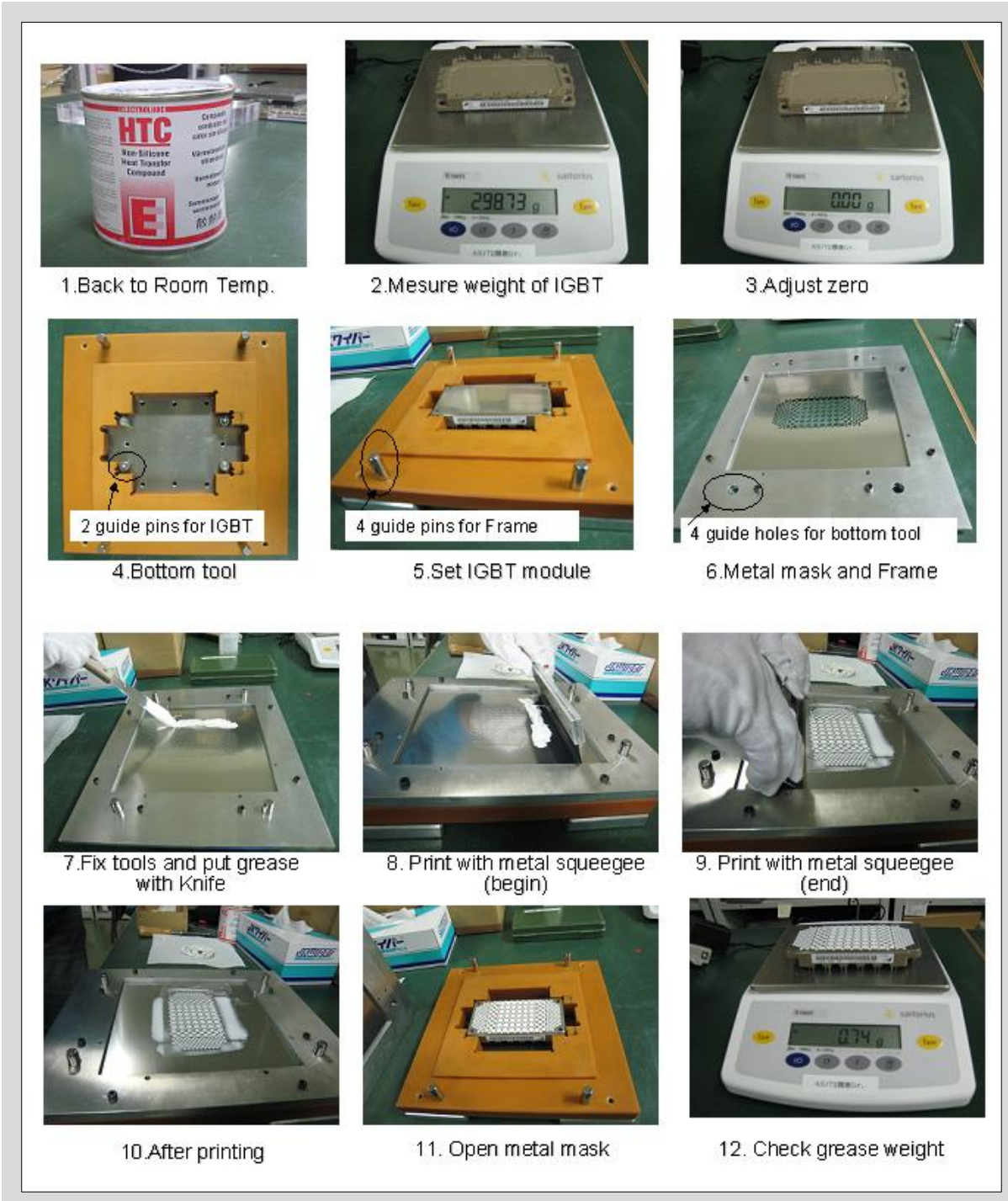


Fig. 6-13 Schematic diagram of example of thermal grease application

If the thermal grease is applied uniformly, the required weight can be calculated as follows.

$$\text{Thermal grease hickness (μm)} = \frac{\text{Weight of thermal grease (g)} \times 10^4}{\text{Base area of module (cm}^2\text{)} \times \text{Density of thermal grease (g/cm}^3\text{)}}$$

Calculate the weight for the required thermal grease thickness from the above formula and apply to the IGBT module. The recommended thermal grease thickness is about 100μm after spreading. However, the optimal thickness of the thermal grease differs depending on the thermal grease characteristics and the application method. Please check them before using.

Example of recommended thermal greases are shown in Table 6-1.

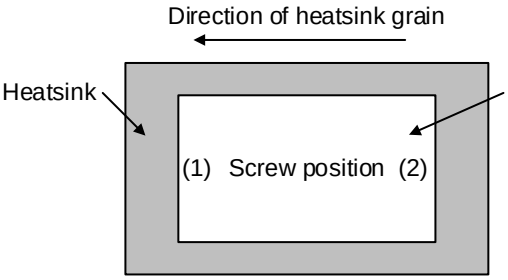
Table 6-1 Example of thermal grease

Product name	Manufacturer
TG221	Nihon Data Material Co., Ltd.
HTC	Electrolube
G747	Shin-Etsu Chemical Co., Ltd.
SC102	DuPont Toray Specialty Materials Co., Ltd.
YG6260	Momentive Performance Materials Japan LLC
P12	Wacker Asahikasei Silicone Co., Ltd.

6.4 Mounting procedure

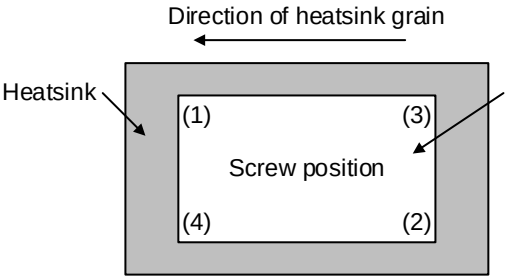
Fig. 6-14 shows examples of screw tightening when mounting an IGBT module to heat sink. Each screw must be tightened with the specified torque. Refer to the module datasheets for the specified torque.

Insufficient tightening torque may cause the contact thermal resistance to increase or the screws to become loose during operation. On the other hand, excessive tightening torque may damage the IGBT's case. The screw tightening method differs for each product. Please refer to the mounting instructions of each product for details.



	Torque	Sequence
Temporary tightening	1/3 of specified torque	(1)→(2)
Final tightening	Specified torque	(2)→(1)

(1) Two points mounting type module



	Torque	Sequence
Temporary tightening	1/3 of specified torque	(1)→(2)→(3)→(4)
Final tightening	Specified torque	(4)→(3)→(2)→(1)

(2) Four points mounting type module

Fig. 6-14 Mounting procedure

6.5 IGBT module mounting direction

When mounting the IGBT module on a heat sink made by an extrusion mold, it is recommended to mount the IGBT module parallel to the heat sink extrusion direction as shown in Fig. 6-14. This is to reduce the effect of heat sink deformation.

6.6 Temperature verification

After selecting a heat sink and determining the mounting positions, measure the temperature of each part to confirm that the T_{vj} of each module is within the module rating or design value. Fig. 6-15 shows an example of how to measure T_C. There is also a measurement method using thermocouple. Please contact us for details.

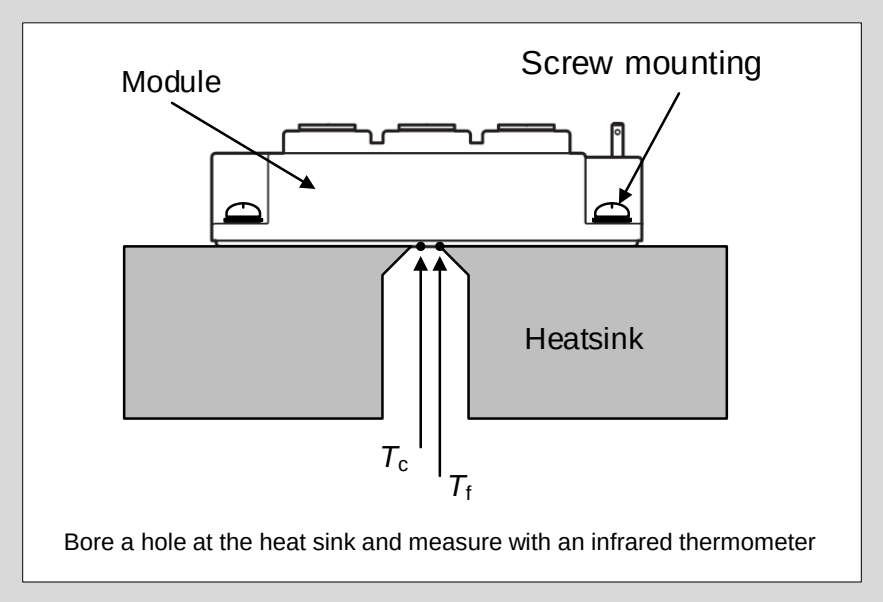


Fig. 6-15 T_C measurement method

Chapter 7 Gate Drive Circuit Design

This chapter describes about the gate drive circuit design.

1. IGBT Gate Drive Conditions and Main Characteristics

Table 7-1 shows the general relationship between the gate drive conditions and the main characteristics of the IGBT. Since the main characteristics of the IGBT change depending on V_{GE} and R_G, it is necessary to set them according to the design goal of the equipment.

Table 7-1 IGBT drive conditions and main characteristics

Main characteristics	$+V_{GE}$ increase	$-V_{GE}$ increase	$R_{G(ON)}$ increase	$R_{G(OFF)}$ increase
$V_{CE(sat)}$	↓	–	–	–
t_{on} E_{on}	↓	–	↑	–
t_{off} E_{off}	–	↓	–	↑
Turn-on FWD surge voltage	↑	–	↓	–
Turn-off IGBT surge voltage	–	↑	–	↓*1
dv/dt malfunction	↑	↓	↓	↓
Saturation current	↑	–	–	–
Short circuit withstand capability	↓	–	–	–
Radiation noise	↑	–	↓	↓

*1: Gate voltage dependence of surge voltage is different for each series

1.1 Gate forward bias voltage $+V_{GE}$ (On state)

The recommended value for $+V_{GE}$ is +15V. Notes when designing $+V_{GE}$ are shown as follows.

(1) Set $+V_{GE}$ so that it remains below the maximum G-E rated voltage of ±20V.
(2) It is recommended that supply voltage fluctuations are kept within ±10%.
(3) The $V_{CE(sat)}$ is inversely proportional to $+V_{GE}$, so the higher the $+V_{GE}$ the smaller the $V_{CE(sat)}$.
(4) The higher the $+V_{GE}$, the shorter the turn-on switching time (smaller turn-on loss).
(5) The higher the $+V_{GE}$, the larger the opposing arm FWD reverse recovery surge voltage.
(6) Even while the IGBT is in the off-state, there may be malfunction due to dv/dt during FWD reverse recovery, causing pulsed short circuit current to flow and resulting in excessive heat generation. In the worst case, the module might be destroyed. This phenomenon is called a dv/dt shoot-through and is more likely to occur when $+V_{GE}$ is higher.
(7) The higher the $+V_{GE}$, the higher the saturation current.
(8) The higher the $+V_{GE}$, the smaller the short circuit withstand capability.

1.2 Gate reverse bias voltage -V_{GE} (Off state)

The recommended value for $-V_{GE}$ is –5 to -15V. Notes when designing $-V_{GE}$ are shown as follows.

(1) Set $-V_{GE}$ so that it remains below the maximum G-E rated voltage of ±20V.
(2) It is recommended that supply voltage fluctuations are kept within ±10%.
(3) The IGBT turn-off characteristics depend on $-V_{GE}$, especially the characteristics of the part where the collector current I_C begins to turn off strongly depend on $-V_{GE}$. Therefore, the higher the $-V_{GE}$, the shorter the turn-off switching time (smaller turn-off loss).
(4) If $-V_{GE}$ is too small, d*v*/d*t* shoot-through may occur. It is recommended to set $-V_{GE}$ to at least –5V. It is especially important when the gate wiring is long.

1.3 Gate resistance R_G

The R_G listed in the product datasheets is the value that minimizes the switching losses within the absolute maximum ratings under Fuji's measurement environment. Thus, R_G must be changed appropriately according to the circuit and operating conditions. Notes when designing R_G are shown as follows.

(1) The switching characteristics of both turn-on and turn-off are dependent on the value of R_G. The larger the R_G, the longer the switching time and the greater the switching loss. On the other hand, although generally the surge voltage during turn-off switching decreases as R_G increases, surge voltage may increase as R_G increases depending on the device structure. Refer to technical documents for details. Technical documents are available for each IGBT series and voltage rating. .
(2) The larger the R_G, d*v*/d*t* shoot-through is less likely to occur.
(3) Various switching characteristics vary greatly due to stray inductance in the circuit. In particular, the surge voltage during IGBT turn-off and FWD reverse recovery are greatly affected by stray inductance. Therefore, minimize the stray inductance when designing R_G.

Select the most suitable gate drive conditions while paying attention to the above points.

1.4 Countermeasures of d*v*/d*t* induced false turn-on

Fig. 7-1 shows the principle of d*v*/d*t* induced false turn-on. In this figure, it is assumed that IGBT1 transition from off state to on state, and V_{GE} of IGBT2 is reverse biased. In this condition, when IGBT1 turns on, reverse recovery of FWD2 happens. At the same time, the voltage across IGBT2 (FWD2) rises, generating d*v*/d*t* according to the turn-on of IGBT1. Because IGBT1 and IGBT2 have feedback capacitance C_{res}, current $I=C_{res}$ x d*v*/d*t* flows through C_{res}. V_{GE} of IGBT2 rises as this current flows through R_G. When V_{GE} exceeds the sum of the reverse biased voltage and gate threshold voltage $V_{GE(th)}$ of IGBT2, IGBT2 is turned on, resulting in short circuit of IGBT1 and IGBT2.

Based on this principle, countermeasures are shown in Fig. 7-2. There are three methods, which are (a) adding C_{GE} to suppress the transient rise of V_{GE}, (b) increase $-V_{GE}$ to lower the transient peak value of V_{GE}, and (c) increase R_G to lower d*v*/d*t*. The effectiveness of these countermeasures vary depending on the gate drive circuit, thus be sure to evaluate them thoroughly. Note that these countermeasures also affect switching loss, so be sure to consider this as well.

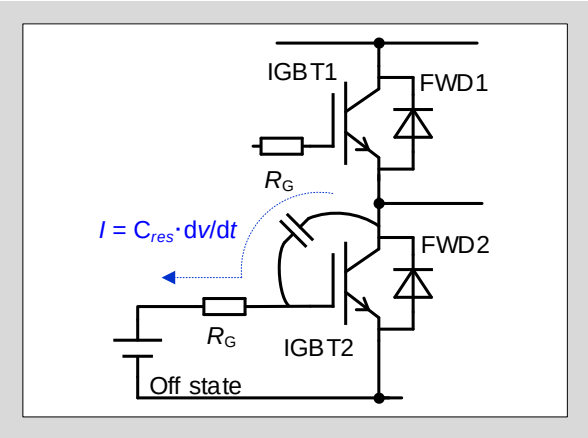


Fig. 7-1 Principle of d*v*/d*t* induced false turn-on

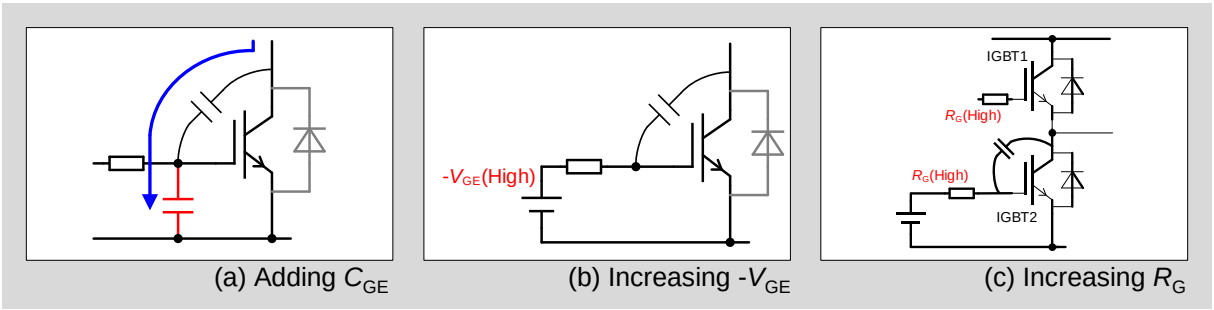


Fig. 7-2 Countermeasures against d*v*/d*t* induced false turn-on

The aim of adding C_{GE} is to reduce the current flowing through R_G by bypassing to C_{GE}. However, by adding C_{GE}, it is necessary to charge this C_{GE} when driving the gate, which reduces the switching speed and increase the switching loss. This can be adjusted by lowering the R_G value. In other words, by selecting an appropriate combination of C_{GE} and R_G, it is possible to avoid d*v*/d*t* induced false turn-on without increasing switching loss. As a guideline, the recommended C_{GE} value is about twice the C_{ies} value shown in the datasheet, and the recommended R_G value is about half the value before adding C_{GE}. Connect C_{GE} as close as possible to the G-E terminals. Confirm the selection of C_{GE} and R_G by actual evaluation.

2. Drive Current

Since IGBT has a MOS gate structure, drive current is needed to charge and discharge this gate during switching. Fig. 7-3 shows the gate charge (dynamic input) characteristics. The gate charge characteristics show the amount of charge required to drive the IGBT and can be used to calculate the average drive current and drive power. Fig. 7-4 shows the gate drive circuit schematic, as well as the gate voltage V_{GE} and drive current I_G waveforms. The principle of the gate drive circuit is to switch alternately between the forward bias and reverse bias power supply using switch S_1 and S_2. During switching, the drive current is used to charge and discharge the gate. The area (shaded) under the drive current waveform in Fig. 7-4 is equal to the gate charge shown in Fig. 7-3.

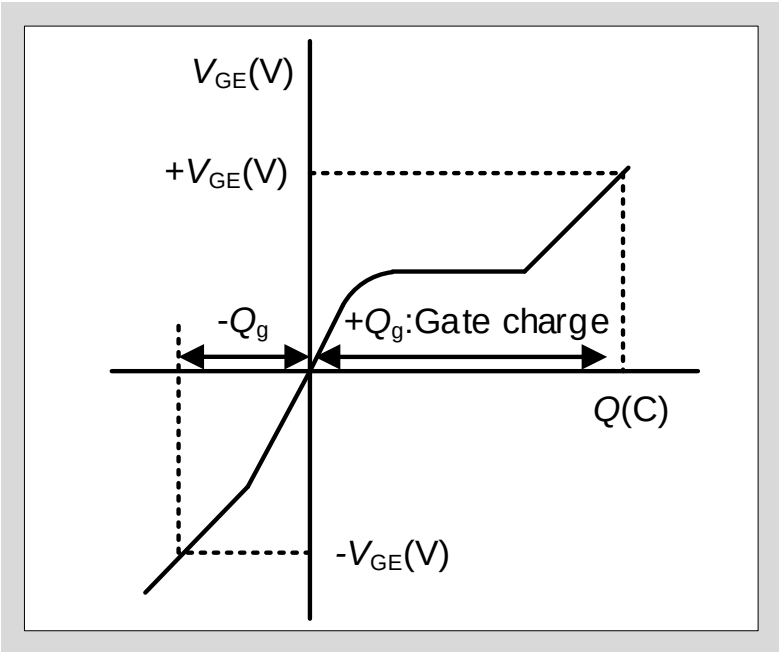


Fig. 7-3 Gate charge (Dynamic input) characteristics

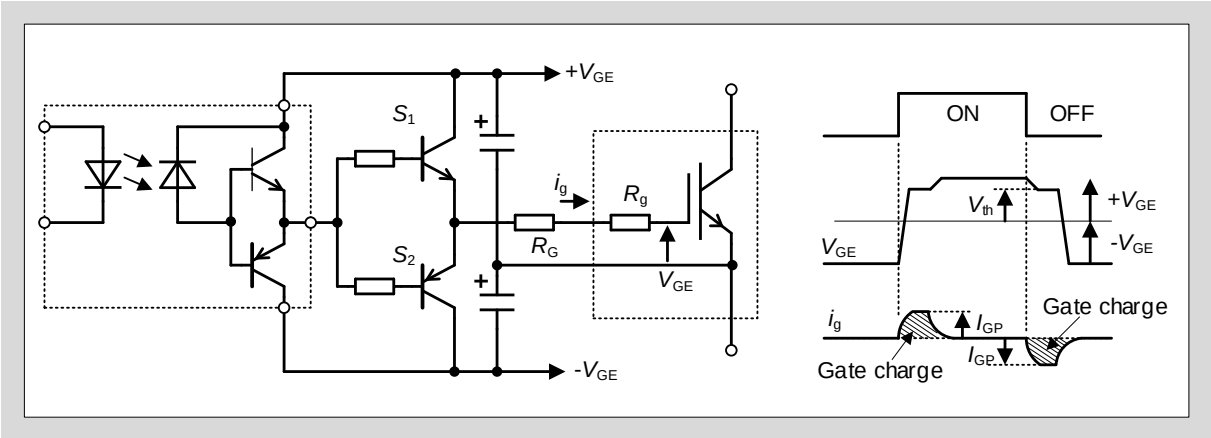


Fig. 7-4 Gate drive circuit schematic and waveforms

The drive current peak value I_{GP} can be approximately calculated as follows.

$$I_{GP} = \frac{+V_{GE} + |-V_{GE}|}{R_G + r_g}$$

$+V_{GE}$:Forward bias supply voltage
$-V_{GE}$:Reverse bias supply voltage
R_G :Gate resistance
r_g :Module internal gate resistance

Internal gate resistance r_g differs for each product. Thus, refer to the datasheet of each product.

On the other hand, the average value of the drive current I_G can be calculated by the following formula using the gate charge characteristics (Fig.7-3).

$$+I_G = -I_G = f_C \cdot \left(|+Q_g| + |-Q_g|\right)$$

f_c :Switching frequency
$+Q_g$:Gate charge from 0V to $+V_{GE}$
$-Q_G$:Gate charge from $-V_{GE}$ to 0V

Furthermore, if all the power loss of the gate drive circuit is consumed by R_G, the drive power P_d required to drive the IGBT is shown by the following formula.

$$P_{d(on)} = f_C \cdot \left[\frac{1}{2}\left(|+Q_g| + |-Q_g|\right) \cdot \left(|+V_{GE}| + |-V_{GE}|\right)\right]$$

$$P_{d(off)} = P_{d(on)}$$

$$P_d = P_{d(off)} + P_{d(on)}$$

$$= f_C \cdot \left(|+Q_g| + |-Q_g|\right) \cdot \left(|+V_{GE}| + |-V_{GE}|\right)$$

Therefore, it is necessary to select R_G with proper power rating according to P_d.

Be sure to design the gate drive circuit so that the above-mentioned drive current and drive power can be properly supplied.

3. Setting Dead time

In inverter circuits, etc., it is necessary to set an on-off timing delay (dead time) in order to prevent short circuits between the upper and lower arms. As shown in Fig. 7-5, both the upper and lower arms are in the off state during the dead time.

Basically, the dead time needs to be set longer than the IGBT switching time ($t_{off\ max}$.). For example, if R_G is increased, switching time also becomes longer, so the dead time must be increased as well. Also, it is necessary to consider other drive conditions and temperature characteristics. If the dead time is too short, short circuit between the upper and lower arms may occur, and the heat generated by the short circuit current may destroy the module. A dead time of 3μsec or more is recommended for IGBT modules. Check if the dead time is sufficient by doing actual evaluation.

One method of determining whether the dead time setting is sufficient is to check the current in the DC power line at no load condition.

In the case of a 3-phase inverter, set the inverter outputs (U, V, W) to open, apply normal input signals, and measure the DC power line current as shown in Fig. 7-6. Even if the dead time is sufficient, a very small pulse current (d*v*/d*t* current through the device output capacitance: about 5% of the rated current) will be observed. However, if the dead time is insufficient, a large short circuit current will be observed. In this case, increase the dead time until the short circuit current disappears. It is recommended to perform this test at high temperature as the turn-off time is longer. Short circuit current also increases if the gate reverse bias voltage $-V_{GE}$ is insufficient (refer to Chapter 4, section 3.3). Increase $-V_{GE}$ if increasing the dead time does not reduce the short circuit current. $-V_{GE}$ of 5V and above is recommended.

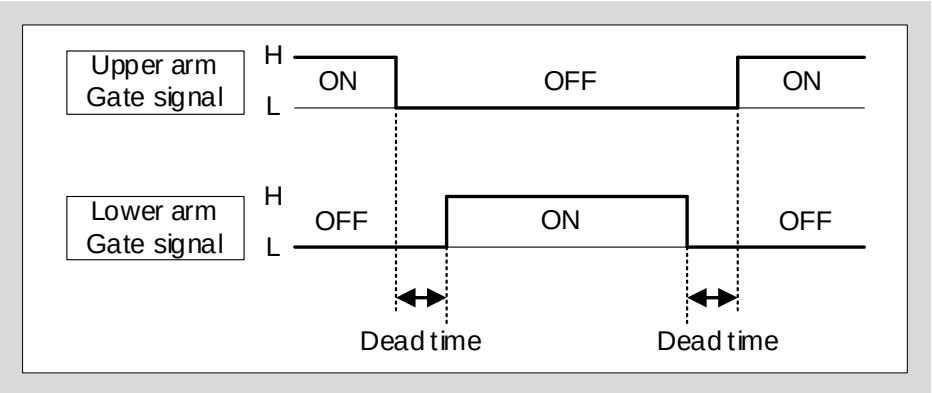


Fig. 7-5 Dead time timing chart

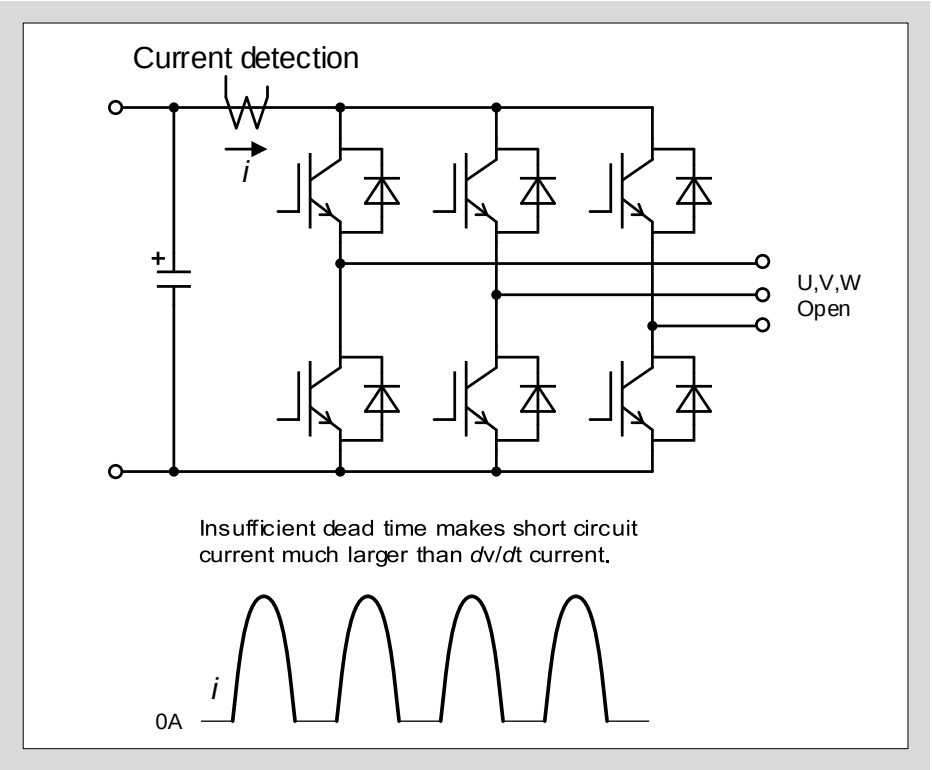


Fig. 7-6 Method for detecting short circuit current due to insufficient dead time

4. Example of Gate Drive Circuits

In inverter circuits, etc., it is necessary to electrically isolate the main circuit and the control circuit. Fig. 7-7 shows an example of a gate drive circuit using high speed optocoupler. By using optocoupler, the input signal and the module are electrically isolated from each other. Also, since optocouplers do not limit the output pulse width, they are suitable for applications where the signal pulse width varies over a wide range, such as PWM control, and is the most widely used.

In addition, turn-on and turn-off gate resistors can be used separately.

Furthermore, there is also a signal isolation method using a pulse transformer. This method can simplify the circuit because both the signal as well as the gate drive power can be supplied simultaneously from the signal side. However, this method have limitations such as a maximum duty ratio of 50%, and reverse bias cannot be set.

Recently, gate drive units (GDUs) that use pulse transformer are available in the market. Refer to the website of each GDU manufacturer for details.

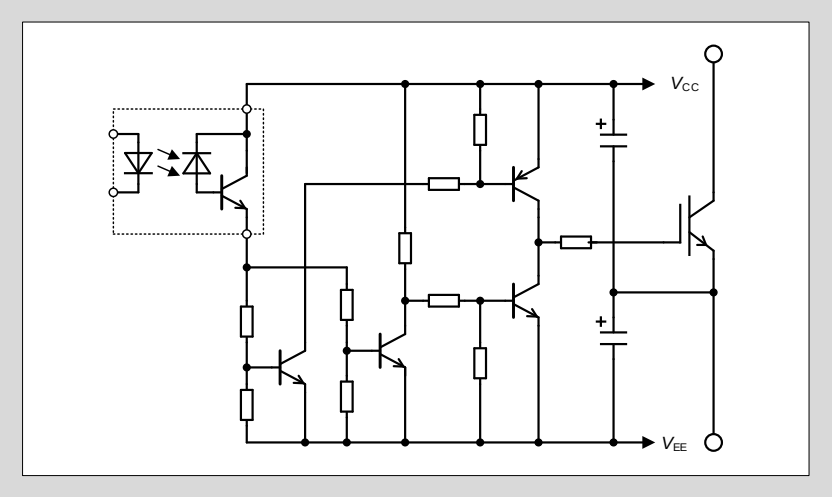


Fig. 7-7 Example of gate drive circuit using high speed optocoupler

5. Precautions for Gate Drive Circuit Design

5.1 Optocoupler noise ruggedness

As IGBTs are high speed switching devices, it is necessary to select optocoupler for gate drive circuit that has high noise ruggedness (e.g. HCPL4504). Also, to prevent malfunctions, make sure that the wiring from the optocoupler primary side and secondary side do not cross. Furthermore, in order to make full use of the IGBT high speed switching capability, using optocoupler with a short signal transmission delay is recommended.

5.2 Wiring between gate drive circuit and IGBT

If the wiring between the gate drive circuit and the IGBT is long, the IGBT may malfunction due to gate signal oscillation or induced noise. There are the following countermeasures.

(1) Make the gate drive circuit wiring as short as possible, and use twisted pair wires for the gate and emitter wiring.
(2) Increase R_G. However, pay attention to the increase of switching time and switching loss.
(3) Separate the gate drive circuit and main circuit wiring as far as possible. If the wirings overlap, design the layout so that they cross each other (in order to avoid mutual induction).
(4) Do not bundle the gate wiring or other phases together.

*1 About R_{GE}

The IGBT may be destroyed if voltage is applied to the main circuit when the gate drive circuit is malfunctioned or not fully operating (gate in open state). In order to prevent this, it is recommended to connect a resistor R_{GE} of about 10kΩ between G-E (refer to Fig. 7-8).

When powering up, first turn on the gate drive circuit power supply. Switch on the main circuit power supply when the gate drive circuit is fully operational.

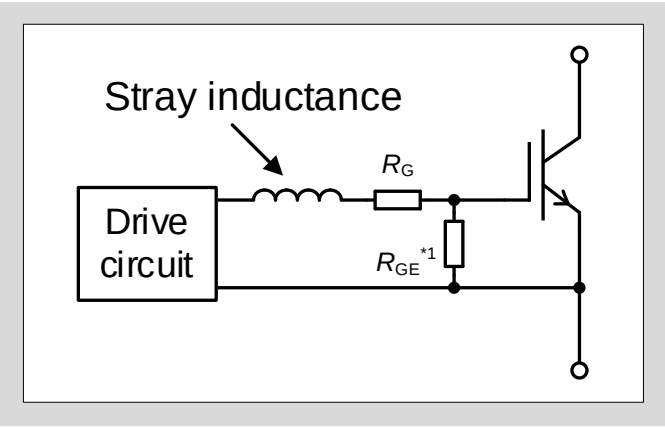


Fig. 7-8 Precautions for gate drive circuit design

5.3 Gate overvoltage protection

It is necessary that IGBT modules, like other MOS devices, are sufficiently protected against static electricity. The G-E absolute maximum rated voltage is ±20V. If there is a possibility that a voltage exceeding this may be applied to G-E, protective measures such as connecting Zenner diode between G-E are required as shown in Fig. 7-9.

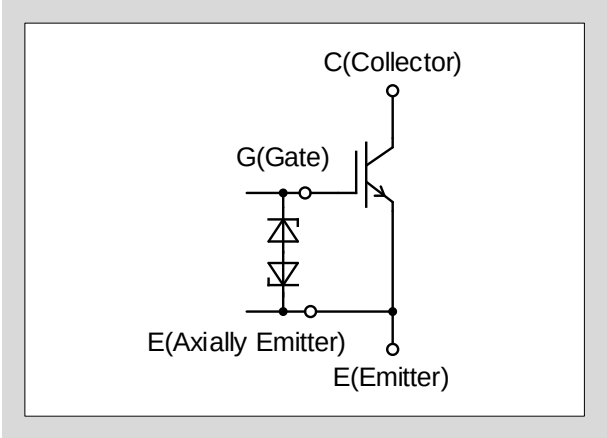


Fig. 7-9 G-E overvoltage protection circuit example

Chapter 8 Parallel Connections

The IGBT current capacity can be increased by connecting the IGBT modules in parallel. However, in this case, it is necessary to consider the current imbalance between the modules, the temperature distribution, and the increase in noise and surge voltage due to the increase in wiring length.

Note the following points when connecting IGBT modules in parallel.

1. Selection of IGBT modules
2. Main circuit design
3. Gate drive circuit design
4. Cooling design

This chapter describes the details of each point when connecting IGBT modules in parallel. Note that excluding EconoPACK™+*, 6-Pack, PIM, IPM, and Small IPM cannot be used in parallel connection.

*EconoPACK™+ is a registered trademark of Infineon Technologies.

1. Selection of IGBT modules

Points to consider when connecting IGBT modules in parallel are $V_{CE(sat)}$ variation ($\Delta V_{CE(sat)}$) and temperature dependent characteristic differences among the IGBTs on the same arm. Due to this $\Delta V_{CE(sat)}$, that is, the difference in the output characteristics of each IGBT, current imbalance occurs in the steady-state. If this current imbalance becomes excessive, the power loss of IGBT with larger current sharing increases, and there is a possibility of thermal destruction. Therefore, when selecting IGBT modules to be connected in parallel, it is necessary to choose IGBT modules with small $\Delta V_{CE(sat)}$. This concept applies to FWD as well.

1.1 Current imbalance caused by $\Delta V_{CE(sat)}$

Fig. 8-1 shows the output characteristics of two IGBTs (Q1 and Q2) with different $V_{CE(sat)}$. $\Delta V_{CE(sat)}$ is the $V_{CE(sat)}$ difference between Q1 and Q2. The output characteristics of Q_1 and Q_2 can be approximated by the following equations.

$$V_{CEQ1} = V_{01} + r_1 \cdot I_{C1}$$
$$r_1 = V_1/(I_{C1} - I_{C2})$$
$$V_{CEQ2} = V_{02} + r_2 \cdot I_{C2}$$
$$r_2 = V_2/(I_{C1} - I_{C2})$$

Based on the above, when collector current I_{Ctotal} ($=I_{C1}+I_{C2}$) flow through a circuit in which Q_1 and Q_2 are connected in parallel, the voltages across Q1 and Q2 being the same according to Kirchhoff's law, then each collector current can be calculated by the following equations, respectively.

$$I_{C1} = (V_{O2} - V_{O1} + r_2 \cdot I_{Ctotal})/(r_1 + r_2)$$
$$I_{C2} = (V_{O1} - V_{O2} + r_1 \cdot I_{Ctotal})/(r_1 + r_2)$$

If $V_{01}=V_{02}$ in the above equations, I_{C1} is r_2/r_1 times larger than I_{C2}. As shown in Fig. 8-1, $r_2>r_1$, thus the current sharing of Q1, which is the IGBT with lower $V_{CE(sat)}$ becomes larger.

The ratio of current sharing is called the current imbalance rate, and is determined by $\Delta V_{CE(sat)}$ of each IGBT. Fig. 8-2 shows an example of current imbalance rate for 2 parallel connection of V series IGBTs. It can be seen that the current imbalance rate increases as $\Delta V_{CE(sat)}$ increases. Therefore, when connecting IGBTs in parallel, it is important to combine products with small $\Delta V_{CE(sat)}$.

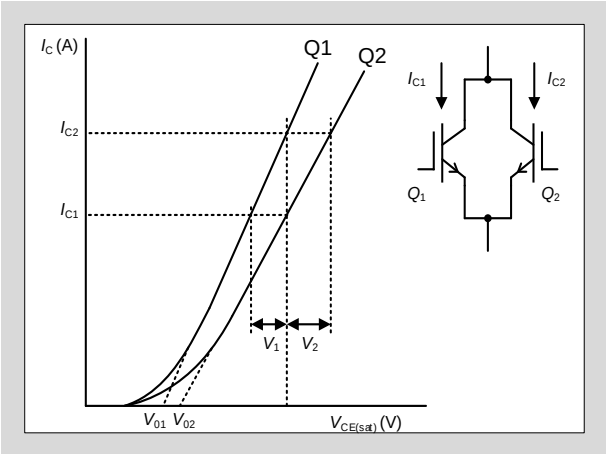


Fig. 8-1 Example of different output characteristics

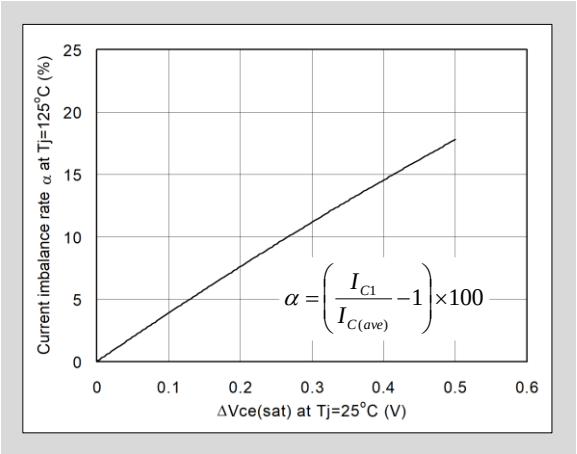


Fig. 8-2 $\Delta V_{CE(sat)}$ and current imbalance rate

1.2 $\Delta V_{CE(sat)}$ minimization

$\Delta V_{CE(sat)}$ can be minimized by using IGBT modules from the same product lot. This is because the influence of fabrication process, such as variations in raw materials, manufacturing, and inspection process can be minimized. Therefore, parallel connection with modules from the same product lot is recommended.

In addition, some products have $V_{CE(sat)}$ and V_F values displayed on the product label, and Data Matrix code that allow $V_{CE(sat)}$ and V_F to be read. Using this data, combining products with little variation is recommended. Fig. 8-3 shows the product label, and Fig. 8-4 shows an example of the Data Matrix code. For details, please refer to the specifications of each product.

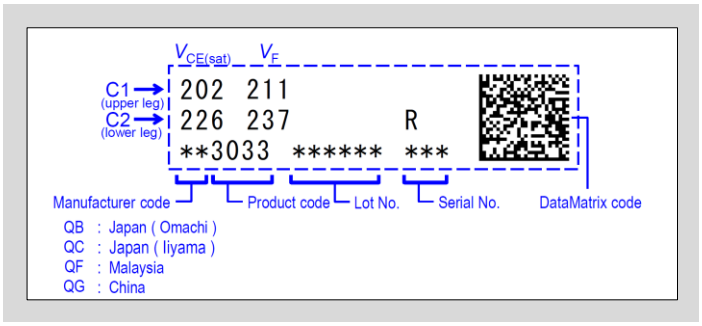


Fig. 8-3 Product label

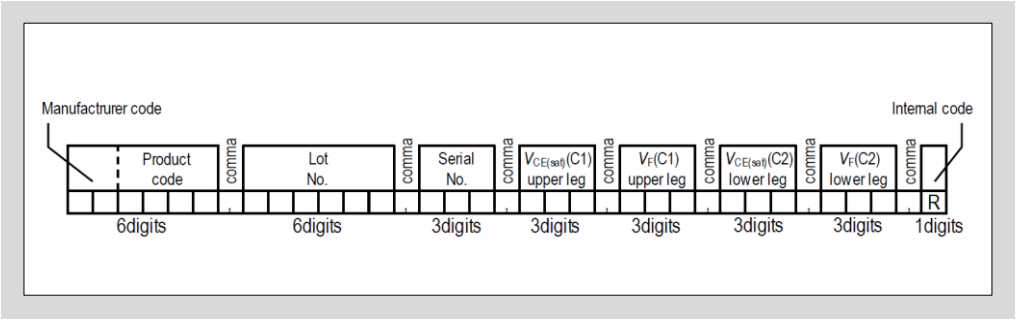


Fig. 8-4 Data Matrix code

1.3 T_{vj} dependency of output characteristics and current imbalance

T_{vj} dependency of output characteristics deeply affects current imbalance. Here, output characteristic, whose $V_{CE(sat)}$ is higher and lower with the increase of T_{vj}, is defined as the positive and negative T_{vj} dependency, respectively. Using 100A rated IGBT as an example, Fig. 8-5 shows the output characteristics with positive and negative T_{vj} dependency.

As described in section 1.1, when two IGBTs are connected in parallel, the current sharing of the IGBT with lower $V_{CE(sat)}$ increases. Therefore, steady-state power loss is larger for the IGBT with lower $V_{CE(sat)}$, and T_{vj} rises more than the other IGBT. In this case, if the T_{vj} dependency is positive, $V_{CE(sat)}$ increases as T_{vj} increases, and the current sharing decreases accordingly. In this way, in a combination of IGBTs with positive T_{vj} dependency, the current flowing through both IGBTs becomes balance due to temperature rise. On the other hand, in a combination of IGBTs with negative T_{vj} dependency, $V_{CE(sat)}$ decreases as T_{vj} rises, which increases the current imbalance. Therefore, when IGBTs and FWDs whose output characteristics are temperature dependent are connected in parallel, an increase in T_{vj} may affect the current imbalance rate.

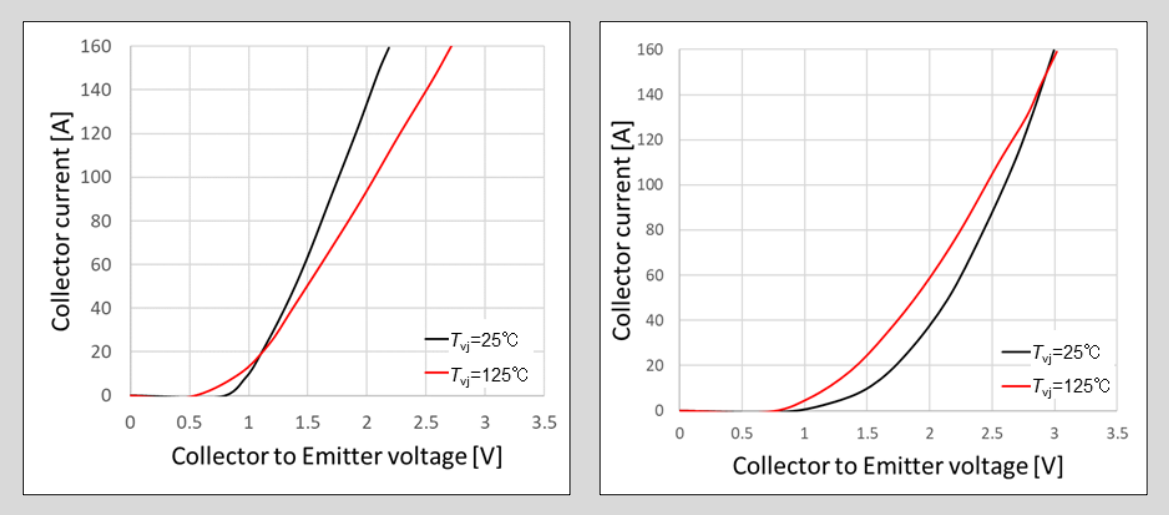


Fig. 8-5 Comparison of IGBT output characteristics
(left: positive T_{vj} dependency, right: negative T_{vj} dependency)

1.4 Derating in parallel connection with multiple of IGBTs

When IGBTs are connected in parallel, the current imbalance must be taken into consideration, and the total current (maximum current that can flow) must be derated (decrease of total current) relative to the total rated current. When n-number of IGBTs are connected in parallel, the worst condition is current concentration in the IGBT with the lowest $V_{CE(sat)}$. Therefore, the allowable maximum current Σ*I* when n-number of IGBTs are connected in parallel can be expressed by the following formula, using the current imbalance rate α when two IGBTS are connected in parallel.

$$\sum I = I_{C(max)}\left[1 + (n-1)\frac{\left(1-\frac{\alpha}{100}\right)}{\left(1+\frac{\alpha}{100}\right)}\right] \qquad \alpha = \left(\frac{I_{C1}}{I_{C(ave)}} - 1\right)\cdot 100$$

Here, the current imbalance rate α in the above formula can be obtained from the current value I_{C1} and the average current value $I_{C(ave)}=(I_{C1}+I_{C2})/2$ for two parallel IGBTs as shown in Fig. 8-1. $I_{C(max)}$ is the maximum current for a single IGBT, and Σ*I* is the maximum current of the parallel connection. However, in order to operate with the maximum current Σ*I*, each IGBT connected in parallel must satisfy the RBSOA stated in the specification, and T_{vj} rise caused by power loss must be kept bellow $T_{vj(max)}$ as well. Note that T_{vj} rise varies depending on the operating conditions such as switching frequency, gate drive condition, cooling condition, snubber condition, etc.

The total current Σ*I* in a parallel connection requires derating with respect to the simple sum of currents (n· $I_{C(max)}$). For example, if α=15%, $I_{C(max)}$=200A and n=4, then Σ*I*=643.4A. In this case, derating of 19.6% is required from the simple sum of 200x4=800A.

Fig. 8-6 shows the IGBT derating rate when α=15%. As shown in this figure, derating rate increases as the parallel number increases. Therefore, derate the total current according to the parallel number. Note that derating rate depends on the current imbalance rate.

The derating rate shown in this example is a reference value calculated from the current imbalance rate. Please determine the derating rate after verifying the imbalance rate by actual evaluation.

If it is necessary to replace the paralleled modules due to troubles and/or maintenances, it is recommended that all the paralleled modules be replaced. In this case, it is recommended to use modules from the same production lot.

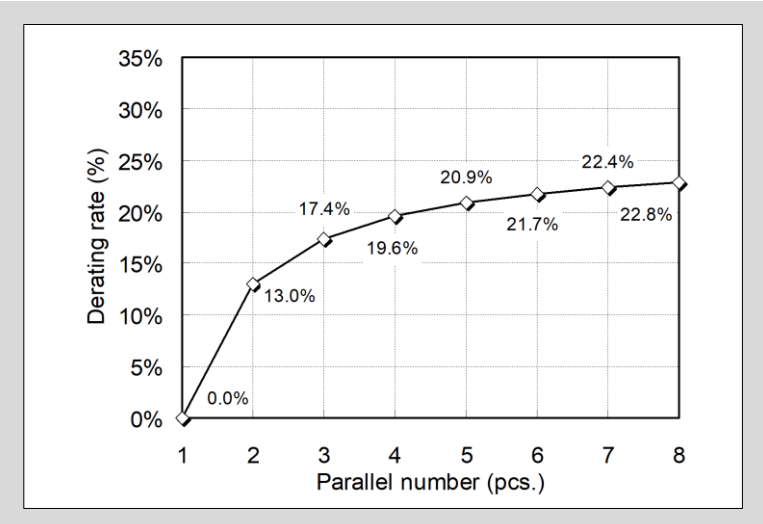


Fig. 8-6 Relationship between derating rate and parallel number

2. Main Circuit Design

Variation in the main circuit wiring between each IGBT module in a parallel connection has a large effect on the current imbalance during both steady-state operation and switching operation. Since this may lead to malfunction, it is necessary to keep the following two factors in mind and design the main circuit wiring symmetrically and as short as possible.

(1) Variation in main circuit wiring resistance
(2) Variation in main circuit wiring inductance

2.1 Variation in main circuit wiring resistance

Fig. 8-7 shows the simplified equivalent circuit of a two parallel IGBT connection showing the main circuit wiring resistance. The collector side resistance component is omitted.

If the resistance component of the main circuit wiring is large, the total collector current flowing through Q1 and Q2 will decrease compared to when the resistance component is small. The larger the resistance component, the smaller the total collector current.

In this way, the resistance component of the main circuit may cause a decrease in collector current or current imbalance. Therefore, in order to reduce this effect, the wiring on the emitter side must be as short and as symmetric as possible.

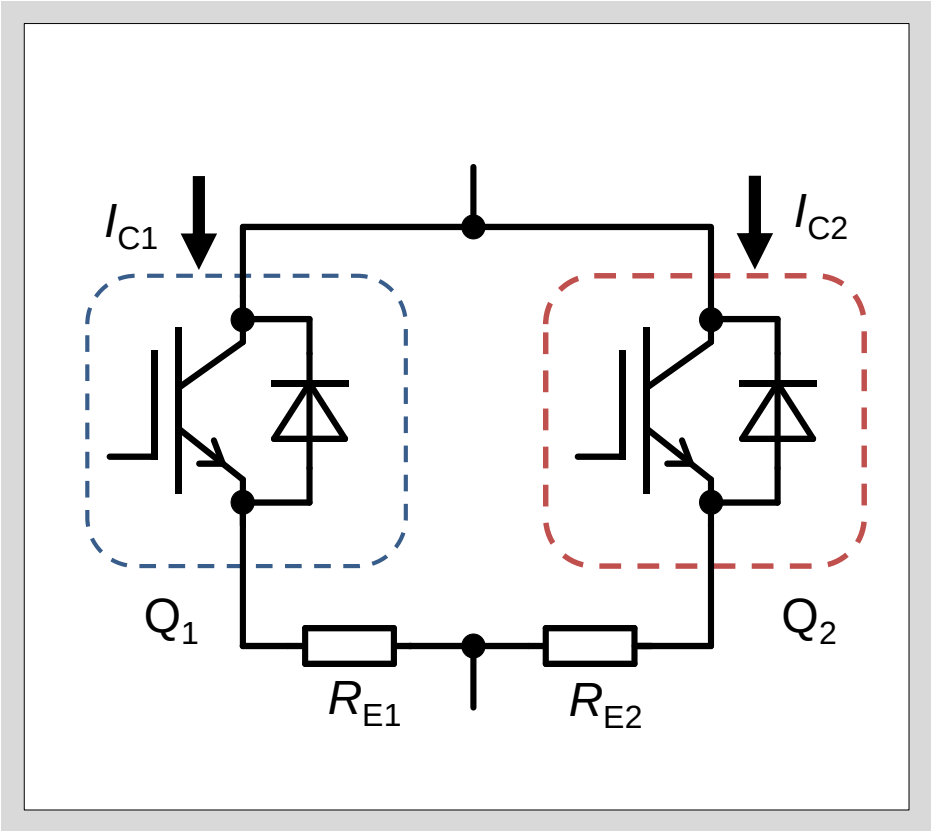


Fig. 8-7 Equivalent circuit of main circuit with wiring resistance component

2.2 Variation in main circuit wiring inductance

Fig. 8-8 shows the simplified equivalent circuit of a two parallel IGBT connection showing the main circuit wiring inductance. If the main circuit wiring inductance is uneven, current imbalance will occur between the IGBTs during switching. When collector currents I_{C1} and I_{C2} flow through IGBT Q1 and Q2, respectively, the current sharing is affected by the difference between the wiring inductances of each IGBT L_{E1} and L_{E2}. The current sharing is mostly determined by the inductance ratio. Therefore, in order to reduce the current imbalance during switching, it is necessary to design the wiring inductance as even as possible. If the wiring inductances L_{E1} and L_{E2} are different, there will be difference in the induced voltage of L_{E1} and L_{E2} caused by di/dt at turn-on. The difference in induced voltage affects the effective gate voltage of each IGBT and promotes current imbalance. For this reason, in a parallel connection, it is important to design the main circuit so that L_{E1}=L_{E2} as much as possible. Also, if the main circuit wiring inductance is large, the surge voltage at IGBT turn-off will increase. Therefore, it is necessary to design the wiring inductance as small as possible.

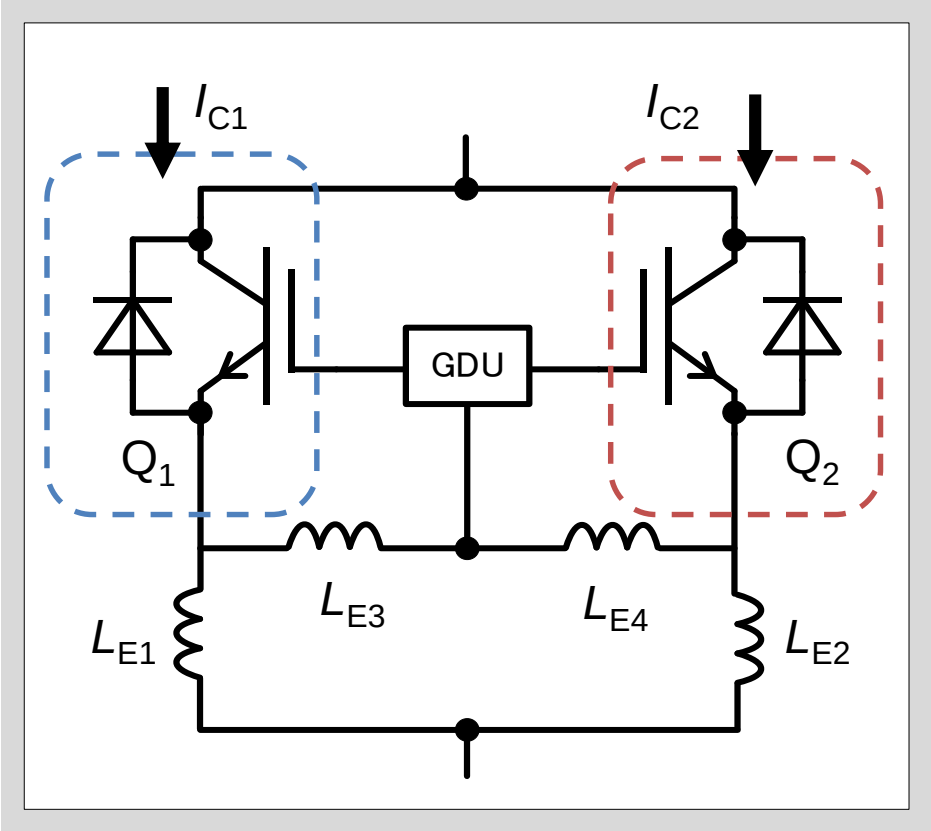


Fig. 8-8 Equivalent circuit of main circuit with wiring inductance component

2.3 Wiring example for parallel connection

As described above, care must be taken in the main circuit design of a parallel connection.

Fig. 8-9 shows an example of equivalent circuit when paralleling two 2-Pack modules. As shown in Fig. 8-9, all the wiring to the IGBTs (IGBT1 and IGBT2) are connected symmetrically.

Fig. 8-10 shows the switching waveforms of two 1700V/1000A 2-Pack modules connected in parallel with symmetrical wiring. As shown in this waveform, both the currents I_{C1} and I_{C2} flowing through each IGBT are almost equal, and the current imbalance rate is only 2%. This shows that symmetrical wiring in parallel connection can realize good current balance.

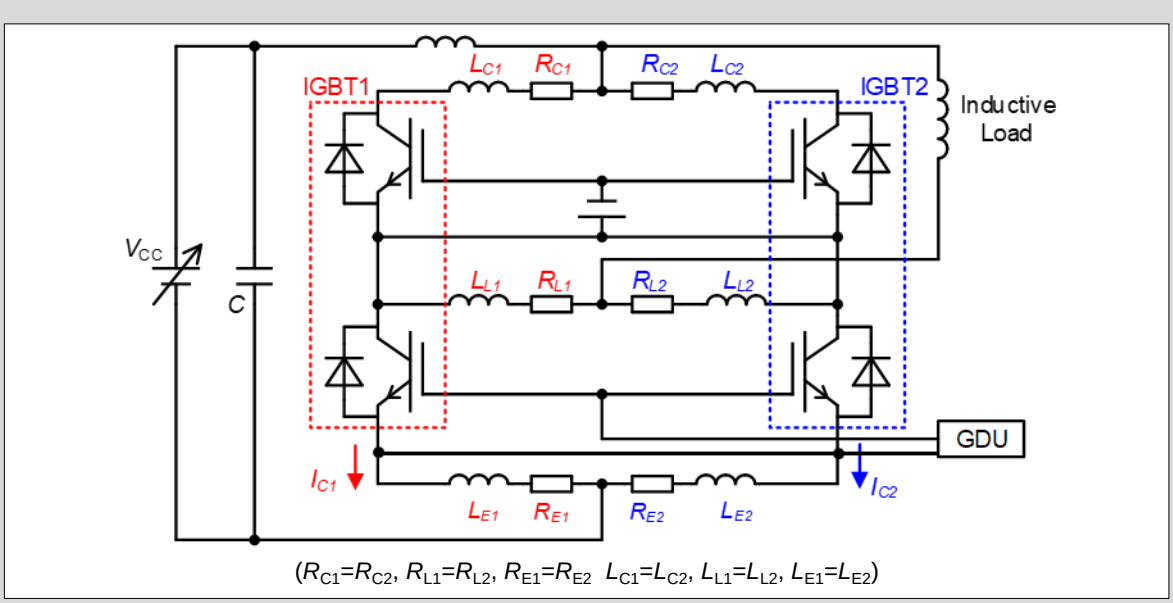


Fig. 8-9 Equivalent circuit when paralleling two 2-Pack modules

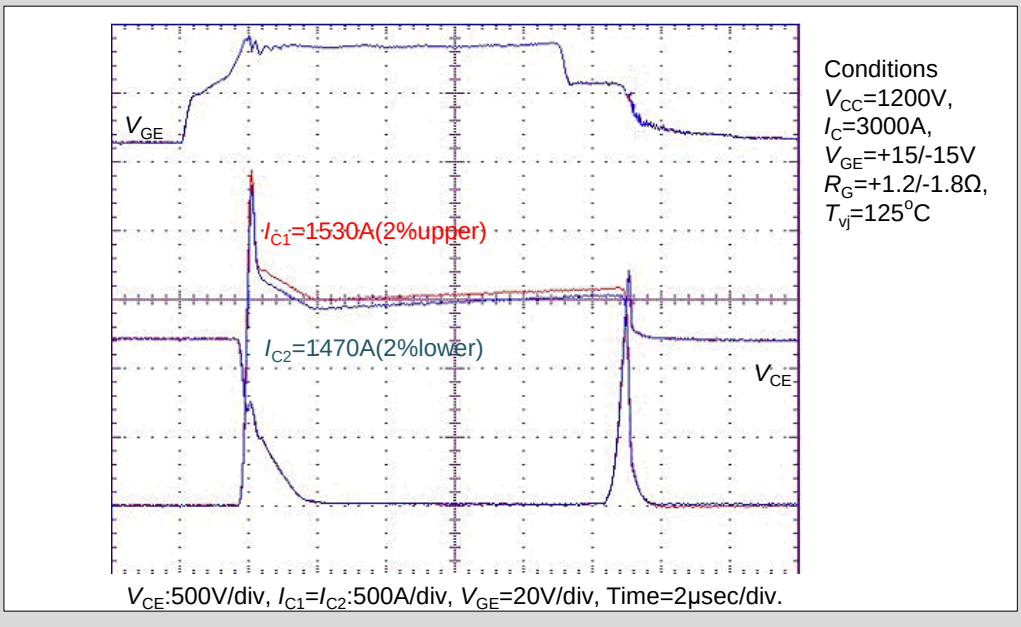


Fig. 8-10 Switching waveforms of two 1700V/1000A 2-Pack modules connected in parallel

3. Gate Drive Circuit Design

In addition to the contents of Chapter 7, there are other precautions when designing gate drive circuits for parallel connection of IGBT modules. Also, there are different precautions depending on the gate driver configuration for parallel connection. If these precautions are not taken into consideration, the gate drive circuit may cause current imbalance or malfunction, possibly destroying the IGBT modules. The main precautions when designing gate drive circuits for parallel connections are described as follows.

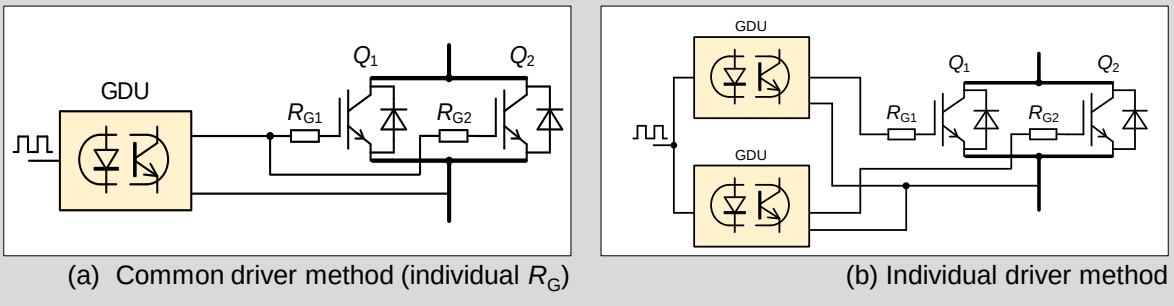
3.1 Connection of gate drive circuit to gate-emitter terminal

When driving parallel connected IGBTs, if the IGBT module has auxiliary emitter terminal, use the auxiliary emitter terminal to drive the IGBT. If there is no auxiliary emitter terminal, and the emitter wiring of the gate drive circuit is connected at a position where the wiring inductances L_{E1} and L_{E2} as shown in Fig. 8-8 are uneven, the gate voltage of each IGBT during switching will differ, resulting in unbalanced transient current sharing. Normally, IGBT modules such as 2-Pack have auxiliary emitter terminal for the gate drive circuit. Using this terminal will realize balanced L_{E1} and L_{E2}, thus transient current imbalance can be suppressed.

However, even if auxiliary emitter terminal is used to drive the IGBT, if the emitter wiring from the gate drive circuit to each IGBT module is long and uneven, current imbalance will occur. Therefore, it is important to design the gate drive circuit wiring to each IGBT with equal length, as short as possible, and symmetrical. The gate drive circuit wiring should be twisted, and kept as far away from the main circuit wiring as possible and not parallel to each other.

3.2 Precautions when designing gate drive circuits for parallel connections

There are several gate drive circuit methods for parallel connection of IGBT modules, and precautions differ depending on the gate driver configuration. As example of gate drive circuit configuration for parallel connection, Fig. 8-11(a) shows the common driver method (a configuration in which one gate driver drives all the IGBTs), and Fig. 8-11(b) shows the individual driver method (a configuration in which each IGBT is driven by individual gate drivers equal to the number of parallel IGBTs). Details of these two types of gate drive circuits and their design considerations are described in the following pages.



(a) Common driver method (individual R_G)　　(b) Individual driver method

Fig. 8-11 Gate drive circuit configuration for parallel connection

3.2.1 Common driver method

A feature of the common driver method is that the power supply and optocoupler that drive each IGBT can be shared, thus the gate drive circuit can be simplified and the number of components can be reduced. On the other hand, driving multiple IGBTs connected in parallel with a single power supply requires a large power supply capacity.

In addition, the emitters of each parallel IGBT are common within the gate drive circuit, creating a closed loop which may generate gate voltage fluctuations during switching and cause the IGBTs to malfunction. As example, a turn-on waveform with parasitic oscillation is shown in Fig. 8-12, and the mechanism of the parasitic oscillation is shown below. If the wiring inductances L_{E1} and L_{E2} as shown in Fig. 8-8 are uneven, the difference in wiring inductance and the input capacitance of the IGBT will generate a cross current, which will generate electromotive force in L_{E3} and L_{E4}, resulting in parasitic oscillation of the gate voltage.

As countermeasures, consider inserting a common mode choke in the gate circuit or a resistor R_E on the emitter side, and confirm that the problem described above does not occur.

Mechanism of parasitic oscillation during turn-on in common driver method

(a) When IGBTs Q1 and Q2 turns on, I_C increases and di/dt occurs in the main circuit. As a result, electromotive forces V_{LE1} and V_{LE2} are generated in the wiring inductances.

(b) When there is a difference in the wiring inductances, the magnitude of electromotive forces V_{LE1} and V_{LE2} will be different, generating a cross current i_N in the closed loop.

(c) Electromotive forces V_{LE3} and V_{LE4} are generated in the wiring inductances between the GDU and the emitter L_{E3} and L_{E4} by this cross current i_N, and parasitic oscillation of the gate voltage is generated by the charging and discharging currents to Q1 and Q2.

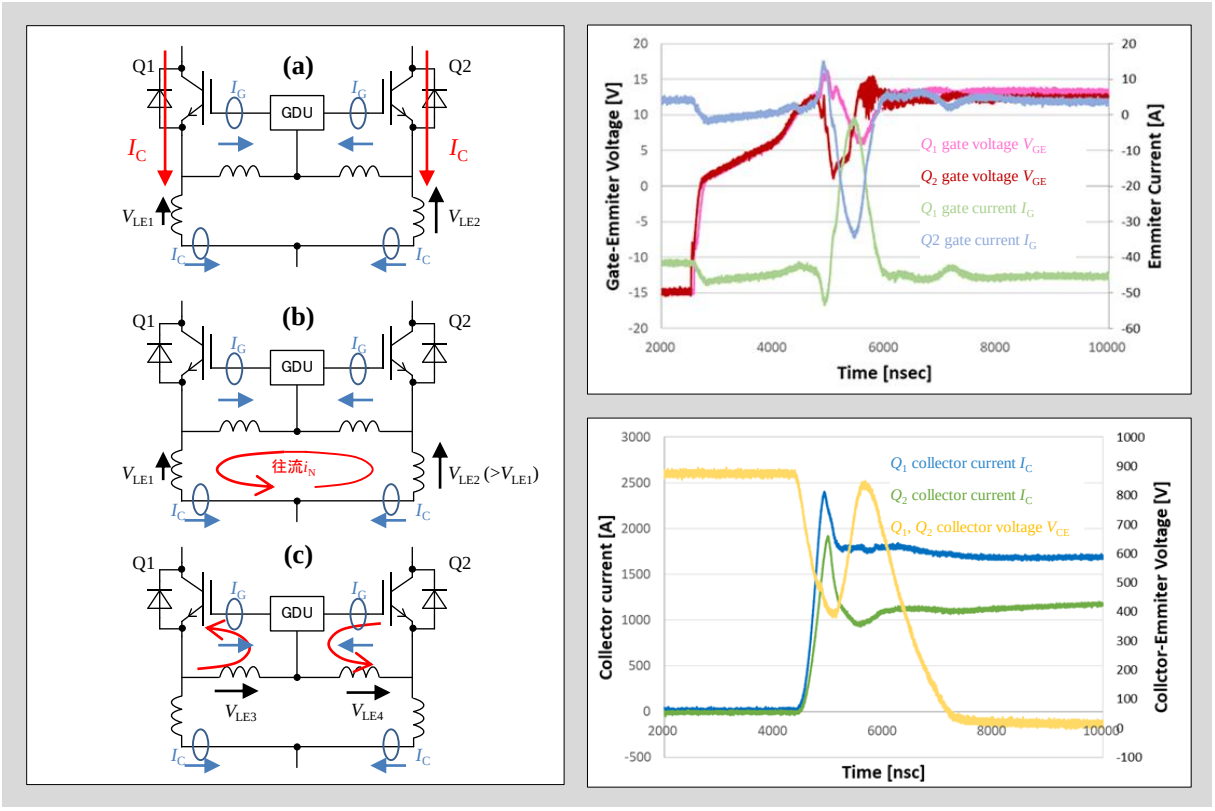


Fig. 8-12 Parasitic oscillation mechanism and turn-on waveforms

3.2.2 Individual driver method

A feature of the individual driver method is that the emitters of the parallel IGBTs are not common. In this case, a closed loop is not formed thus there will no cross current at the emitter, and risk of malfunction such as parasitic oscillation shown in Fig. 8-12 is reduced. On the other hand, arranging individual gate drive circuits for each parallel IGBT modules complicates the gate drive circuit. In addition, due to variations in the characteristics of electronic components such as optocouplers, each parallel IGBT has a difference in turn-on/turn-off timing, which may cause current imbalance or malfunction during switching. Therefore, when designing gate drive circuit for the individual driver method, it is necessary to minimize the difference in timing between turn-on and turn-off of each IGBT by considering the characteristics variation of electronic components.

3.2.3 Gate resistor configuration in common driver method

As shown in Fig. 8-13, there are three methods for configuring the gate resistor R_G in the common driver method.

In the case of the individual gate resistor method as shown in Fig. 8-13(a), the R_G connected to each IGBT can suppress the parasitic oscillation caused by the circuit inductance of the gate circuit wiring and the input capacitance of the IGBT. However, even if each IGBT is connected to the same driver IC, variations in the R_G can cause differences in the turn-on/turn-off timing of each IGBT during switching, which may cause current imbalance or malfunction.

In the case of the common gate resistor method as shown in Fig. 8-13(b), there will be no difference in the R_G value of each IGBT, so the difference in turn-on/turn-off timing of each IGBT can be minimized. However, due to LC resonance of the gate drive circuit wiring inductance and the input capacitance of the IGBT, parasitic oscillation may occur when the gate voltage rises.

If no parasitic oscillation or IGBT turn-on/turn-off timing difference is observed, it is possible to apply the common gate resistor method or the individual gate resistor method. However, when designing a new gate drive circuit, it is recommended to apply the combination gate resistor method as shown in Fig. 8-13(c), which combines the characteristics of both common gate resistor method and the individual gate resistor method.

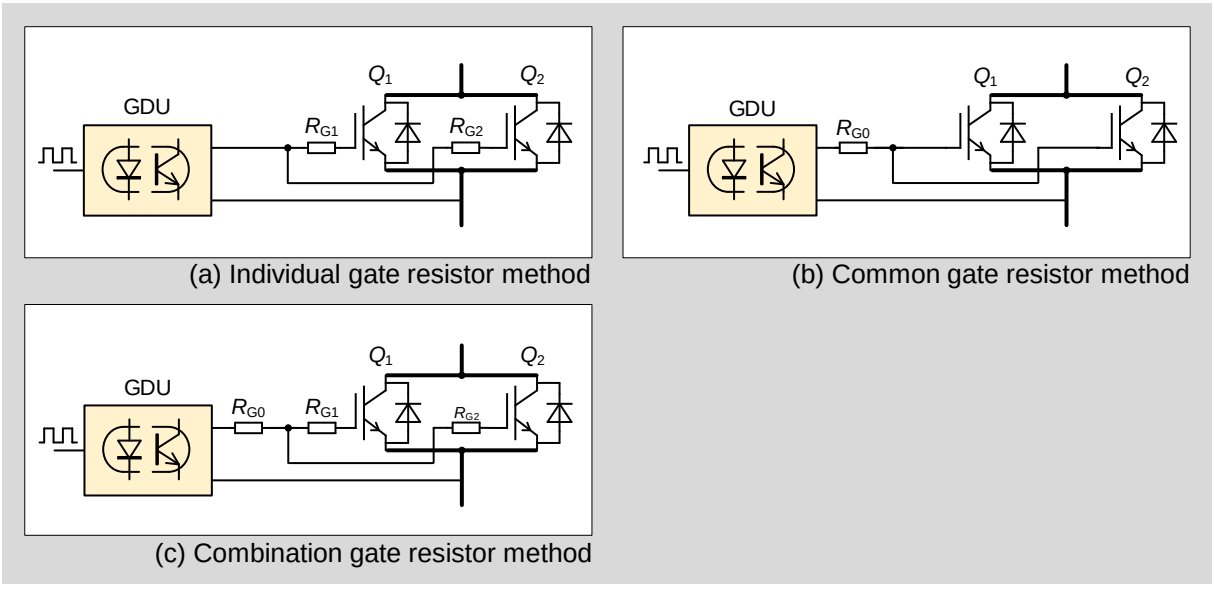


Fig. 8-13 Gate resistor configuration in common driver method

4. Cooling Design

When connecting IGBT modules in parallel, it is necessary to consider the thermal interference of each IGBT module. If the junction temperature T_{vj} increases due to thermal interference, the junction temperature absolute maximum rating $T_{vj(max)}$ may be exceeded and cause thermal destruction of the IGBT modules. Therefore, it is necessary to consider the thermal interference between each module and design the modules layout to reduce T_{vj}. The points to consider regarding cooling design in parallel connection are shown below.

(1) Layout design considering thermal interference between each module.
(2) Equalize cooling conditions for each module.
(3) Uniform thermal grease thickness applied to each module.

Especially for (1), simulation of thermal interference when adjusting the spacing between two parallel IGBT modules (2MBI1400VXB-170P-50) on the same heat sink is conducted. Fig. 8-14 shows the simulation result. In the case of equidistant layout (where each IGBT module is centered between the centerline and edge of the heatsink), the temperature rise $\Delta T_{v(j-a)}$ is lowest. Therefore, in order to minimize the thermal interference of each IGBT module, it is effective to design a layout in which the heat sink area is evenly divided by the number of IGBT modules, and each module is placed in the center of each area.

On the other hand, if the size of the heat sink is increased as the IGBT module spacing is increased, the thermal interference between each IGBT module can be further reduced. However, in this case, the wiring inductance L_S of the main circuit increases, which increases the surge voltage V_{CEP} at turn-off, and the IGBT module may be destroyed by overvoltage.

Therefore, consider the trade-off between thermal interference of each IGBT module and increase of surge voltage, and design an appropriate cooling system.

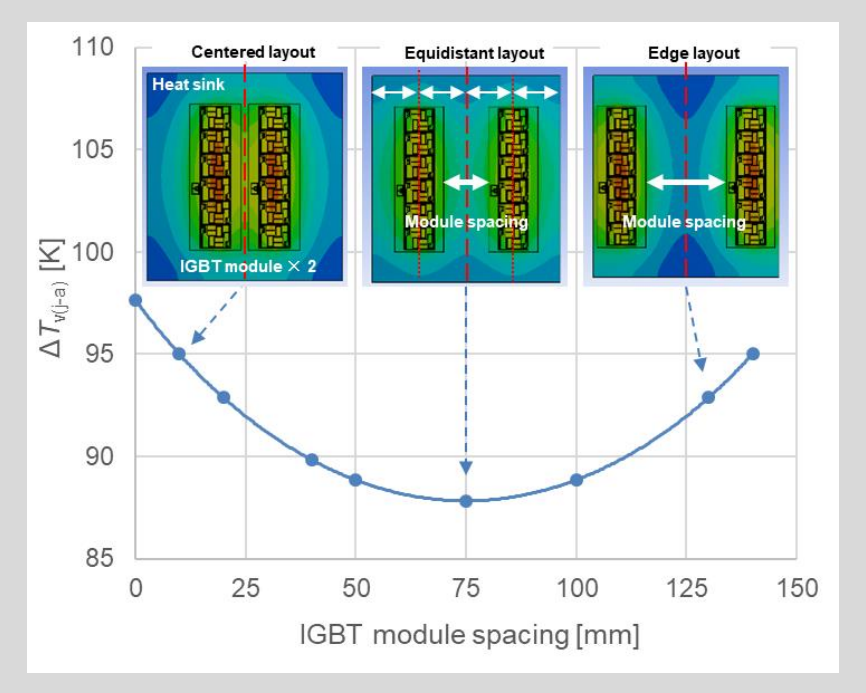


Fig. 8-14 $\Delta T_{v(j-a)}$-IGBT module spacing dependency

Chapter 9 Evaluation and Measurement

This chapter describes how to evaluate the characteristics of IGBT module, and voltage and current measurement methods.

1. Application Scope

This chapter describes the method of evaluating the characteristics of IGBT modules applied to power electronics equipment with a switching frequency of several kHz to 20kHz and equipment capacity of several hundred VA or more.

2. Evaluation and Measurement Methods

2.1 Overview of evaluation and measurement methods

During development of power electronics equipment, it is necessary to evaluate the characteristics and measure the load of the IGBT modules while they are installed in the equipment. An overview of the evaluation items and measurement methods is shown in Table 9-1.

Table 9-1 Overview of evaluation items and measurement methods

No.	Evaluation item	Measurement item	Measurement methods	Measuring instrument
1	Isolation voltage	Voltage	With the module terminals shorted, apply a voltage between the conductive part and the device frame.	Isolation voltage tester
2	Collector-Emitter voltage		With G-E shorted, apply test voltage to C-E. *If there is possibility that the test voltage may exceed the rating of the components connected to C-E, disconnect those components first.	Curve tracer
3	Collector-Emitter saturation voltage		Measure by connecting a voltage clamping circuit between C-E so that the built-in amplifier of the oscilloscope does not saturate. *Static characteristics can be measured with a curve tracer or pulse h_{FE} meter	Oscilloscope
4	Turn-off surge voltage	Voltage	Measure the C-E voltage directly at module terminals.	Oscilloscope
5	Switching time	Voltage Current	Measure the required voltage and current waveforms according to the switching time definition.	Oscilloscope Current probe
6	Current sharing (parallel connection)	Current	Measure the current flowing through each module.	Oscilloscope Current probe
7	Switching loss	Voltage Current	The product of the current and voltage is integrated over a specified period. (1) Calculate from voltage & current waveforms (2) Use a measuring instrument with math function	Oscilloscope
8	Operation locus		Plot the voltage & current during switching in current-voltage graph.	Oscilloscope
9	Case temperature	Temperature	Measure on the copper base under the chip *The measurement location is point A as shown in Fig. 6-9 in Chapter 6.	Thermocouple
10	Junction temperature		Create a calibration curve for the junction temperature and device characteristics with temperature dependence characteristics (for example, saturation voltage), and measure the characteristics of the device during operation to estimate the junction temperature. *Can be measured directly using an IR camera.	IR camera

2.2 Voltage measurement

Note that voltage measurement during IGBT operation is susceptible to noise caused by high-amplitude, high-speed switching operation.

(1) Measuring instrument and calibration

Both the waveform and the target voltage value are important. Normally, an oscilloscope is used as the measuring instrument, and a voltage probe is used for voltage measurement. The time constant of the voltage divider RC of the probe/oscilloscope vary depending on the oscilloscope/probe combination. Therefore, before using the probe, carry out probe compensation to achieve uniform attenuation across all frequency range by connecting it to the calibration terminal of the oscilloscope.

Set the appropriate sensitivity (generally, 3 to 4 division amplitude on the display screen) and set the input coupling to DC. Exercise caution in selecting the probe, because the adjustment capacitance of the probe and the input capacitance of the oscilloscope must match to enable adjustment. The selection of oscilloscopes and probes are shown in sections 2.5 and 2.6.

(2) Saturation voltage measurement

Generally, while the circuit voltage using IGBT is as high as several hundred volts, the IGBT saturation voltage is as low as several volts. Because the size of the screen of the oscilloscope is limited, increasing the voltage sensitivity in an effort to measure the saturation voltage accurately will result in the display of a waveform that is different from the actual waveform due to effect such as saturation of the oscilloscope built-in amplifier. Therefore, the IGBT saturation voltage during switching operation cannot be measured by directly measuring the C-E voltage of the IGBT with an oscilloscope.

The method to measure the saturation voltage is by adding a voltage clamping circuit as shown in Fig. 9-1.

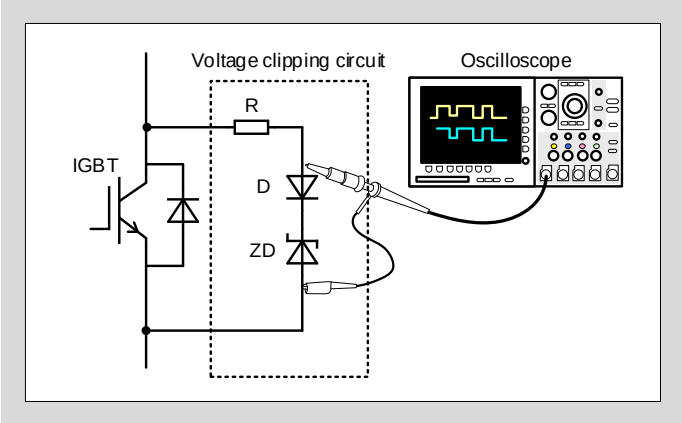


Fig. 9-1 Measurement method of saturation voltage

In Fig. 9-1, the Zener diode (ZD) limits the high voltage when the IGBT is turned off. Generally, a Zener diode with Zener voltage of 10V or less is used. R is a current-limiting resistor. Because most of the circuit voltage is applied to this resistor when the IGBT is turned off, the resistor must have a relatively large capacity. The diode (D) prevents the charges built in the junction capacitance of the Zener diode from discharging, and also prevents a RC filter from being formed by the junction capacitance and the current-limiting resistance.

(3) Surge voltage measurement (Collector-emitter voltage measurement)

While IGBTs offer the benefit of fast switching, the current change rate (-d*i*/d*t*) at turn-off is large, inducing a high voltage in the main circuit wiring inductance (L_S) of the equipment. This voltage is superimposed over the DC circuit voltage and cause a spike voltage to be applied to the module. This voltage is called surge voltage, and it is necessary to confirm that the voltage is within a predetermined voltage margin with respect to the maximum rating of the module.

The surge voltage can be measured at the terminals of the module with an oscilloscope and directly reading the value on the oscilloscope screen. Note the following precautions during measurement.

a. Use a probe and an oscilloscope having a sufficient frequency bandwidth.
b. Adjust the oscilloscope sensitivity and calibrate the probe.
c. Connect the measurement probe directly to the module terminals.

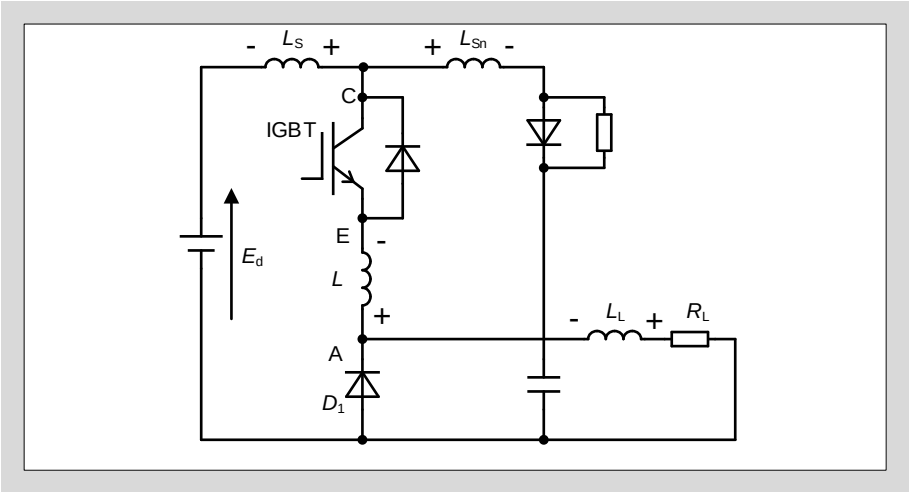


Fig. 9-2 Example of surge voltage measurement circuit

During IGBT turn-off, voltages of the polarity shown in Fig. 9-2 are induced in the circuit inductances of each part of the circuit. Note that in the case where V_{CA} is measured instead of V_{CE}, then a voltage lower than V_{CE} by $-L \cdot di/dt$ will be erroneously measured. Therefore, when measuring the surge voltage of the IGBT, it is necessary to measure it in a state where the influence of the wiring inductance L is minimized, such as by connecting the voltage probe directly to the module terminal.

d. Keep the probe measurement leads as short as possible.
e. Keep probe leads away from high d*i*/d*t* areas so that noise interferences are minimized.

When the voltage probe is connected to the switching circuit, the reference potential of the oscilloscope would equal the switching circuit. If there is a large ground potential fluctuation in the switching circuit, common-mode current would flow through the power line of the oscilloscope, which may cause the internal circuit to malfunction. Noise interferences can be verified by the following methods.

a. Consider whether the measured waveform can be logically explained.
b. Comparing with waveforms measured on a battery-powered oscilloscope that is less susceptible to noise interferences.

(4) Gate voltage measurement (Gate-emitter voltage measurement)

The V_{GE} can be directly measured with an oscilloscope similar to the surge voltage. However, since the IGBT gate is a capacitive load and the voltage probe also has capacitive impedance, do not attach or detach the voltage probe during measurement. The same precautions as for the surge voltage measurement are required.

2.3 Current measurement

Current probes are used for current measurement. However, in practical device, the main circuit is compact in order to reduce wiring inductances L_S and simplify the structure. Thus, the wiring needs to be extended to measure the device current. A current transformer can be used to minimize the wiring extension. In addition, the use of current transformers is also necessary due to the limited measuring capacity of the current probe.

Current probe can measure current while maintaining insulation from the conductive part, but in addition to being an electromagnetic induction-based detector, the signal level is low that it is susceptible to induction caused noise interferences. Care should be taken against noise interferences.

(1) Current detectors

Table 9-2 shows the examples of current detectors.

Table 9-2 Current detectors

No.	Product name	Model	Brand	Remarks
1	DC current probe (Dedicated amplifier and power supply required)	Model A6302	Tektronix	Maximum circuit voltage: 500V ~20A at DC~50 MHz Peak pulse current: ~50A
2		Model A6303		Maximum circuit voltage: 700V ~100A at DC~5MHz Peak pulse current: ~500 A
3	AC current probe	Model P6021		Maximum circuit voltage: 600V ~15Ap-p at 120Hz~60MHz Peak pulse current: 250A
4		Model P6022		Maximum circuit voltage: 600V ~6Ap-p at 935Hz~120MHz Peak pulse current: 100A
5	ACCT	Varied	Pearson	~35MHz
6	Rogowski coil current probe	CWT	PEM	Current range: 300mA~300kA Bandwidth: 0.1Hz~16MHz

(2) Current probe sensitivity check

Before making any measurements, it is necessary to check the probe sensitivity.

Current probe can be calibrated using the oscilloscope calibrator output or using an oscillator as shown in Fig. 9-3. The measurement method in Fig. 9-3 uses a known resistance *R* (non-inductive) to measure the voltage *e* across *R* to obtain the current *i*. Compare the current *i* and the waveform of the current probe to calibrate. If the current *i* is too small, sensitivity can be increased by increasing the number of primary winding of the current probe.

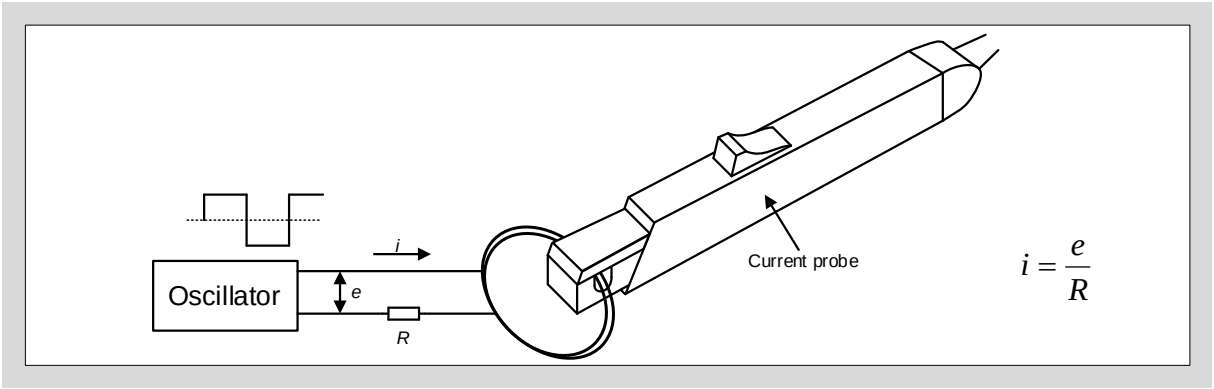


Fig. 9-3 Current probe calibration method

(3) Current measurement method

Using a two parallel connection as example, Fig. 9-4 shows where current transformers (CT) are inserted to measure the current. When measuring the current on the positive side of T_{11}, measure the secondary side current of CT_1 with a current probe. For T_{12}, measure the secondary side current. The total current on the positive side (sum of T_{11} current and T_{12} current) can be measured with the same current probe by aligning the directions of the secondary side currents of CT_1 and CT_2 and measuring them at once. Refer to sections 2.6 and 2.7 for the application of current probe and current transformer.

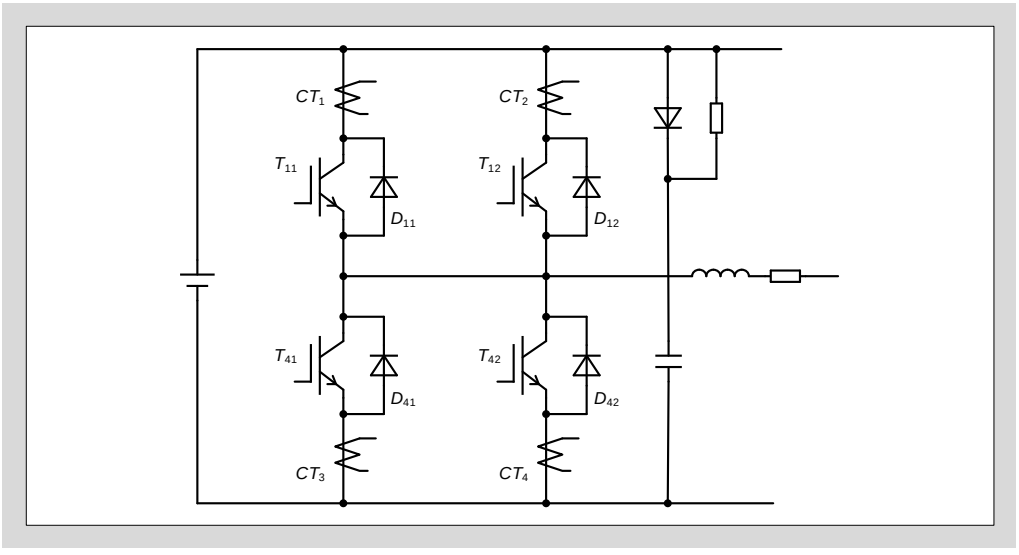


Fig. 9-4 CT insert position and current measurement method

2.4 Switching loss measurement

Switching loss is the loss generated during the period from the start of switching to the end of switching operation and reaching a steady-state. For example, the turn-on loss is the loss that is generated from V_{GE} is above 0V until V_{CE} reaches the saturation voltage.

The switching loss is generally expressed in terms of energy generated per instance of switching.

Fig. 9-5 shows example of switching waveform and switching loss. To measure switching loss, the current and voltage waveforms must be measured correctly. Note that when current and voltage are measured simultaneously, the common-mode current flowing from the voltage probe may cause the current waveform to be distorted. The presence or absence of this common-mode effect can be determined by comparing the current waveforms before and after the voltage probe is connected. If the current waveform is distorted, inserting a common-mode choke into the voltage probe cable and the oscilloscope power cable (by winding the cable around a core with excellent high frequency characteristics) as shown in Fig. 9-6 will reduce the waveform distortion.

In addition, the settings of reference 0V and 0A is important. Note that when using an AC current probe, the position of 0A varies depending on the current value and the conduction ratio.

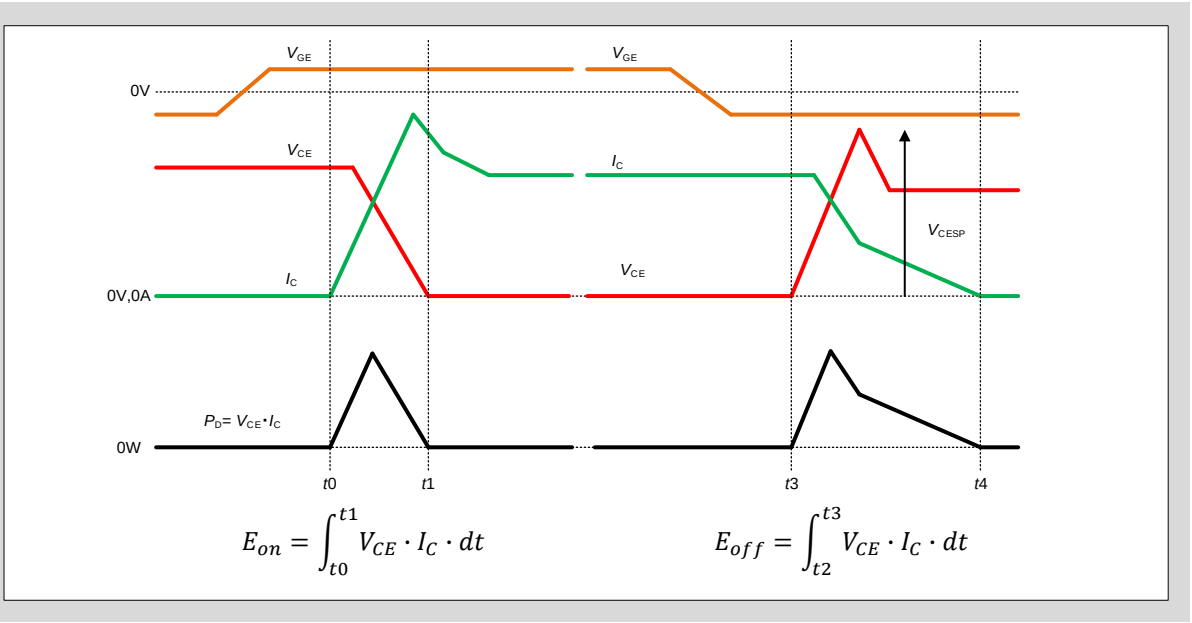


Fig. 9-5 Switching loss

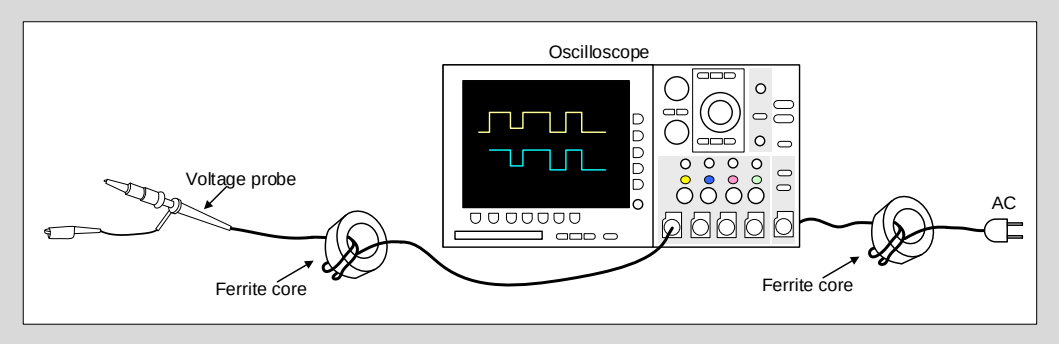


Fig. 9-6 Inserting common mode choke

2.5 Selecting oscilloscopes

Because oscilloscopes vary in terms of functionality and performance, it is important to select the right oscilloscope to suit the measurement items required and the rate of change in the signal to be measured. This section outlines the signal source rise time and the frequency bandwidth requirements for the oscilloscopes.

(1) Relationship between the rise time of a pulse waveform and the frequency bandwidth

The rise time of a pulse waveform is defined as the time needed for the voltage to change from 10% to 90% as shown in Fig. 9-7.

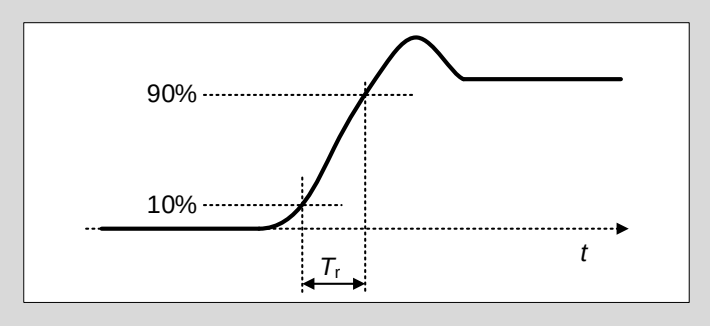


Fig. 9-7 Definition of the rise time of pulse waveform

Assuming that the rise time is T_r and the frequency at which -3dB is attained is F_{-3dB}, the following equation can be expressed.

$$T_r \cdot F_{-3dB} \fallingdotseq 0.35 \quad \text{.....(1)}$$

(2) Signal source rise time T_{r1} and oscilloscope selection

Fig. 9-8 shows the rise time of each component in an actual measurement system.

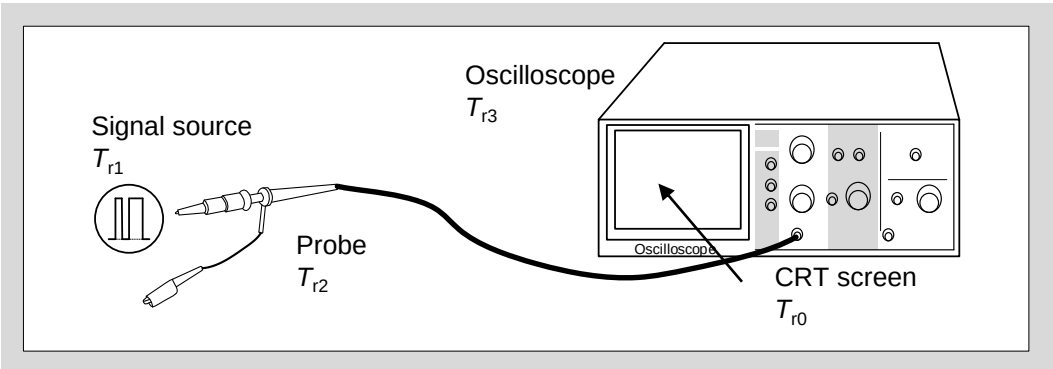


Fig. 9-8 Measurement system and rise time of each component

The rise time T_{r0} of the waveform displayed on the CRT screen of the oscilloscope is determined by the rise time of each component and is given by the following equation.

$$T_{r0} = \sqrt{T_{r1}^2 + T_{r2}^2} \quad \text{.....(2)}$$

A correct reproduction of the waveform of the signal source is accomplished by setting $T_{r0} = T_{r1}$. Assuming that:

$$\varepsilon = \frac{T_{r0} - T_{r1}}{T_{r1}} \times 100(\%) \qquad k = \frac{T_{r2} + T_{r3}}{T_{r1}} \qquad \text{.....(3)}$$

the relationship between ε and k is shown in Table 9-3, obtained using equation (2)

Table 9-3 Waveform measurement errors and rise time of signal source and measuring instrument

ε (%)	1	2	3
k	7	5	4

For example, to measure a signal with a rise time of 3.5ns with ε = 3%, the combined rise time of the probe and oscilloscope should be less than 1/4 (3.5 / 4 = 0.87ns) of the rise time of the signal source. If the rise time of the probe is ignored, solving equation (1) gives the required bandwidth of the oscilloscope as $0.35/0.87\times10^{-9} = 4\times10^{8}$, or 400 MHz. Accordingly, an oscilloscope having a frequency bandwidth of 400 MHz or above must be used.

Thus, the oscilloscope to be used should be selected according to the rise time of the signal.

2.6 Selecting probes

As mentioned before, there are voltage probes and current probes. This section describes the basics for selecting probes and the precautions on their use.

2.6.1 Voltage probes

(1) Rise time

As described in section 2.5, it is necessary to consider the frequency bandwidth of the probe to be used in accordance with the rise time of the signal. The concept of probe selection is similar to the concept of oscilloscope selection and is omitted here.

(2) Effect of the signal source impedance and probe capacitance on the rise time

Fig. 9-9 shows the electrical equivalent circuit of the measurement system, in which R_1 and C_1 denote the output impedance and capacitance of the signal source, respectively, and R_2 and C_2 denote the input impedance and capacitance of the oscilloscope, respectively.

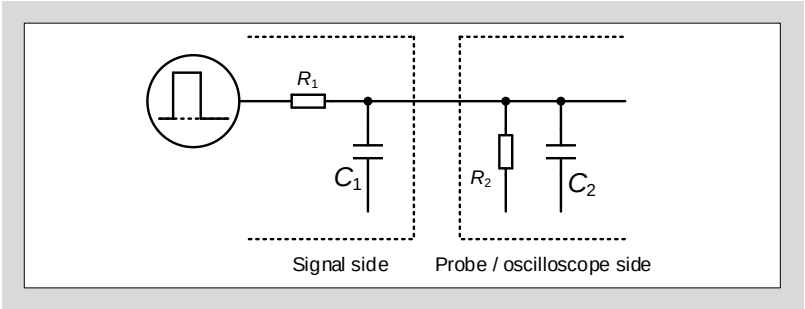


Fig. 9-9 Electrical equivalent circuit of the of measurement system

The rise time T_r of the RC filter can be expressed by

$$T_r = 2.2 \cdot R \cdot C$$

In the case of Fig. 9-9, R and C can be expressed as follows.

$$R = \frac{R_1 \cdot R_2}{R_1 + R_2} \qquad C = C_1 + C_2$$

The following facts become apparent from these relationships:

a. The higher the output impedance of the signal source, the longer the rise time becomes.
b. The larger the capacitance of the probe or oscilloscope, the longer the rise time becomes.

For example, if the signal of a signal source (R_1 = 500Ω, C_1 = 2 pF) is measured using an ordinary passive 10:1 probe (C_2 = 9.5 pF, R_2 = 10 MΩ), while the rise time is 2.2 ns when the probe is not connected, the rise time is 12 ns when the probe is connected, resulting in a significant error.

(3) Probe selection

Table 9-4 shows the guideline for selecting probes and precautions according to the measurement objectives.

Table 9-4 Guideline for selecting probes according to the measurement objectives

Objective / Item	Amplitude	Rise time, etc.	Phase difference
Probe requirements	High input impedance in the working frequency bandwidth.	Sufficient frequency bandwidth against signal source rise time.	Low input capacitance. Matched cable lengths and characteristics
Precautions	The pulse width should be at least 5 times the time constant of the probe or oscilloscope. Select a signal source with lowest impedance possible as the measurement point.	The pulse width should be at least 5 times the time constant of the probe or oscilloscope. Select a signal source with lowest impedance possible as the measurement point.	Measure the probe-to-probe time difference in advance. *A 3.5ft probe has a delay of 5ns.

(4) Precautions

Correct signal measurement requires an understanding of the probe characteristics and selection of the appropriate probe. Key items to consider when selecting a probe are listed below.

a. Is the probe suitable for the measurement objectives?
b. Is the frequency bandwidth of the probe correct for the measurement?
c. Is the maximum input voltage (withstand voltage) sufficient?
d. Will the loading effect of the probe cause a false reading? (optimal measuring point selection)
e. Is the ground (earth wire) connected properly?
f. Are there mechanical or physical strains?

When measuring high-speed switching pulses, resonance may occur due to the ground lead inductance and probe capacitance, especially in wideband oscilloscopes. Shortening the ground lead and grounding the probe tip can reduce this resonance. The necessary adapters are usually included as accessories.

In addition, multiple probes may each have their ground lead to prevent induction noise interferences as shown in Fig. 9-10. However, in this case, the potential at the points where the ground leads are connected must be equal.

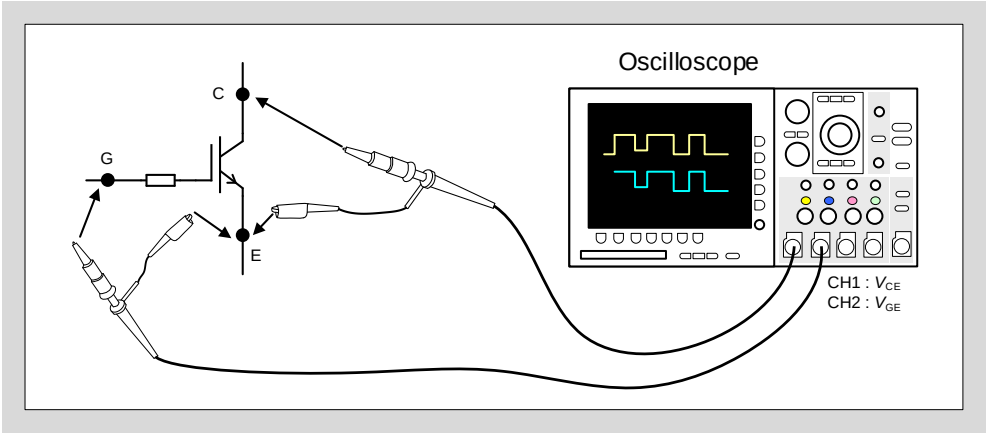


Fig. 9-10 Voltage probes connection

2.6.2 Current probes

The types and outlines of current probes are shown in section 2.3. This section describes the precautions in actual applications.

(1) Current probe selection

As mentioned before, there are two types of current probes: DC current probes and AC current probes. AC current probes, due to their excellent noise immunity, are recommended for measuring current waveforms during high-speed switching operation.

If a DC or low-frequency AC current is measured with an AC current probe, the core inside the probe will saturate and output will not be obtained. Therefore, to measure the switching operation of IGBTs used in circuits that operates with DC or low-frequency AC, some techniques are necessary, such as fabricating and using a timing control circuit to simulate the actual operation.

(2) Precautions

a. The tip of the current probe contains a ferrite core, which is extremely vulnerable to impact and must be handled with care.
b. Be careful not to exceed the ratings.
   - Withstand voltage: If the circuit voltage is high, cover the measuring point with a voltage resistant tube.
   - A-S (product of current): Pulse current rating. Excessive current may damage the probe.
   - Maximum RMS current resistance: Limited by the power capacity of the secondary circuit in the probe transformer. Exceeding this maybe burn out the probe.
c. In the case of clip type, perform measurement with the probe being securely clipped.
d. Do not leave the secondary side open with the current probe clipped to the circuit. (Especially if there is no terminator, high voltage will be generated on the secondary side)
e. Inserting the probe generates an insertion impedance on the primary side of the circuit. It is important to ensure that the insertion impedance does not affect the measurement target. Assuming that the probe is an ideal transformer, the insertion impedance can be expressed as shown in Fig. 9-11.

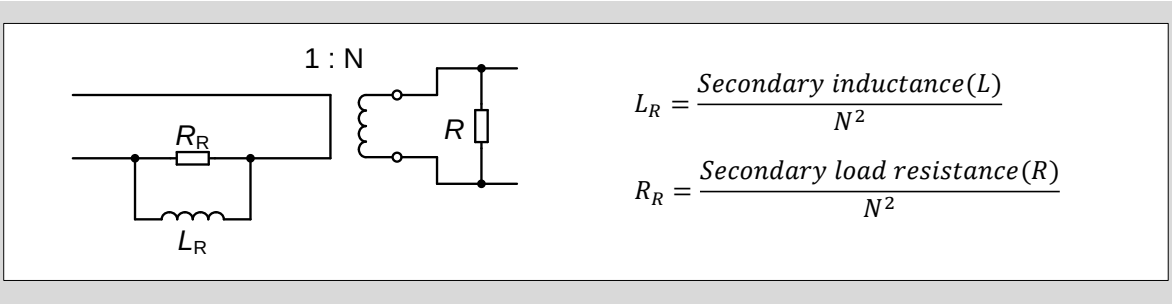


Fig. 9-11 Probe insertion impedance

2.7 Using current transformer

A current transformer is used to ease the constraint on the application range of a current probe and to minimize the effect of modifications made for measurement purposes may have upon circuit performance. Refer to section 2.3 for information on the current transformer insert locations and current measurement method.

Assuming that the number of turns (secondary) of the transformer is N, the primary current is I_1, and the secondary current is I_2, an ideal transformer would meet the relationship $I_2 = I_1/N$. Considering the excitation current I_0, the relationship can be rewritten as follows.

$$I_o = I_1 - N \cdot I_2$$

The excitation current must be a small value because it might cause measurement error. Check the current transformer N value, measure I_1 and I_2, and calculate I_0 from the above equation to make sure that the measurement accuracy is acceptable. Also, be careful not to drop the ferrite core of the current transformer, which is extremely vulnerable to impact.

Chapter 10 EMC Design of IGBT Module

This chapter describes the EMC design guidelines for IGBT modules.

1. General Information of EMC in Power Electronics Equipment

Recently, EMC countermeasures coping with European CE Marking and Japanese VCCI (Voluntary Control Council for Interference by Information Technology Equipment) standards are essential in designing power electronics equipment such as PDS (Power Drive System) and UPS (Uninterruptible Power Supply) using IGBT modules.

EMC stands for Electro Magnetic Compatibility, which is classified into EMI (Electro Magnetic Interference) and EMS (Electro Magnetic Susceptibility). EMI is the adverse effects that electronic devices have on peripheral equipment, and it is also called Emission. There are two kinds of EMI, one is conducted emission that leaks to power line and the other is radiated emission that radiated as electromagnetic wave. EMS is the immunity performance of electronics equipment against disturbance, such as electromagnetic wave, voltage sag, electrostatic discharge, EFT/burst and lightning surge from the surrounding and it is also called Immunity. This can be simplified as shown in Fig.10-1.

Since IGBT modules are capable of high-speed switching of several hundreds of volts and amps in 500ns or less, reducing both conducted emission and radiated emission is important when designing power electronics equipment.

In this chapter, effects of IGBT modules switching, which is likely to cause troubles to other equipment (EMI characteristics), and the countermeasures are introduced.

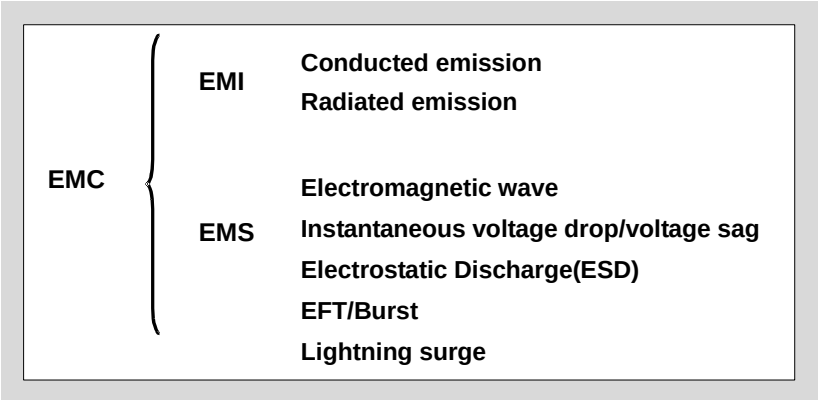


Fig. 10-1 Classification of EMC

1.1 EMI performance

IGBT modules are used in a wide range of application field and power including home appliances such as air conditioners and refrigerators, automobiles and traction system, as well as industrial. Here, we introduce the EMI standards for variable speed drives such as general-purpose inverters, which is one of the main application of IGBT modules.

(1) Conducted emission (noise terminal voltage)

In IEC61800-3, the limits (QP (Quasi-Peak) values) of conducted emission for PDS is shown in Fig. 10-2.

The limits in the standard are classified into Category C1, applied for equipment used in commercial area, and Category C2 and C3, applied for equipment used in industrial area. Industrial PDS are designed to meet Category C3 limits.

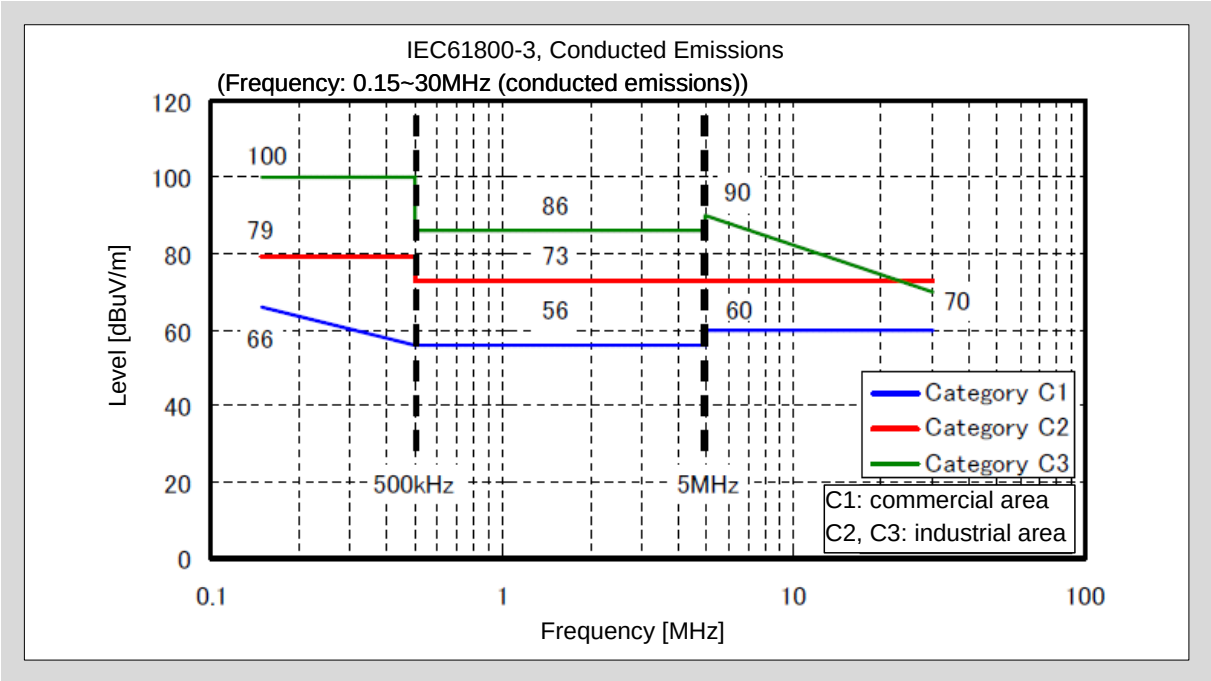


Fig. 10-2 Limits of conducted emissions in IEC61800-3

(2) Radiated emission

Fig. 10-3 shows the limits of radiated emission (radiated noise) for each category.

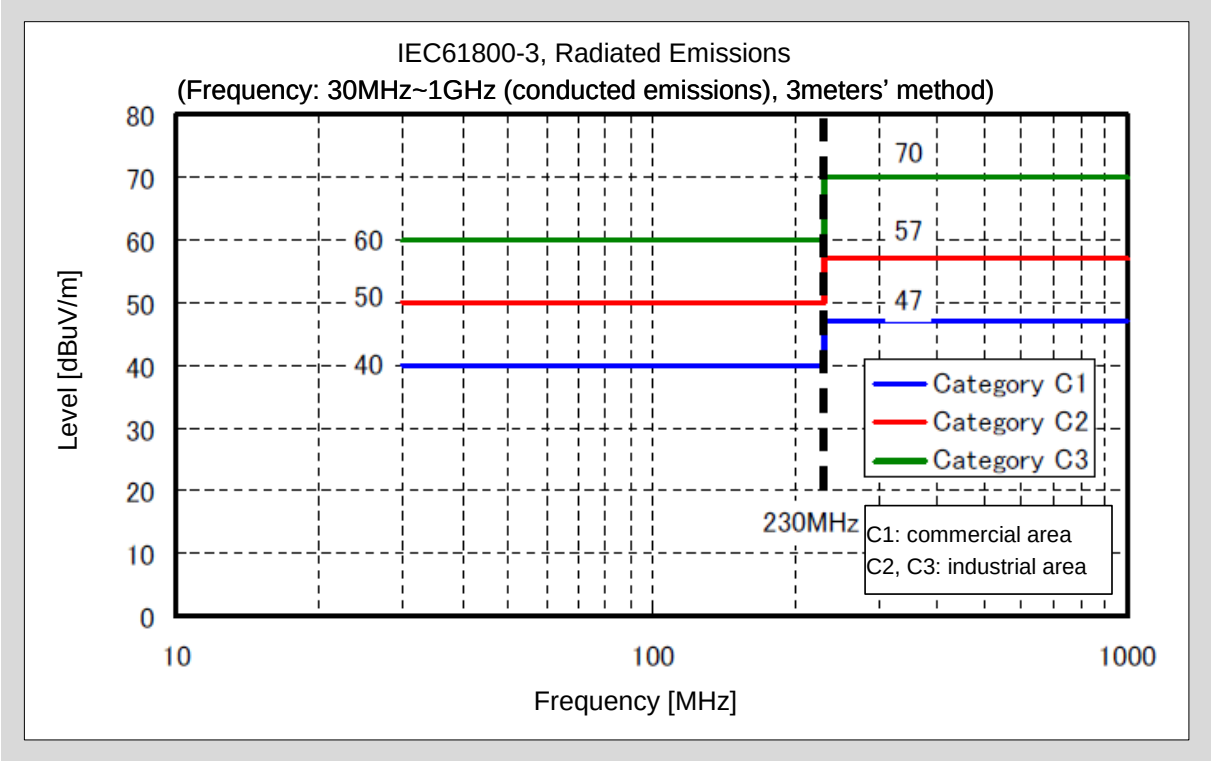


Fig. 10-3 Limits of radiated emissions in IEC61800-3

The category classification is defined as shown in Fig. 10-4.

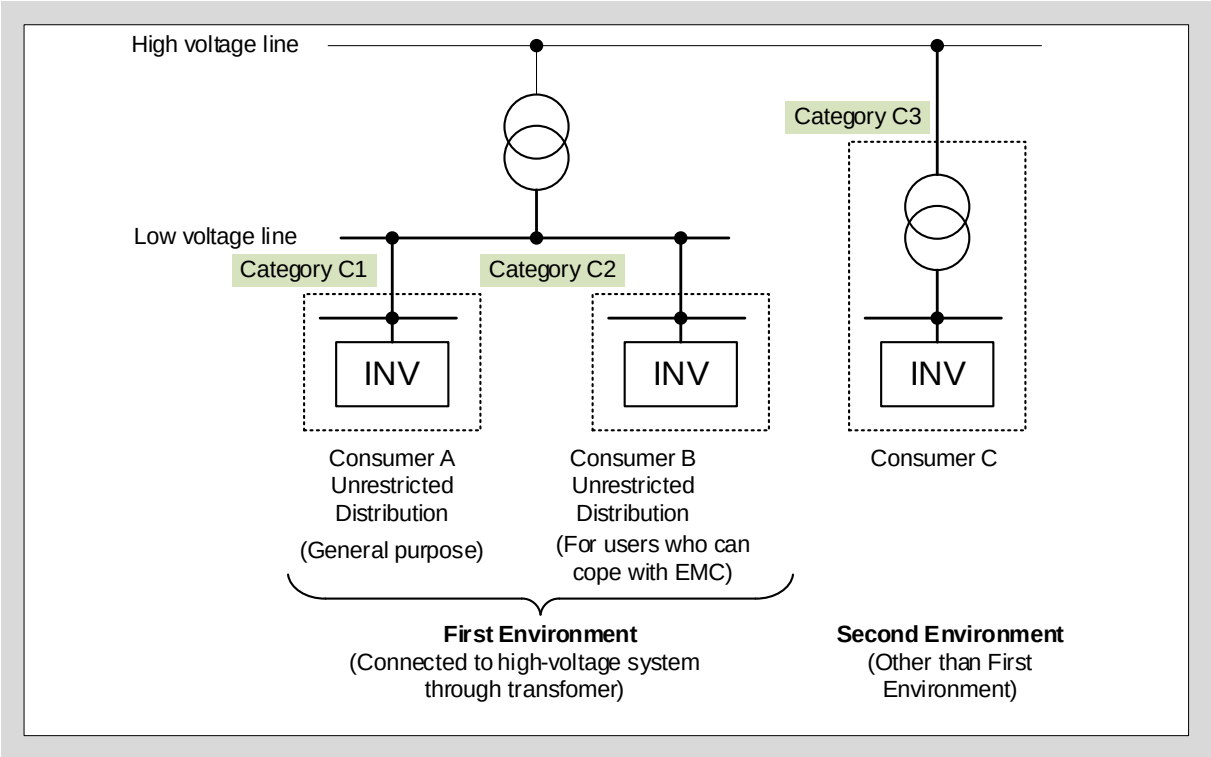


Fig. 10-4 Category classification in IEC61800-3

2. EMI Countermeasure Design for Inverters

2.1 Common mode and normal mode noise

The propagation path of conducted emission is mainly classified into two types, normal mode and common mode.

The normal mode noise is generated by high d*v*/d*t* and d*i*/d*t* due to switching of IGBT, and appears at AC input and output terminals. The path of the normal mode noise is shown in Fig. 10-5.

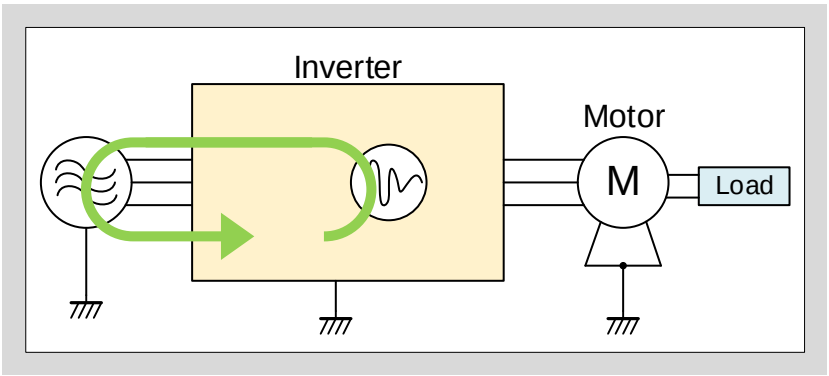


Fig. 10-5 Path of normal mode noise

On the other hand, the common mode noise is generated by potential fluctuation against ground caused by switching, which charge and discharge stray capacitance that exists between the main circuit and ground and in the transformers. Noise current is propagated through the ground line. The path of common mode noise is shown in Fig. 10-6.

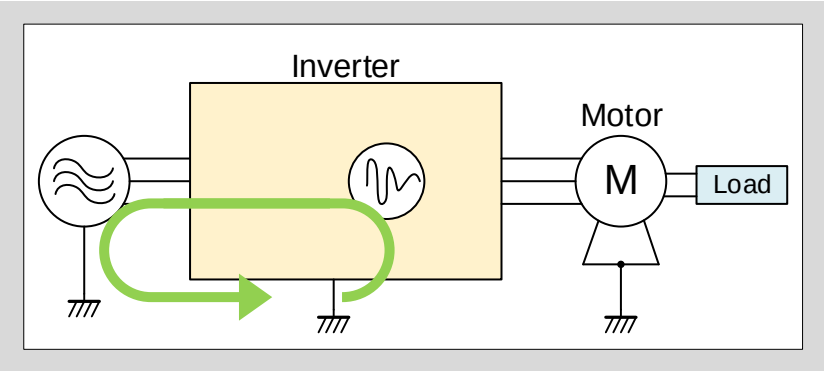


Fig. 10-6 Path of common mode noise

In actual equipment, there is impedance imbalance in the wiring of each phase (e.g. R/S/T phases), thus normal mode noise may be converted to common mode noise via the ground line (Fig. 10-7), or vice versa. Therefore, it is very difficult to separate the noise through the normal mode path and the noise through the common mode path in actual noise spectrum. As a general precaution, it is necessary to prevent unbalanced wiring of each phase as much as possible.

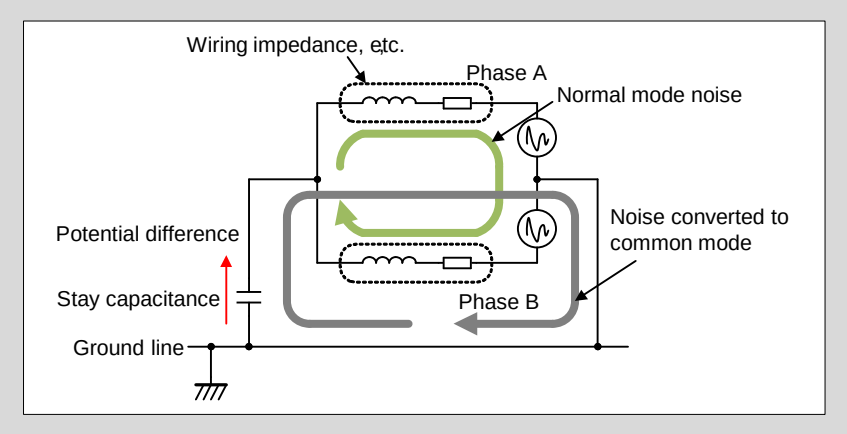
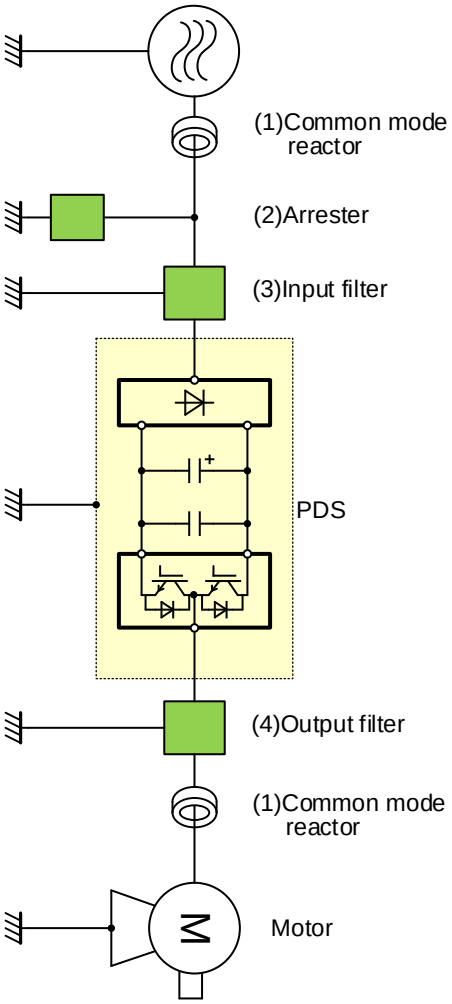


Fig. 10-7 Conversion from normal mode noise to common mode noise

2.2 Countermeasures against EMI noise in PDS

Fig. 10-8 shows example of countermeasures against noise in PDS. It is possible to suppress noise (mainly harmonic current and conducted emission) generated by the PDS by inserting countermeasure components such as commercial noise filters and reactors.



The effect of each components are as follows.

(1) Common mode reactor
This is a reactor of the common mode to be inserted into the input/output line. It is effective in suppressing noise up to the several MHz band.

(2) Surge protective device (Arrester)
This is installed to protect the PDS from induced common mode and normal mode lightning that flows from the input power line.

(3) Input filter
Composed of L, C, and R, it suppresses noise flowing out to the input power line.
Various products with different noise attenuation characteristics are available in the market, thus proper selection should be made in accordance with the specification and purpose.
Since attenuation effect may be inferior depending on the installation method, proper wiring and installation in accordance with the instruction manual is required.

(4) Output filter
This is used to suppress surge voltage applied to the motor and to suppress induced noise in the output cable.

Fig. 10-8 Noise countermeasures for PDS

Such filters installed outside the PDS as described above are generally effective in suppressing noise in the 100kHz to several MHz band, but may be less or not effective for higher bands (conducted emissions above 10MHz and radiated emissions above 30MHz). This is because there are limits to the frequency characteristics of filters, thus in order to effectively suppress noise over a wide range of frequency, it is necessary to install optimum filters for each frequency band.

One of the causes of noise around 10MHz to 50MHz is thought to be due to the resonance associated with switching caused by the inductance and stray capacitance around the IGBT modules inside the PDS.

The following section describes the mechanism of noise generation around the IGBTs and the countermeasures.

2.3 Mechanism of noise generation attributable to IGBT module characteristics

Fig. 10-9 shows the block diagram of a typical PDS. AC power source is rectified into DC by rectifier diodes, and then reversely converted into AC by high frequency switching of the IGBT in the inverter portion, thereby achieving variable speed driving of the motor. The IGBT modules and rectifier diodes are mounted on a heat sink, and in some cases this heat sink is a part of the PDS body, thus it is normally grounded for safety reasons.

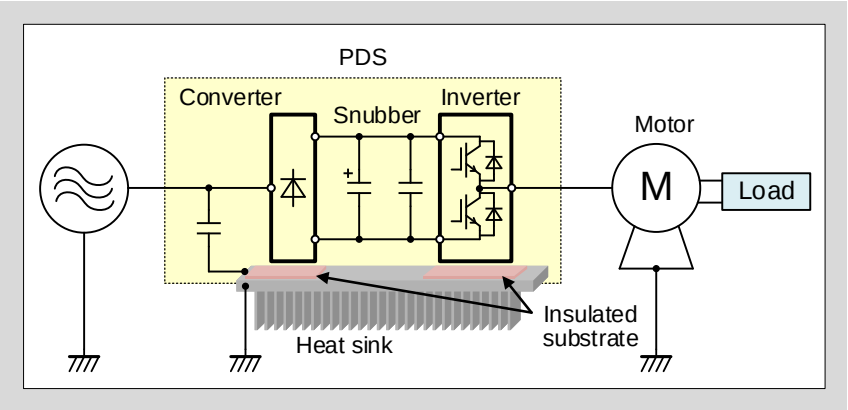


Fig. 10-9 Example of power drive system

In this system , the metal base of IGBT module mounted on a heat sink and the electric circuit side such as IGBT chip are insulated by an insulating substrate with high thermal conductivity (for the detailed structure of the module interior, refer to Chapter 1). In addition, a snubber capacitor is connected to the inverter circuit to suppress surge voltage.

In particular, stray capacitance and stray inductance that exist in IGBT modules and electrical components can have a large impact in high frequency bands of MHz order, such as radiated and conducted emission. Fig. 10-10 shows a schematic diagram of a PDS in the high frequency band of hundreds of kHz to tens of MHz. There is stray inductance of tens to hundreds nH on the wiring around the IGBT module, and stray capacitance of hundreds pF exists on the insulating substrate. Also, junction capacitance exists at the PN junction of the IGBT itself.

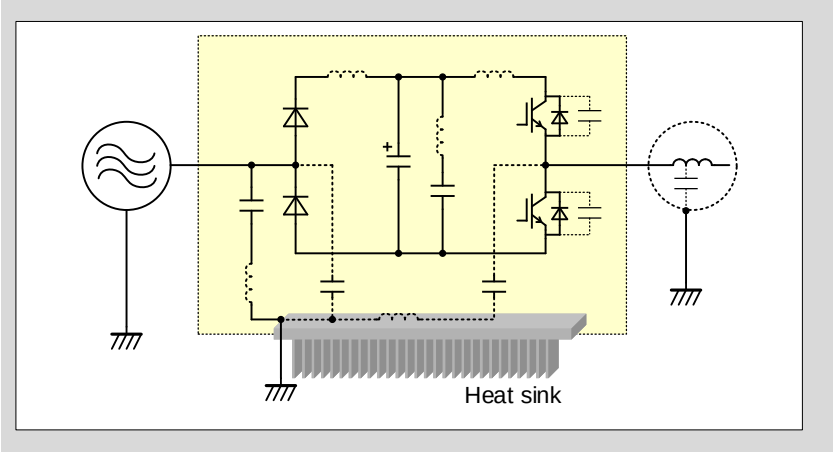


Fig. 10-10 Equivalent circuit considering stray L and C

For example, if the wiring stray inductance is 200nH and the stray capacitance of the substrate is 500pF, and if they form a loop, the resonance frequency f_0 of the loop is calculated as Fig. 10-11.

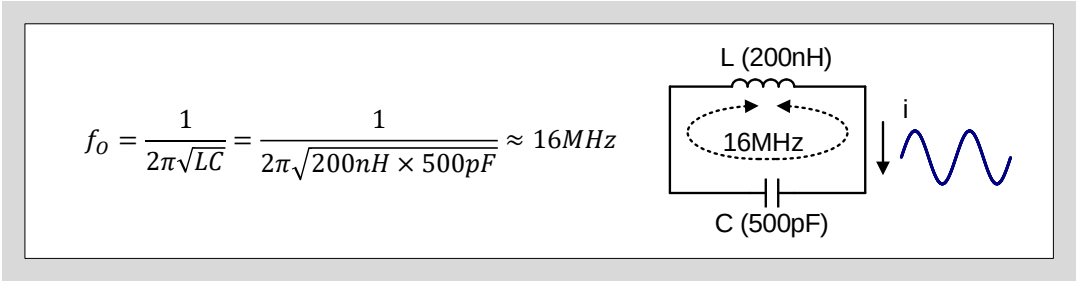


Fig. 10-11 Resonance phenomenon between stray inductance and stray capacitance

If IGBT switching becomes a trigger and resonant current of 16MHz flows in the loop, the resonant current will generate conducted emission and radiated emission. In the case shown in Fig. 10-10, common mode noise current of 16MHz flows through the insulating substrate of the IGBT module to the ground line, and is propagated to the power supply and appears as conducted emission peak. If this resonance frequency becomes 30MHz or higher, it will be observed as radiated emission peak.

Table 10-1 shows examples of stray capacitance and inductance values of each circuit component.

Table 10-1 Examples of stray capacitance and inductance values for each circuit components

Circuit components	Stray capacitance	Stray inductance	Remarks
Between P and N terminals of IGBT module	-	20 ~ 40nH	
IGBT chip	100 ~ 200pF	-	Voltage dependency is large
Snubber capacitor	-	20 ～ 40nH	
Insulating substrate	500 ~ 1000pF	-	
Electrolytic capacitor	100pF	-	Between internal electrode and mounting metallic band
Reactor with iron core	50 ~ 200pF	-	Reactor works as a capacitor at several MHz or higher
Varistor	100 ~ 200pF	-	Stray C is smaller as voltage rating is higher
Motor	13000pF	-	Example of 3φ15kW motor
Shielded 4-core cable	Hundreds of 100pF	Hundreds of nH ~ several μH	Per 1m
Busbar	-	Hundreds of nH	About 100nH per cm

In an actual system, these components are connected in a complicated manner, and unintended LC resonant circuit may be formed. During IGBT switching, resonance occurs in these LC circuits, which is measured as conducted emission and radiated emission peak.

Table 10-2 and Fig. 10-12 show resonance loops that tend to cause the peaks in conducted and radiated emissions.

Table 10-2 Example of resonance frequency and loop in PDS

No.	Frequency	Conducted/radiated	Normal/common	Path
(1)	1 ~ 4MHz	Conducted	Common	Motor capacitance ~ wiring inductance
(2)	5 ~ 8MHz	Conducted	Common	DCB substrate capacitance and wiring inductance
(3)	10 ~ 20MHz	Conducted	Common	DCB substrate capacitance and wiring inductance
(4)	30 ~ 40MHz	Radiated	Normal	Device capacitance ~ snubber capacitance

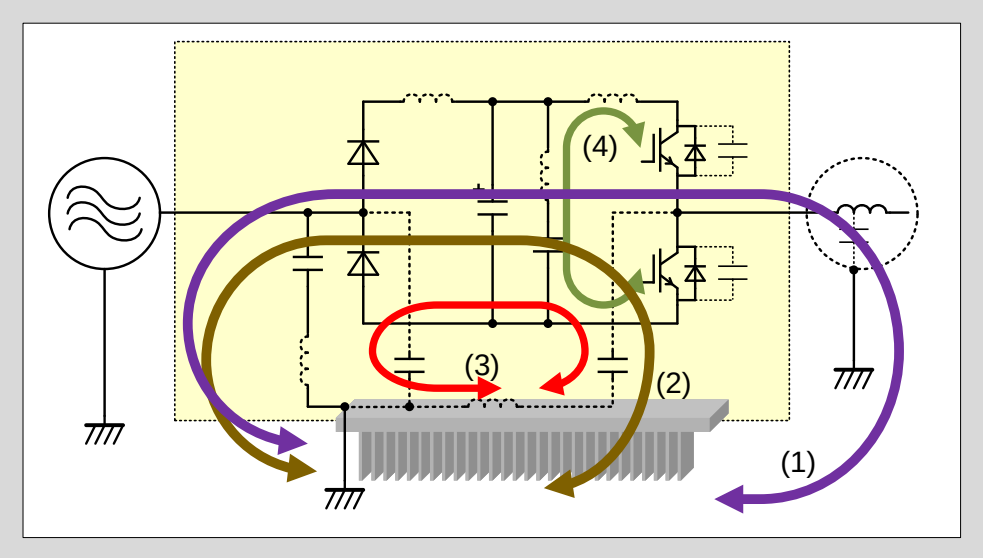


Fig. 10-12 Example of path in Table 10-2

The wire length (inductance) and stray capacitance vary depending on the system configuration, but approximate resonance frequency can be estimated by roughly estimating the inherent stray L and C values of the target system.

2.4 Frequency bands affected by IGBT module characteristics

As aforementioned, the frequency of the conducted emission for a PDS such as general-purpose inverter is 150kHz to 30MHz. Fig. 10-13 shows an example of measured conducted emission in PDS. As shown in Fig. 10-13, the conducted emission is highest around 150kHz, and as the frequency becomes higher, it is mildly attenuated.

This spectrum of conducted emission shows the harmonics of the rectangular switching waveform at the carrier frequency (several kHz to 20kHz), therefore it is almost unaffected by the switching characteristics of the IGBT module itself. This is because, as shown in Fig. 10-14, the voltage rise time and fall time during IGBT module switching are about 50 to 200ns, which is equivalent to frequency of 2 to 6MHz, and in the frequency band lower than this, spectrum of conducted emission does not depend on the difference between the rise time and fall time of the IGBT module

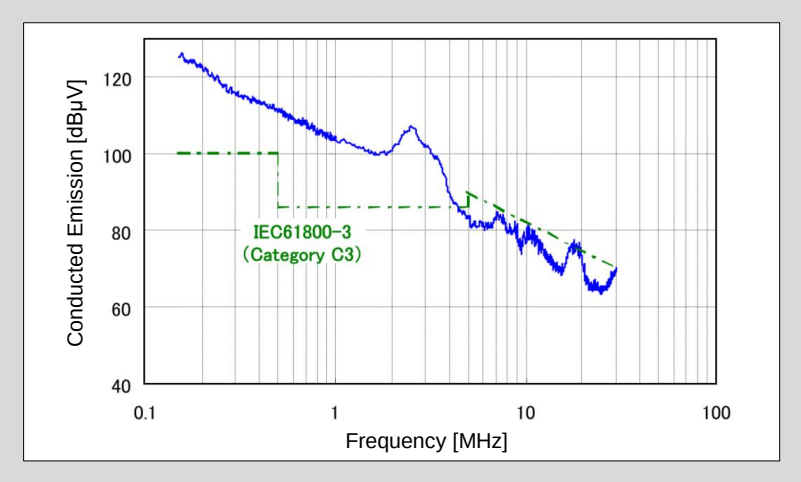


Fig. 10-13 Example of conducted emission of PDS

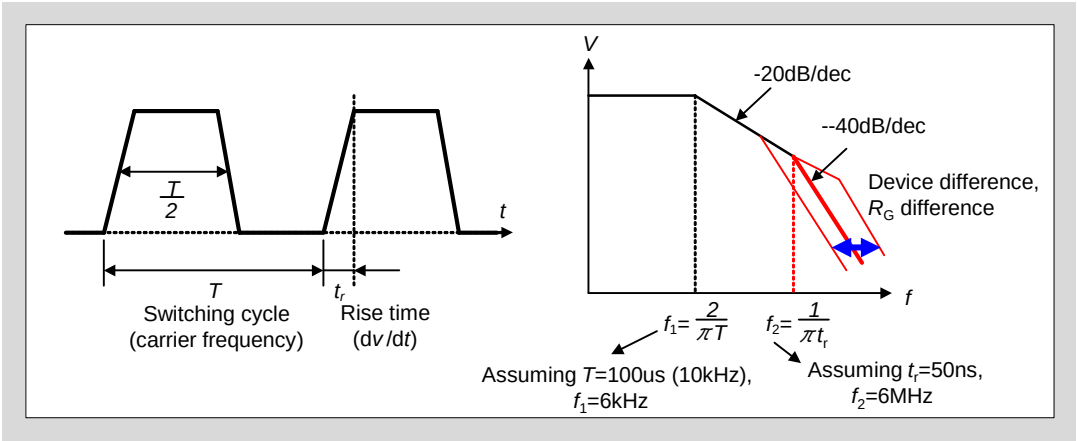


Fig. 10-14 IGBT voltage waveform and frequency spectrum

Fig. 10-15 shows an example of measurement results of radiated emission (30MHz~). Like the conducted emission, the radiated emission become the highest around 30MHz, which is the lowest frequency of the standard, and tend to attenuate as the frequency becomes higher. As shown in Fig. 10-15, the noise spectrum due to IGBT switching does not have a sharp peak like those seen in CPU clocks, but a relatively broad characteristics.

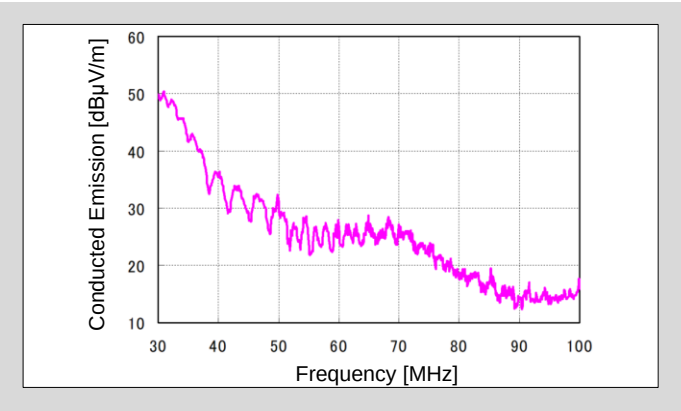


Fig. 10-15 Example of radiated emission spectrum

3. EMI Countermeasures in IGBT Modules Application

3.1 Measures against emission

3.1.1 Filter installation

As countermeasure against conducted emission, it is common to install a filter on the AC power supply input side to prevent the noise current generated by the inverter from flowing out to the AC power line. The filter is composed of *L* and *C* elements, and the cutoff frequency of the filter is designed that sufficient attenuation will be obtained for the target standard value. Since various filters for emission suppression are commercially available, a proper one should be selected according to the relevant standard and required current.

Fig. 10-16 shows the suppression effect of an input filter designed to comply with Category C2 of IEC61800-3. The conducted emission, which was about 125dBμV at 150kHz without the filter, is attenuated to 70dBμV, thus clearing the standard value with a margin of several dBμV.

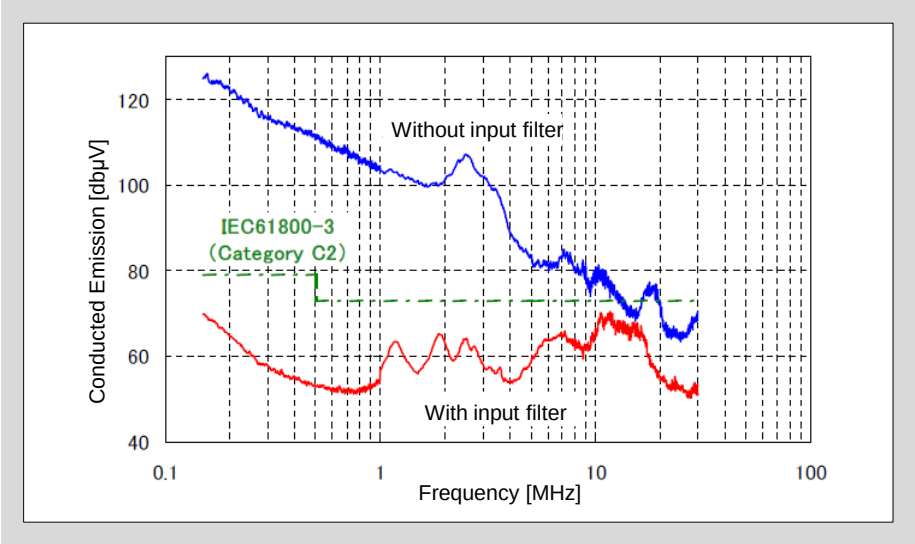


Fig. 10-16 Example of conducted emission in 3φ200V/37kW PDS (QP value)

3.1.2 Cautions when applying filters

In the case of an ideal filter, the attenuation becomes larger as the frequency increases. However, in an actual filter, ideal attenuation characteristic can no more be obtained above a certain frequency as shown in Fig. 10-17. This is because as aforementioned, stray RLC exist in parts used for the filter circuit, and the attenuation effect tends to decrease at the frequency band above 1MHz as shown in Fig. 10-16.

Furthermore, the peak occurs in the high frequency band around 10MHz, and so the margin against the standard is the smallest. Depending on the measuring environment, the level around 10MHz may rise and exceed the standard value.

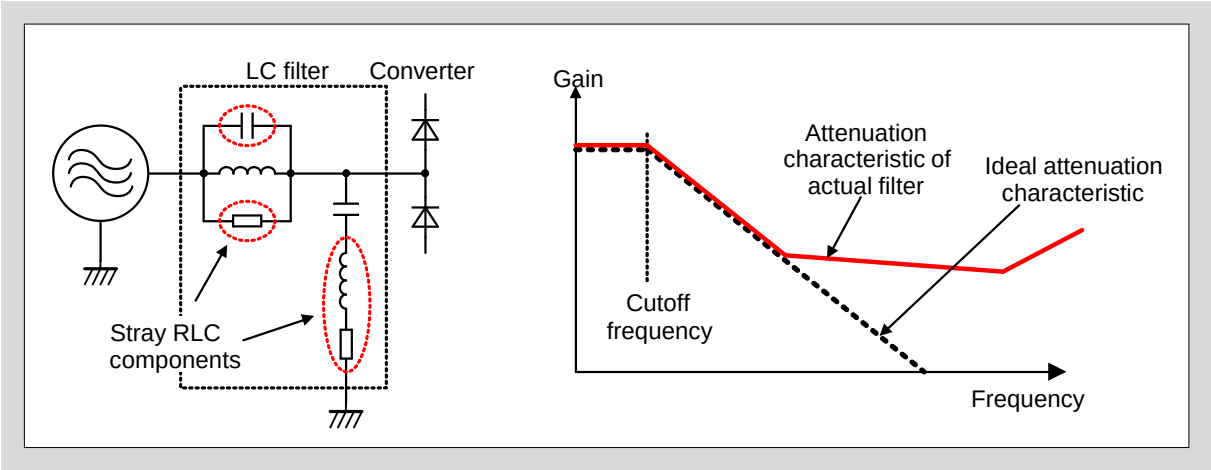


Fig. 10-17 Attenuation characteristics of ideal filter and actual filter

One factor that causes the emission peak occurs in the 10MHz or higher band described in the previous section is the resonance via the insulating substrate of the IGBT module. Assuming that the stray capacitance of the insulating substrate and stray inductance of main circuit are such values as shown in Fig. 10-11, the peak value of conducted emission will occur at 16MHz. The LC values of a loop that resonates at frequency of 10MHz or higher are in the order of hundreds of pF and hundreds of nH, and may be caused by the capacitance of the IGBT chip, insulating substrate capacitance, and wiring inductance inside the package. Fig. 10-18 shows an example of common mode circuit model of resonance via the DCB substrate.

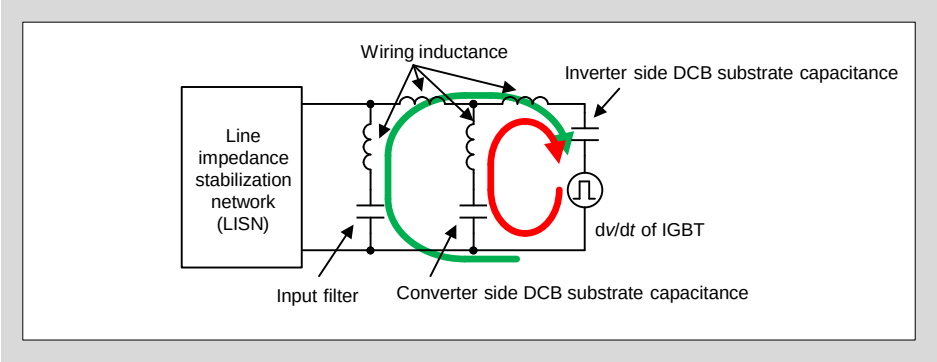


Fig. 10-18 Example of circuit model of resonance via IGBT insulating substrate

This shows the resonance between the inductance of the capacitor connected as an input filter and the DCB substrate capacitance of inverter side module, and the resonance between the converter and the inverter module. When filter or varistor is added as emission countermeasure, it should be noted that peak may occur due to the resonance with the stray L and C of the filter.

3.1.3 Measures against conducted emission of IGBT modules

In order to reduce the peak occurring in the high frequency band of conducted emission spectrum as described above, it is necessary to:

a. Decrease IGBT switching d*v*/d*t*

b. Increase the impedance the resonance loop to suppress the resonance current

However, there are the following demerits.

a. IGBT loss will be increased when d*v*/d*t* is decreased.

b. Simply increasing/decreasing the constants of L and C will result in shifting the resonance frequency, and it is difficult to decrease the peak value. It is impossible to eliminate the stray L and C components structurally and physically.

(1) Measures against conducted emission by adjusting gate resistance

Fig. 10-19 shows an example of conducted emission spectrum of PDS in which the IGBT 7MBR75U4B120 is applied (with input filter). From Fig. 10-19, it can be observed that the conducted emission peak around 10MHz is suppressed by about 5dBμV when the gate resistance is doubled and tripled from the standard value of 22Ω. However, even if the gate resistance is doubled or more, the suppression effect is small, thus it is necessary to judge the suppression effect considering the demerit of increased switching loss.

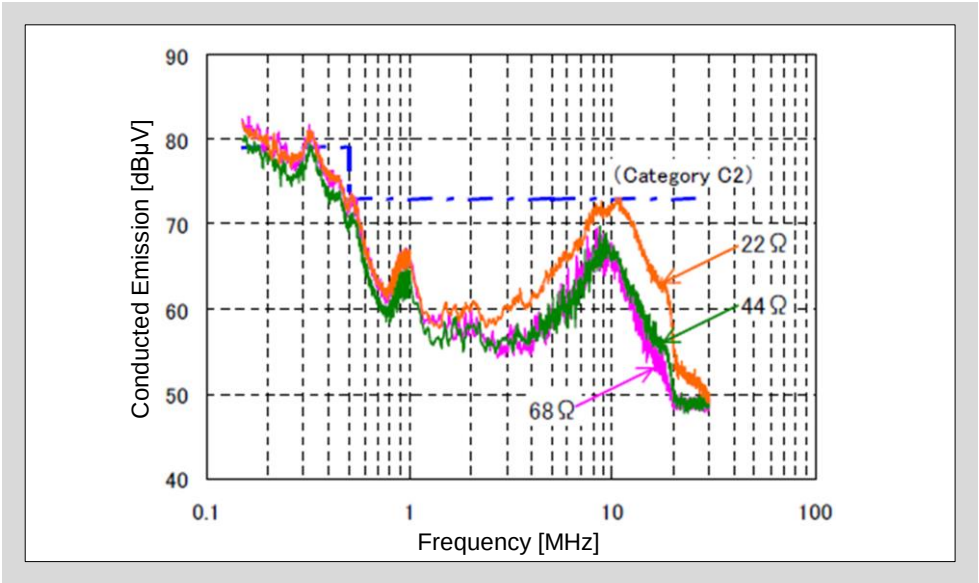


Fig. 10-19 Example of conducted emission spectrum with different gate resistance

(2) Suppression of resonance with ferrite core

The ferrite core is one of the component that is often used for emission suppression. Its equivalent circuit is normally shown as a series circuit of L and R (Fig. 10-20). The characteristics of the ferrite core as magnetic material (L component: μ‘, R component: μ‘‘) is shown in Fig. 10-21.

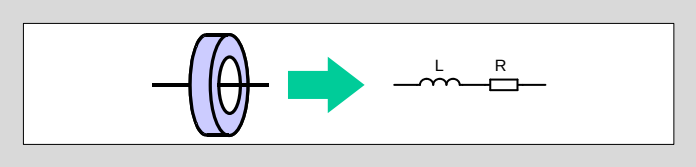


Fig. 10-20 Equivalent circuit of ferrite core

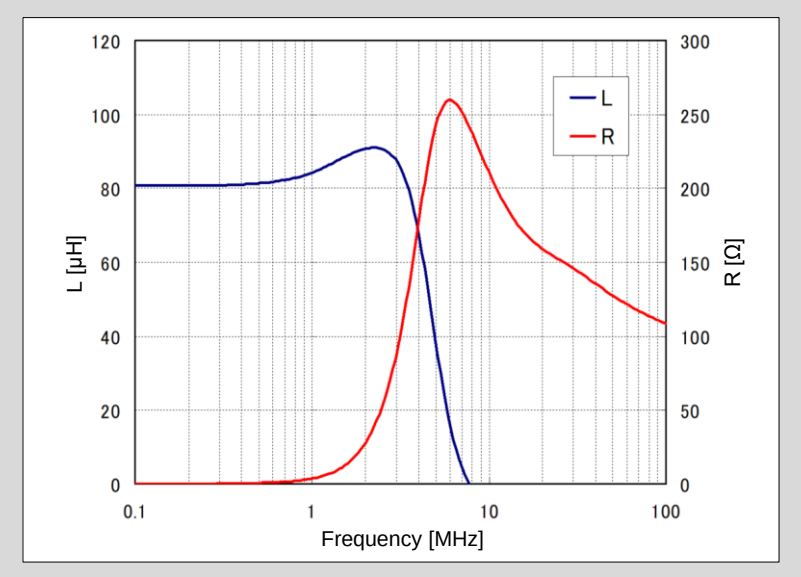


Fig. 10-21 Example of ferrite core impedance (L, R) characteristics

If the ferrite core is inserted into the resonance loop that produces the emission peak described above, the circuit model will be as shown in Fig 10-22.

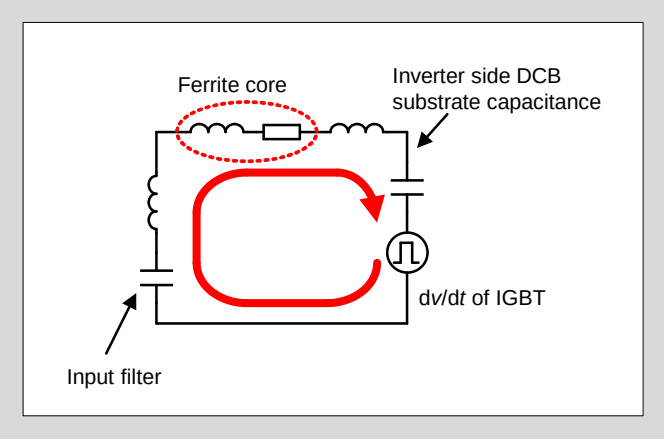


Fig.10-22 Equivalent circuit when ferrite core is inserted

By selecting a ferrite core material with optimum impedance characteristics according to the loop constant (resonance frequency), it is possible to suppress the emission peak by damping the resonance.

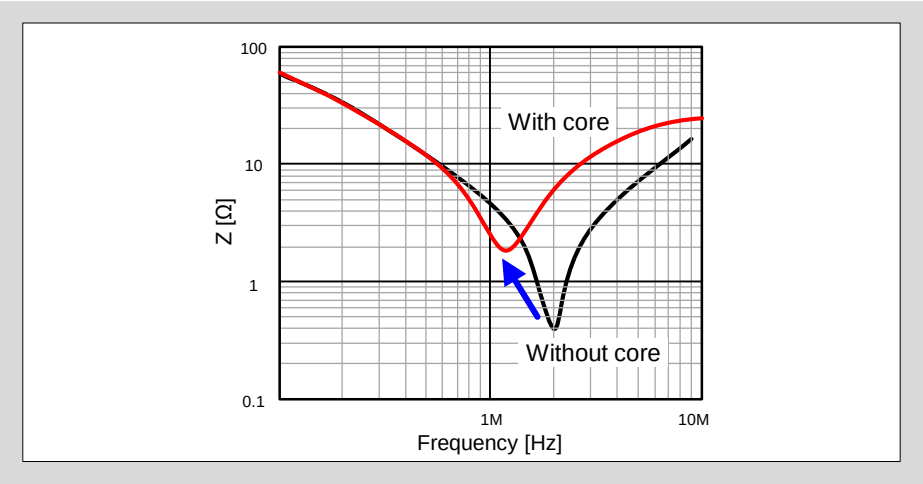


Fig. 10-23 Impedance characteristics of resonance loop with and without core

Fig. 10-23 shows the impedance characteristics of the resonance loop with and without core. At the resonance point, the impedance is lowest and a large resonance current flows, causing a peak in the conducted emission. By inserting the core, the impedance is increased, and the conducted emission can be effectively suppressed by damping the resonance.

Fig. 10-24 and Fig. 10-25 show an example of inserting the ferrite core in the PDS main circuit and the suppression effect, respectively.

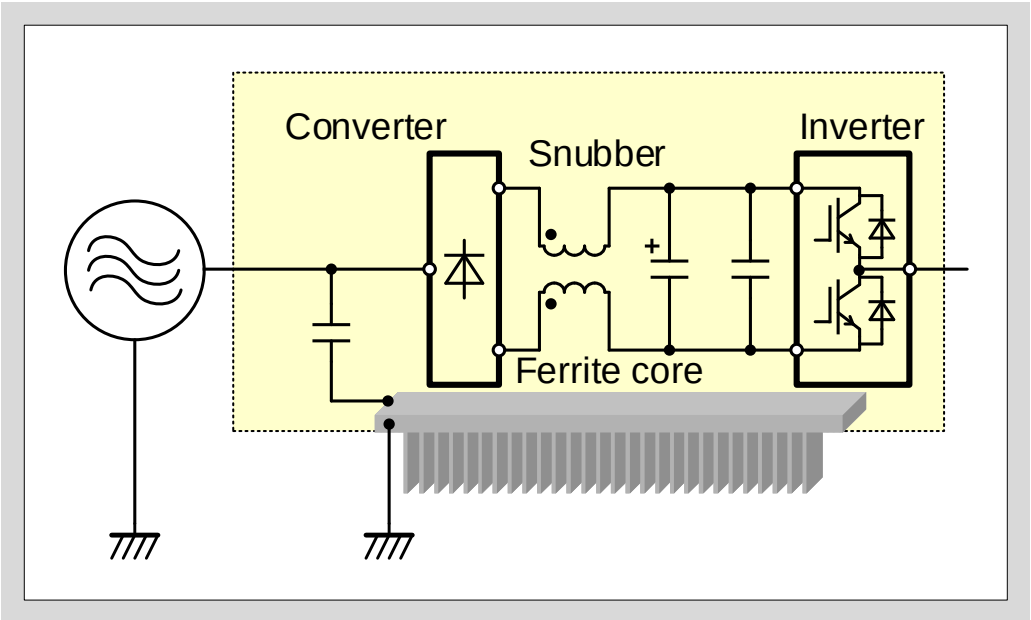


Fig. 10-24 Example of countermeasure using ferrite core

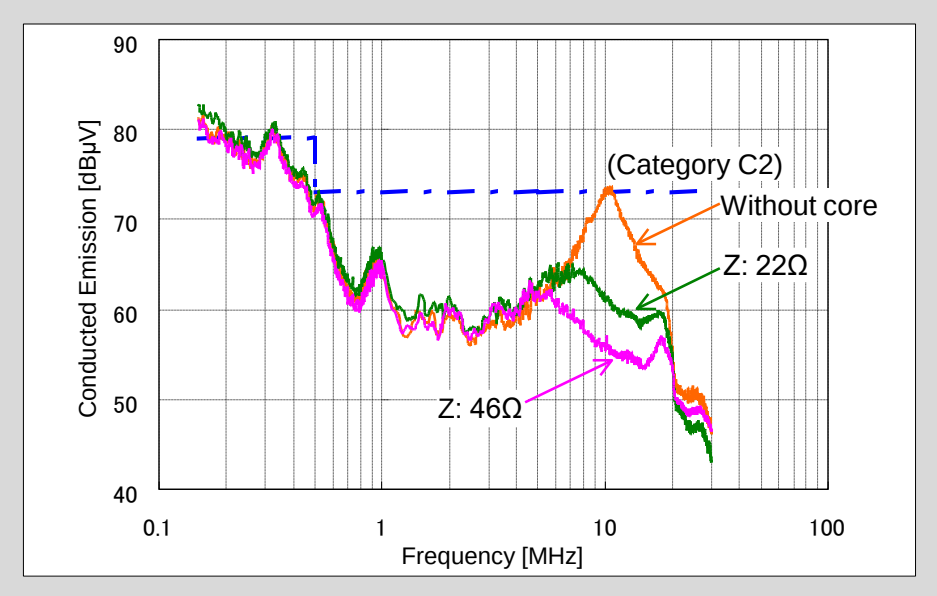


Fig. 10-25 Conducted emission measurement result

Since the loop impedance when no measure is taken is about 8Ω, peak reduction of about 10dB can be achieved by increasing it to about 30Ω by means of the ferrite core.

Unlike the gate resistance method, applying the core can reduce the emission without increasing the IGBT loss.

3.1.4 Measures against radiated emission of IGBT module

The main cause of radiated emission is considered to be the high frequency LC resonance caused by the device junction capacitance and wiring stray inductance (mainly the module internal wiring, and wiring between the module and snubber capacitor, refer to Fig. 10-26) that is triggered by high d*v*/d*t* that occurs during the IGBT turns on (reverse recovery of the FWD on the opposite arm). This is the same generation mechanism as the peak in the conducted emission described above.

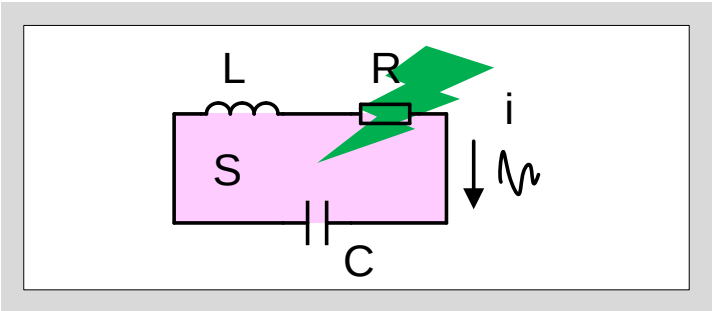


Fig. 10-26 Loop composed of IGBT module and snubber C

Generally, the far electric field E_f at frequency f radiated from a small current loop (the aforementioned LC loop here) placed in a free space is given by the following equation.

$$Ef = \frac{1.32 \times 10^{-14}}{r} \cdot S \cdot If \cdot \sin\theta \qquad \text{.....(1)}$$

r: distance from loop, *S*: area of loop, *If*: loop current, *θ*: angle from loop surface

From equation (1), it is known that *Ef* is inversely proportional to the distance from the loop and proportional to the loop area and loop current.

The current value *If* is given by the following equation.

$$If = \frac{E}{Z} \qquad \text{.....(2)}$$

E: voltage spectrum of IGBT switching waveform (Fig. 10-14), Z: loop impedance

From the above equation, the following measures may be considered to reduce radiated emission.

[1] Increase the distance from the loop
[2] Decrease the loop area S
[3] Decrease the loop current
  [3]a. Decrease the switching voltage spectrum
  [3]b. Increase the loop impedance

As for [1], the measurement at a distance of 10m or 3m is specified in the standard, therefore the practical measures are [2] or [3].

(1) Decrease the loop area S

As described above, the high frequency noise current induced during switching is the resonant current of the LC loop formed by the device capacitance and the snubber capacitor (path [4] in Fig. 10-12).

For 2-Pack medium/large capacity modules, it is necessary to minimize the radiation area of the loop by connecting the snubber capacitor directly to the terminals. This is also effective from the viewpoint of surge voltage suppression during switching.

Pin terminal type modules such as 6-Pack and PIM types are mostly mounted on the power board, but it is important for the snubber capacitor to be placed as close to the P/N terminal pins as possible.

(2) Decrease the voltage spectrum

As described above, the voltage spectrum during IGBT/FWD switching is shown in Fig. 10-27.

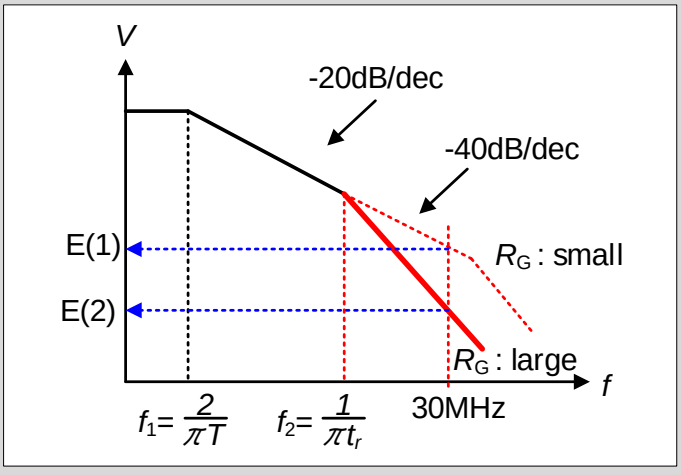


Fig. 10-27 IGBT switching voltage waveform spectrum

Conventionally, increasing the gate resistance to decrease the switching speed has been generally applied as a countermeasure. This lower the frequency of f_2, and reduce the spectrum above 30MHz as shown in Fig. 10-27. In comparison with the voltage component E(1) at 30MHz when R_G is small and the d*v*/d*t* is large, the voltage component when R_G is large and d*v*/d*t* is small becomes smaller like E(2). Since E(1), E(2) are equivalent to E in equation (2), reducing the d*v*/d*t* results in suppressing the noise current *If*.

Fig. 10-28 shows an example of radiated emission dependence on gate resistance. By setting the gate resistance value to about twice the value described in the specification, the radiated emission can be greatly suppressed. However, if the radiated emission is suppressed by adjusting the gate resistance, switching d*v*/d*t* becomes slower, and switching loss increases. As a result, depending on the operating conditions of the equipment, the temperature may rise and the junction temperature may exceed the rating, thus evaluation is required.

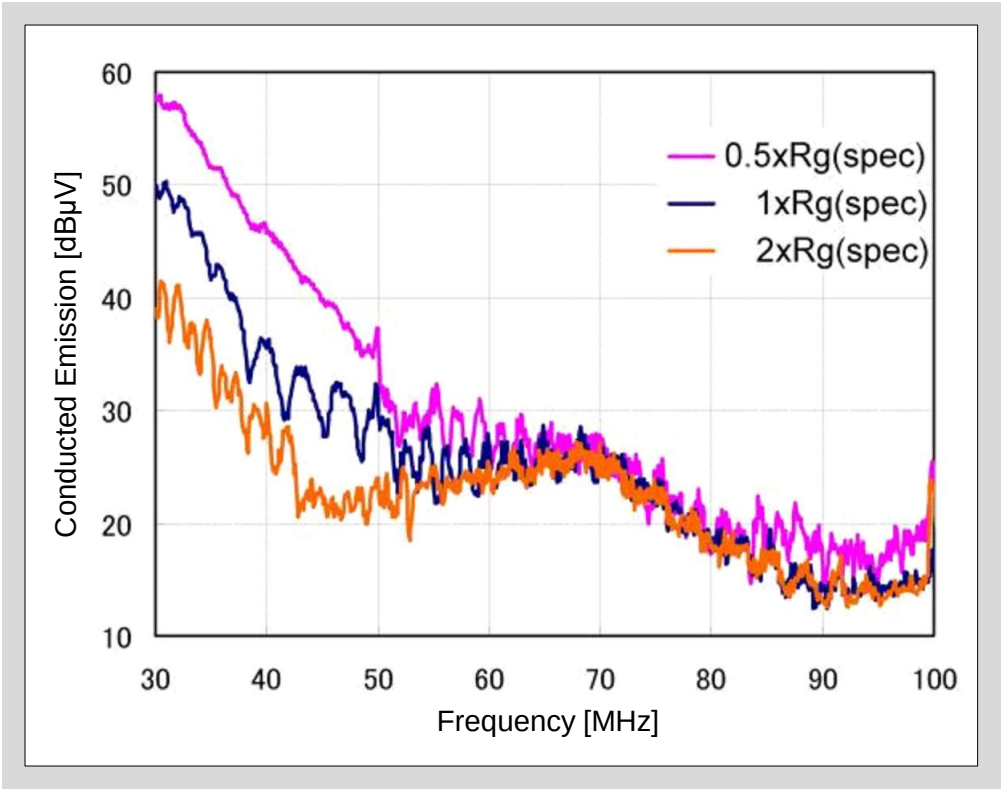


Fig. 10-28 Radiated emission dependence on gate resistance (7MBR100U4B-120)

3.1.5 Summary

As described above, the EMI generated by IGBT switching (especially high frequency conducted emission at 10MHz or higher, and radiated emission) is caused by the resonance of stray L and C existing in the IGBT itself and on its peripheral circuit. These stray L and C components cannot be reduced to zero in principle and physically. Therefore, it is important to accurately identify the loop resonance that cause these problems and take proper countermeasures.

Chapter 11 Reliability of Power Module

The market for power modules is not limited to general-purpose inverters, servo motors, NC machines, elevators, etc., but is expanding into new applications such as electric vehicles, solar, wind and fuel cell power generation systems.

Fuji Electric has developed various power modules to meet the market demands. In the future, as the market expands further, the performance requirements for these power modules are expected to become even more diverse and sophisticated.

To meet these demands, it is necessary to pay attention to ensuring the reliability of the power modules. This chapter describes the reliability of power modules, especially IGBT modules.

1. Basis of Reliability

In general, the failure rate of electronic devices and components such as IGBT modules follows a bathtub-shaped failure rate curve as shown in Fig. 11-1. This failure rate curve is shown in three periods: the early failures period, random failures period, and wear-out failures period.

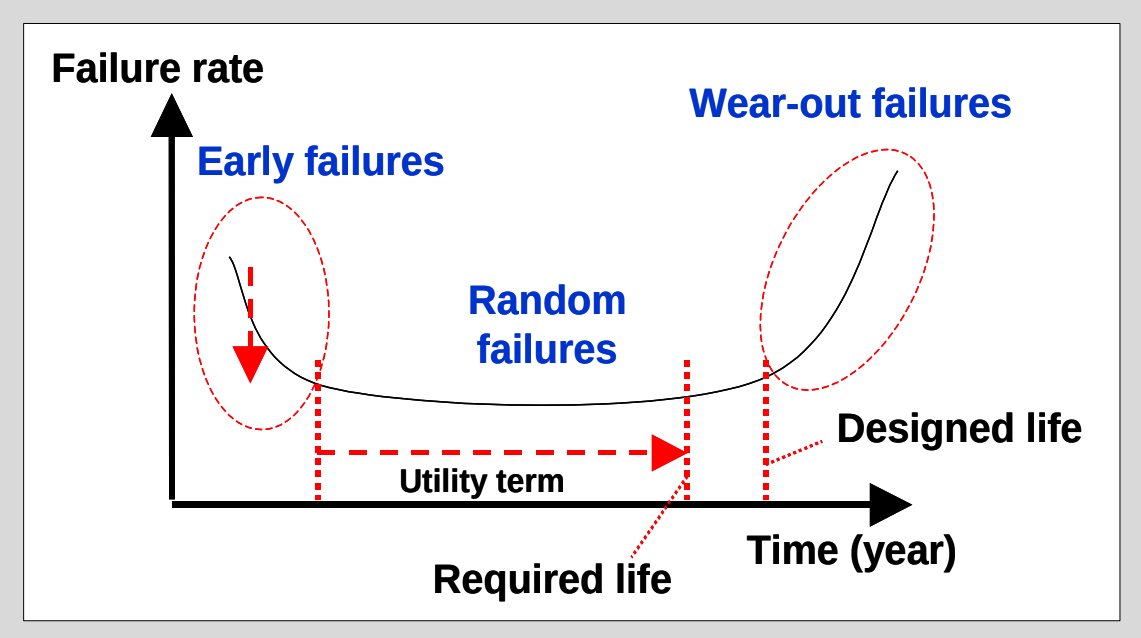


Fig. 11-1 Change in failure rate of semiconductor devices over time

Early failures in IGBT modules are caused by microscopic defects such as minute defects in IGBT/FWD, cracking in DCB, wire contact, and human error, etc.

Such defects and errors can be reduced by continuing the quality improvement using various design methods in IGBT/FWD chip design, module structure design, chip manufacturing process design, and assembly process design. However, it is very difficult to completely eliminate these at the design state, thus screening test (outgoing test) is required.

Fuji Electric is working to reduce the early failure rate by applying screening tests.

The failure rate in the random failures period of the failure rate curve settles down to a constant level because early failures products are removed. Duration of this random failures period varies depending on the operating conditions and environment of the entire system, which is composed of IGBT modules and other components, and corresponds to the system specific reliability. Random failures that occur during this period are generally caused by excessive stress exceeding the product maximum ratings being applied, such as overvoltage (between G-E, between C-E), overcurrent, and overheating.

In order to reduce the failure rate in the random failures period, it is necessary to design and confirm that various characteristics do not exceed the maximum ratings under the worst operating conditions of the system. Therefore, it is recommended to derate the operating conditions such as operating voltage and current from the maximum ratings described in the specifications.

The failures during wear-out failures period of the failure rate curve are due to the product lifetime, and caused by wear and fatigue. Therefore, in order to ensure the long-term reliability of IGBT modules, it is necessary to design that the product reaches the end of its lifetime before the wear-out failures period.

Fuji Electric verifies the long-term reliability test shown in the next section onwards during the design stage. In particular, the power cycling lifetime is verified using two models, the ΔT_{vj} power cycling (ΔT_{vj}-P/C) and the ΔT_C power cycling (ΔT_C-P/C) as shown in section 3 of this Chapter. When designing the lifetime of IGBT module, consider and design within this power cycling lifetime.

Also, the product lifetime varies greatly depending on the environment and operating conditions, thus it is necessary to take this into consideration when designing.

2. Reliability Test Conditions

In order to ensure long-term reliability, Fuji Electric conducts various reliability tests for design verification. Table 11-1 and Table 11-2 show the representative reliability tests for the 7th generation IGBT modules, X series. Refer to the product specification for details.

Table 11-1 Reliability tests of X series (environment tests)

Test categories		Test items	Test methods and conditions	Reference norms JEITA ED-4701 (Aug.-2013 edition)	Number of sample	Acceptance number
Environment Tests	1	High Temperature Storage	Storage temp. : 125±5°C Test duration : 1000hr.	Test Method 201A	5	(0:1)
	2	Low Temperature Storage	Storage temp. : -40±5°C Test duration : 1000hr.	Test Method 202A	5	(0:1)
	3	Temperature Humidity Storage	Storage temp. : 85±2°C Relative humidity : 85±2% Test duration : 1000hr.	Test Method 103A Test code C	5	(0:1)
	4	Temperature Cycle	Test temp. : High temp. 125+15/-0°C Low temp. -40+0/-10°C Minimum soak time : 15 min. Number of cycles : 100cyc	Test Method 105A	5	(0:1)
	5	Thermal Shock	Test temp. : High temp.100+10/-2°C Low temp. 0+2/-10°C Used liquid : Water with ice and boiling water Dipping time : 5min. per each temp. Transfer time : 10sec. Number of cycles : 10cycles	Test Method 307B Condition code B	5	(0:1)

Table 11-2 Reliability tests condition of X series (endurance tests)

Test categories		Test items	Test methods and conditions		Reference norms JEITA ED-4701 (Aug.-2013 edition)	Number of sample	Acceptance number
Endurance Tests	1	High Temperature Reverse Bias (IGBT/FWD chip)	Test temp. Bias voltage Bias method Test duration	: T_{vj} = 175±5°C : V_{CE} = 0.8 x V_{CES} : Applied DC voltage to C-E V_{GE} = 0V : 1000hr.	Test Method 101A	5	(0:1)
	2	High Temperature Bias (for Gate)	Test temp. Bias voltage Bias method Test duration	: T_{vj} = 175±5°C : V_{GE} = +20V or -20V : Applied DC voltage to G-E V_{CE} = 0V : 1000hr.	Test Method 101A	5	(0:1)
	3	Temperature Humidity Bias (IGBT/FWD chip)	Test temp. Relative humidity Bias voltage Bias method Test duration	: 85±2°C : 85±5% : V_{CE} = 0.8 x V_{CES} : Applied DC voltage to C-E V_{GE} = 0V : 1000hr.	Test Method 102A Condition code C	5	(0:1)
	4	Intermitted Operating Life (Power Cycle) (for IGBT)	ON time OFF time Test Temp. Number of cycles	: 2 sec. : 18 sec. : ΔT_{vj} = 100±5 deg. T_{vj} ≤ 175°C, T_S = 75±5°C : 60000 cycles.	Test Method 602	5	(0:1)

3. Power Cycling Lifetime

The temperature of IGBT module rises and falls according to the operating conditions. As the temperature fluctuates, the internal structure of the IGBT module is exposed to thermal stress, causing fatigue and deterioration. This fatigue and deterioration is greatly dependent on the temperature fluctuation range, thus the lifetime of the IGBT module varies depending on the operating and environmental conditions. This thermal stress lifetime is called power cycling lifetime (power cycling capability). The power cycling lifetime can be calculated from the power cycling lifetime curve that shows the relationship between the temperature change ΔT and the number of repeated cycles. There are two types of curves.

One is the ΔT_{vj}-P/C lifetime curve, which is related to the chip junction temperature fluctuation. In this case, the dominant failure modes are failure due to the deterioration of the aluminum wire joints on the chip surface, and deterioration of the solder joints directly under the chip.

The other is the ΔT_C-P/C lifetime curve, which is related to the case temperature (mainly the copper baseplate temperature) fluctuation due to the junction temperature fluctuation. In this case, the dominant failure mode is failure due to deterioration of the solder joints between the DCB insulating substrate and the copper baseplate.

The following sections describe the measurement method and the power cycling lifetime curves for ΔT_{vj}-P/C and ΔT_C-P/C.

3.1 ΔT_{vj}-P/C lifetime curve

Fig. 11-2 shows the current pattern of the ΔT_{vj}-P/C test. Fig. 11-3 and Fig. 11-4 show the equivalent test circuit diagram and the schematic diagram of the T_C and T_f measurement positions, respectively. During the ΔT_{vj}-PC test, T_{vj} is rapidly increased and decreased in a relatively short cycle. Therefore, thermal stress occurs between the power chip and the DCB, and between the power chip and the aluminum wire due to the temperature difference. For this reason, the ΔT_{vj}-PC mainly indicates the lifetime of the aluminum wire joints on the chip surface, and the solder joints directly under the chip.

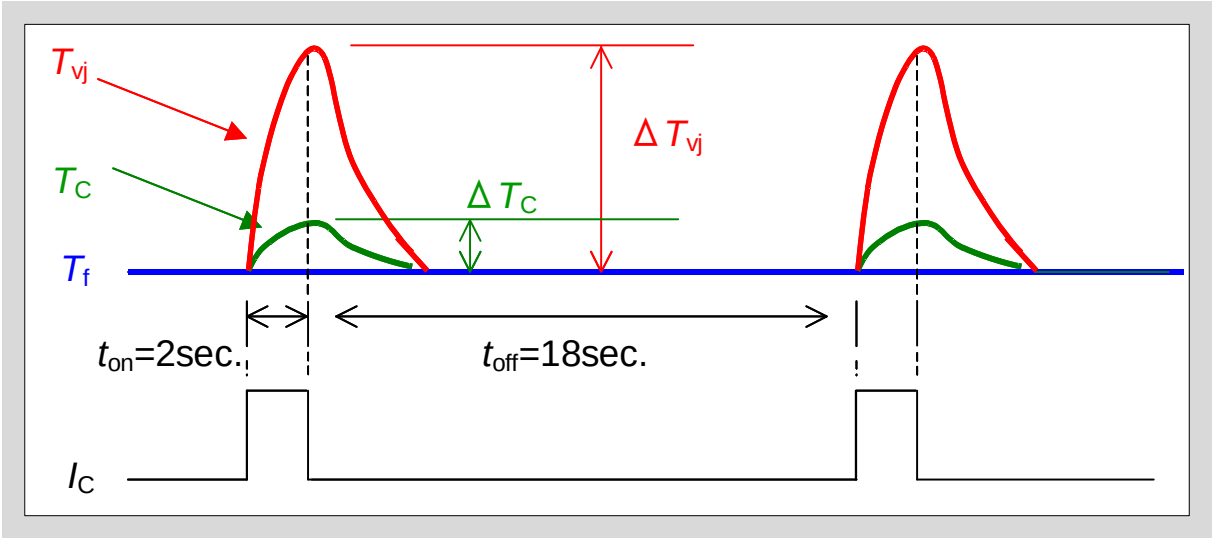


Fig. 11-2 ΔT_{vj}-P/C test current pattern and temperature changes

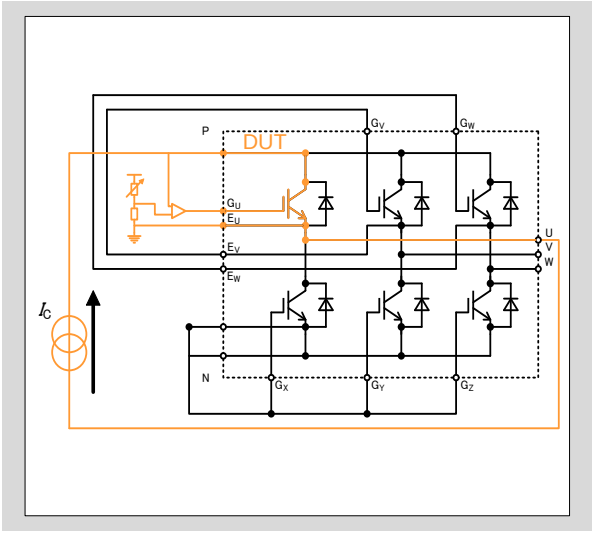


Fig. 11-3 Equivalent test circuit for ΔT_{vj}-PC test

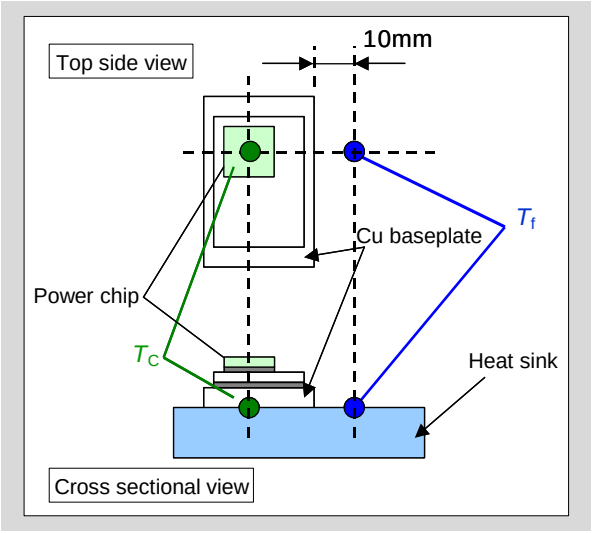


Fig. 11-4 T_C and T_f measurement positions

As example, Fig. 11-5 shows the ΔT_{vj}-PC lifetime curves of U series and V series. In this figure, the $T_{vj(min)}$=25˚ C line indicates the lifetime when the chip junction temperature is changed while the temperature of the heat sink is kept at 25˚ C. For example, when ΔT_{vj} = 50˚ C, the chip junction temperature reaches 75˚ C while the heat sink temperature is 25˚ C. On the other hand, the $T_{vj(max)}$ =150˚ C line shows the lifetime when the heat sink temperature is changed while the chip junction temperature is kept at 150˚ C. For example, when ΔT_{vj} = 50˚ C, the chip junction temperature reaches 150˚ C while the heat sink temperature is 100˚ C. Thus, even if ΔT_{vj} is the same, the higher the heat sink temperature and the chip junction temperature, the shorter the lifetime.

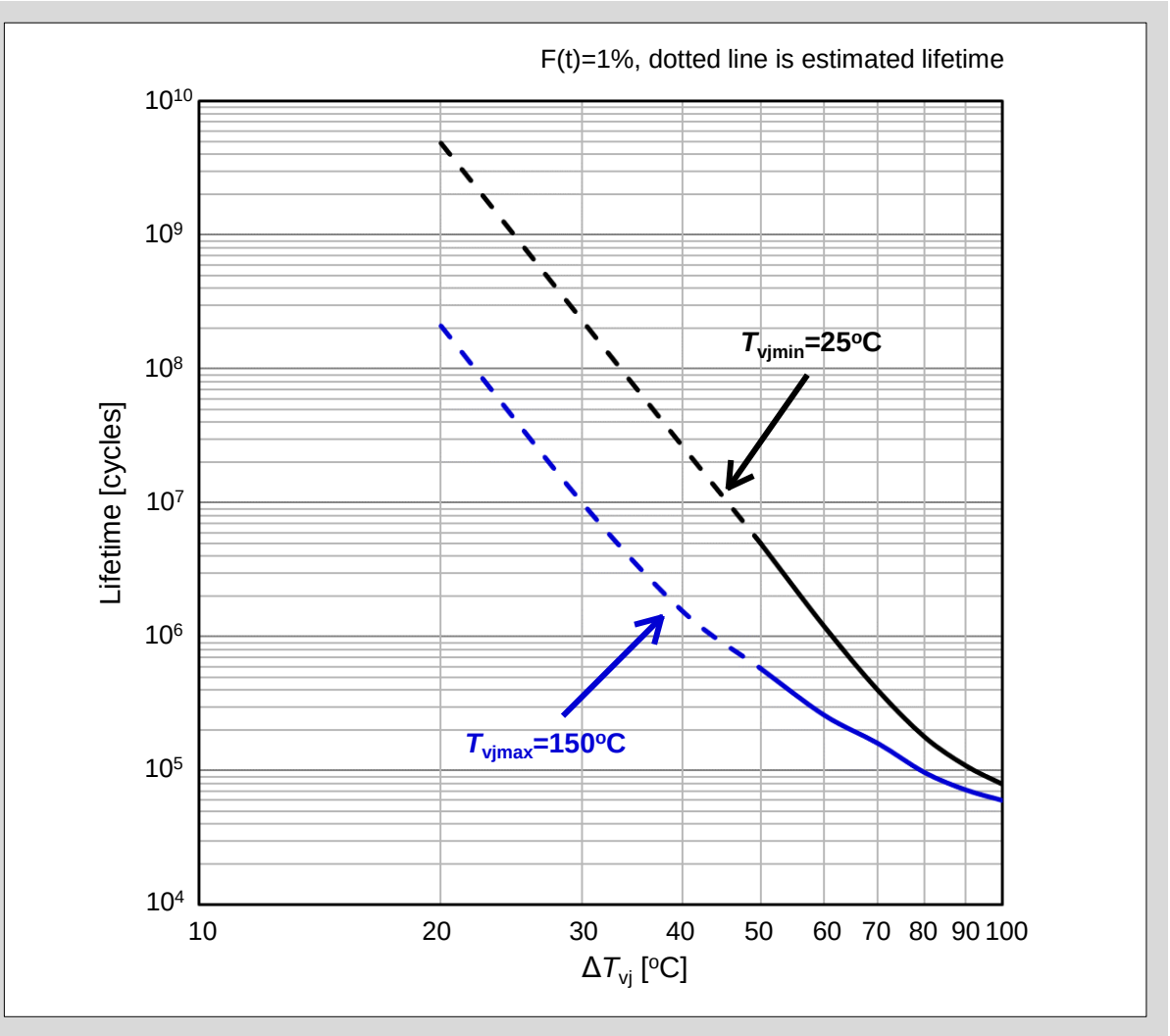


Fig. 11-5 Example of ΔT_{vj}-P/C lifetime curve

3.2 ΔT_{vj}-P/C lifetime in actual equipment

For example, in the equipment shown in Fig. 11-6 where the motor accelerates/decelerates, starts/stops frequently, calculate the ΔT_{vj}-PC lifetime with ΔT_{vj} as the difference between the maximum junction temperature T_{vj} and the heat sink temperature T_f (see Fig. 11-2), and confirm that the lifetime is sufficiently longer than the target lifetime of the equipment. Do not calculate the ΔT_{vj}-PC lifetime under such operating conditions from ΔT_{vj} during steady-state operation. The ΔT_{vj} during acceleration, deceleration, starting and stopping are greater than during steady-state operation, and the lifetime is determined by this ΔT_{vj}. In addition, in an inverter system with low speed operation such as 0.5Hz, note that the ΔT_{vj} changes significantly, thus it is necessary to calculate the lifetime with ΔT_{vj} at this condition.

If there are multiple acceleration, deceleration or low speed operation within one operation cycle of the equipment, refer to the calculation method described later in section 3.4, “P/C lifetime when there are multiple temperature rise peaks in one operation cycle”.

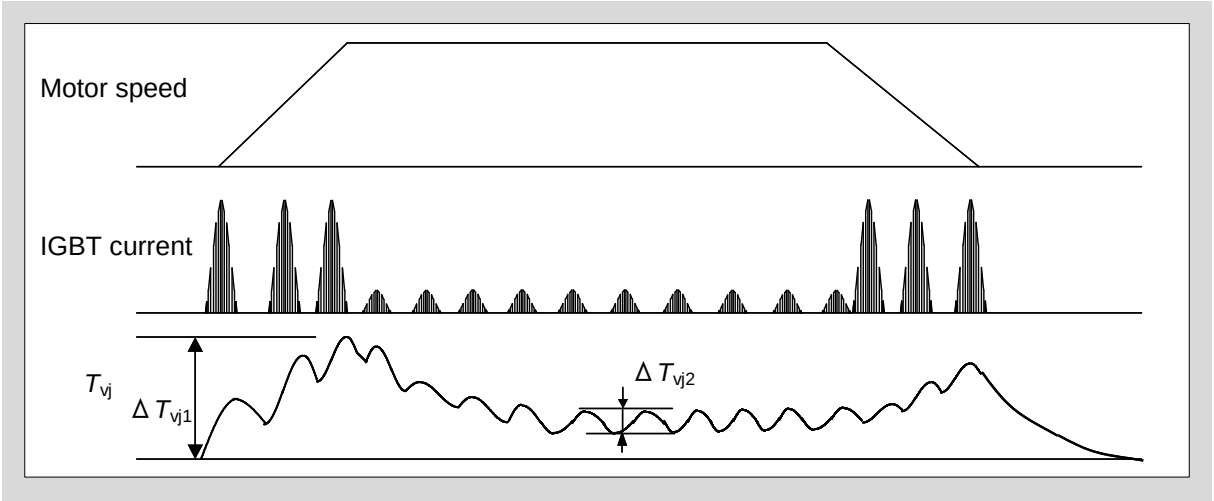


Fig. 11-6 Operation in actual equipment (example)

3.3 ΔT_C-P/C lifetime curve

Fig. 11-7 shows the current pattern of the ΔT_C-P/C test.

Fig. 11-8 shows the equivalent test circuit diagram for ΔT_C-PC test of a 6-Pack module. During the test, all the phases are energized, and the temperature of the entire case (copper base) rises and falls. The case temperature T_C is raised and lowered in a relatively long cycle so that the temperature difference between T_{vj} and T_C becomes small. This is different from the conditions in the ΔT_{vj}-PC test. When such temperature change occurs, large stress strain becomes predominant between the copper base and the DCB insulating substrate. Thus, the ΔT_C-PC mainly indicates the lifetime of the solder joints under the DCB insulating substrate.

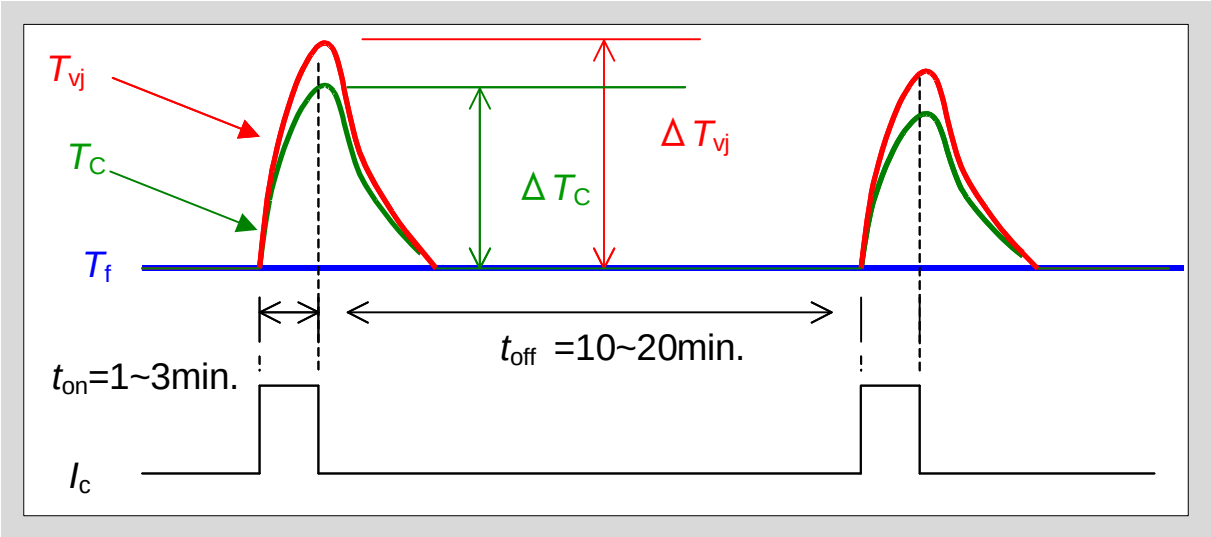


Fig. 11-7 ΔT_C-P/C test current pattern and temperature changes

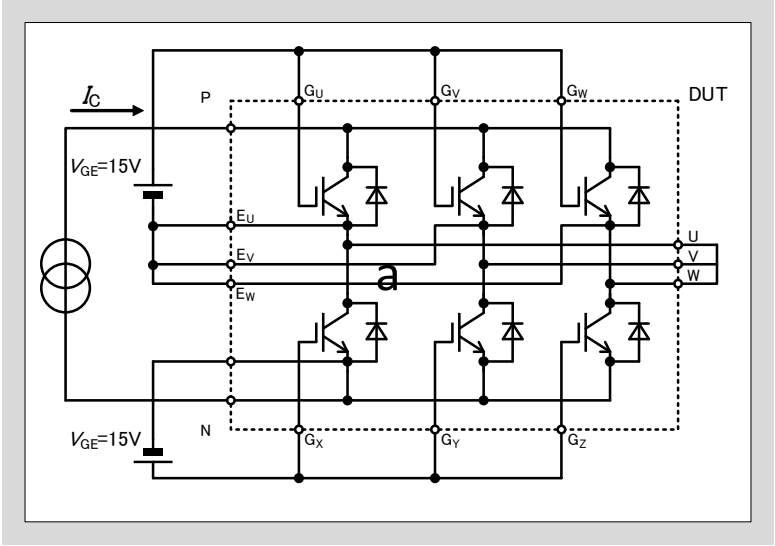
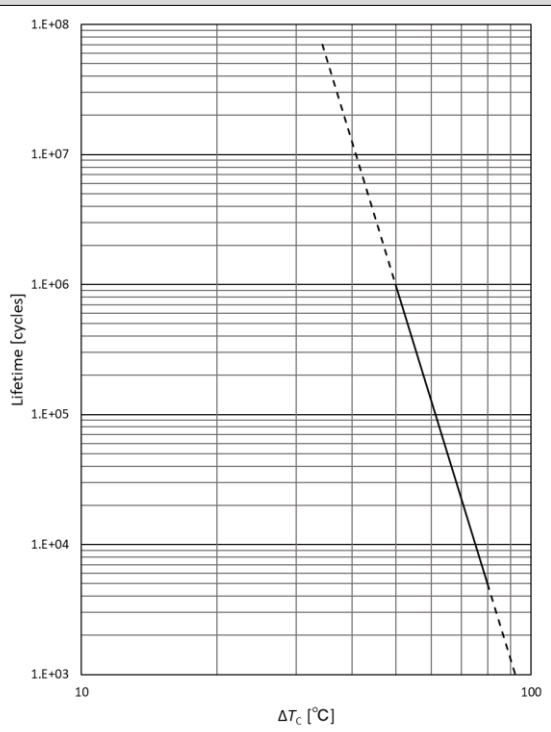


Fig. 11-8 Equivalent test circuit for ΔT_C-P/C test

The failure mode of ΔT_C-PC can be explained as follows. When T_C is raised and lowered, the largest stress strain occurs at the solder joints between the copper base and the DCB insulating substrate due to the difference in thermal expansion coefficient between them. Repeated temperature changes cause cracks in the solder joints due to stress strain. When the crack progresses and reaches the bottom part of the DCB insulating substrate where the chips are mounted, the heat dissipation of the chips deteriorate (thermal resistance R_{th} increases). As a result, T_{vj} rises and may exceed T_{vjmax}, leading to thermal destruction.

Fig. 11-9 shows the ΔT_C-PC lifetime curve of an IGBT module. When the temperature difference between T_{vj} and T_C is small, and T_C rises and falls frequently, make sure that the ΔT_C-PC lifetime of the module is sufficiently longer than the target lifetime of the equipment.



1. The failure criteria is when the thermal resistance becomes 1.2 times of more of the initial value.
2. The heat sink used in the test and the mounting condition for the modules is based on Fuji's standards.
3. The lifetime curve shows the data at F(t)=20% of the accumulated failure rate by Weibull analysis.
4. The lifetime curve shows the test result of multiple types modules.
5. The dashed line shows the estimated lifetime.

(DCB insulating substrate: Al2O3
Solder under DCB: Sn-based lead-free solder)

Fig. 11-9 Example of ΔT_C-PC lifetime

3.4 P/C lifetime when there are multiple temperature rise peaks in one operation cycle

The P/C lifetime of the IGBT module depends on the temperature rise peak and the maximum junction temperature. Therefore, when there is only one temperature rise peak in one operation cycle, the number of cycles calculated from the P/C lifetime curve is the lifetime of the IGBT module. However, when there are multiple temperature rise peaks in one operation cycle, the lifetime becomes shorter due to the impact of multiple temperature rises.

The calculation method of P/C lifetime when there are multiple different temperature rise peaks is shown below. When there are n times of temperature rises in one operation cycle, the combined P/C lifetime can be expressed by the following formula, where P/C(k) is the P/C lifetime for the k-th (k=1, 2, 3, …., n) temperature rise.

$$P/C = 1\Big/\left(\sum_{k=1}^{n}\frac{1}{P/C(k)}\right)$$

For example, when n=4 and the P/C lifetime for the respective temperature rise are 3.8 x 10^6, 1.2 x 10^6, 7.6 x 10^5 and 4.6 x 10^5, the combined P/C lifetime can be calculated as follows.

$$P/C = 1\Big/\left(\frac{1}{3.8\times10^6}+\frac{1}{1.2\times10^6}+\frac{1}{7.6\times10^5}+\frac{1}{4.6\times10^5}\right) = 2.2\times10^5$$

The P/C lifetime can be obtained from the product of the P/C lifetime calculated in this way and one operation cycle (time). For example, when one operation cycle is 1800 seconds (30 minutes), the lifetime is calculated as follows.

$$2.2\times10^5\times1800/(60\times60\times24\times365) = 12.55 \fallingdotseq 12\ years\ and\ 6\ months$$