Chapter 3

Detail of Signal Input/Output Terminals

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1. Control Power Supply Terminals V_{CCH},V_{CCL},COM

1. Voltage Range of control power supply terminals V_{CCH}, V_{CCL}

Please connect a single 15Vdc power supply between V_{CCH},V_{CCL} and COM terminals for the IPM control power supply. The voltage should be regulated to 15V ±10% for proper operation. Table 3-1 describes the behavior of the IPM for various control supply voltages. A low impedance capacitor and a high frequency decoupling capacitor should be connected close to the terminals of the power supply.

High frequency noise on the power supply might cause a malfunction of the internal control IC or erroneous fault signal output. To avoid these problems, the maximum amplitude of voltage ripple on the power supply should be less than ±1V/μs.

The potential at the COM terminal is different from that at the N(*)*1 power terminal. It is very important that all control circuits and power supplies are referred to the COM terminal and not to the N(*)*1 terminals. If circuits are improperly connected, an additional current might flow through the sense resistor and it cause an improper operation of the short-circuit protection function. In general, it is best practice to make the COM as the ground in the PCB layout.

The main control power supply is also connected to the bootstrap circuit which provide a power to floating supplies for the high side gate drivers.

When high side control supply voltage (V_{CCH} and COM) falls down under V_{CCH} UV (Under Voltage protection) level, only the IGBT which occurred the under voltage condition becomes off-state even though the input signal is ON condition.

When low side control supply voltage (V_{CCL} and COM) falls down under V_{CCL} UV level, all lower side IGBTs become off-state even though the input signal is ON condition.

Table 3-1 Functions versus supply voltage V_{CCH}, V_{CCL}

Control Voltage Range [V]	Function Operations
0 ~ 4	The IPM doesn't work. UV and fault output are not activated. dV/dt noise on the main P-N supply might cause a malfunction of the IGBTs.
4 ~ 13	The IPM start to work. UV is activated, control input signals are blocked and a fault output VFO is generated.
13 ~ 13.5	UV is reset. IGBTs are operated in accordance with the control gate input. Driving voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition and high side IGBTs can't operate after VB(*)*2 initial charging because VB(*) can't reach to $V_{B(ON)}$.
13.5 ~ 16.5	Normal operation. This is the recommended operating condition.
16.5 ~ 20	The lower side IGBTs are still operated. Because driving voltage is above the recommended range, IGBT's switching is faster. It causes increasing system noise. And peak short circuit current might be too large for proper operation of the short circuit protection.
Over 20	Control circuit in this IPM might be damaged. If necessary, it is recommended to insert a zener-diode between each pair of control supply terminals.

*1 N(*) : N(U), N(V), N(W)

*2 VB(*) : VB(U)-U, VB(V)-V,VB(W)-W

2. Under Voltage protection of control power supply terminals V_{CCH}, V_{CCL}

Fig.3-1 shows the UV protection circuit of high side and low side control supply(V_{CCH},V_{CCL}). Fig.3-2 and Fig.3-3 shows the sequence of UV operation of V_{CCH} and V_{CCL}.

As shown in Fig.3-1, a diode is electrically connected to the V_{CCH}, V_{CCL} and COM terminals. The diode should not be used for a voltage clamp intentionally otherwise the IPM might be damaged.

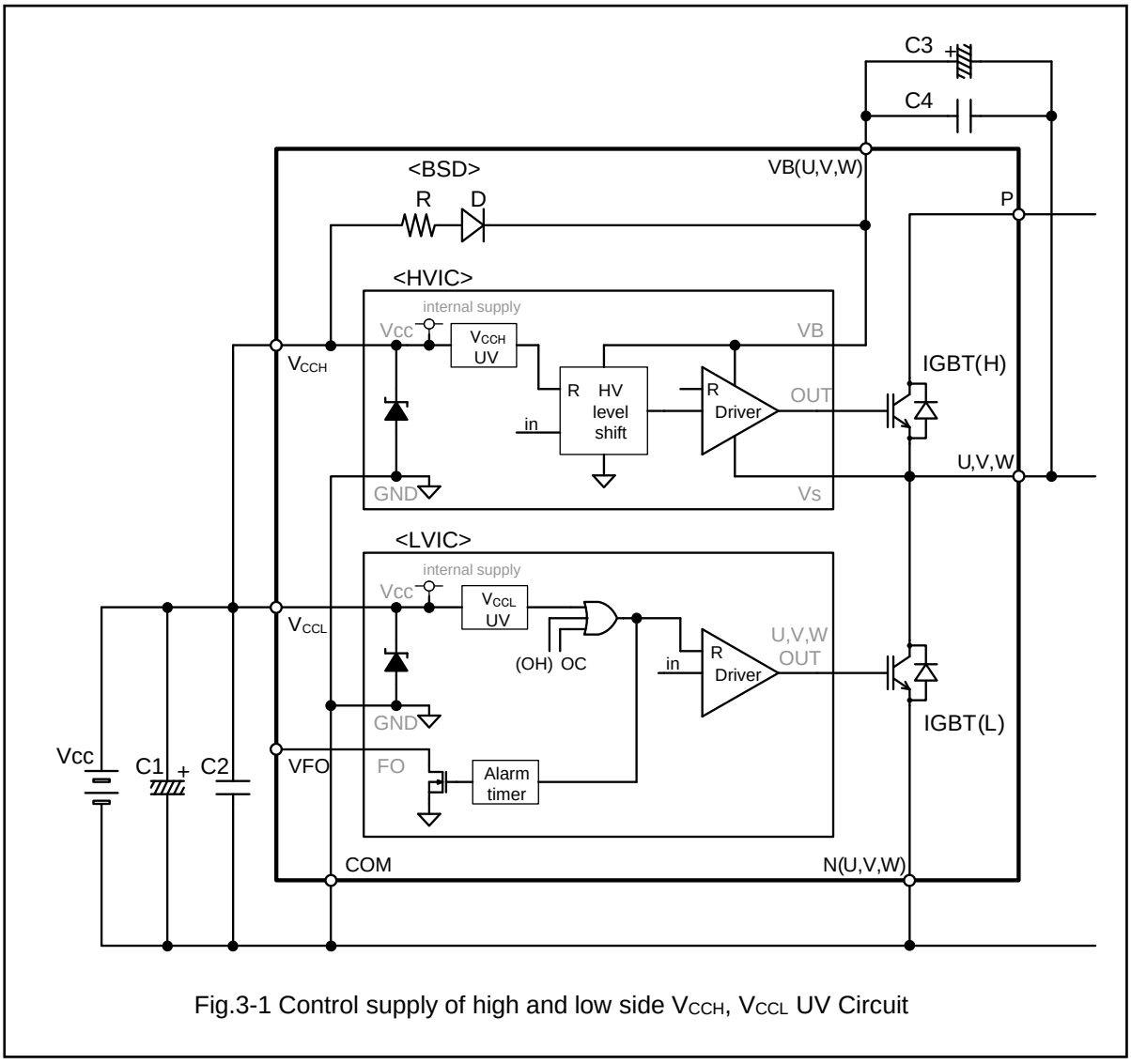

Fig.3-1 Control supply of high and low side V_{CCH}, V_{CCL} UV Circuit

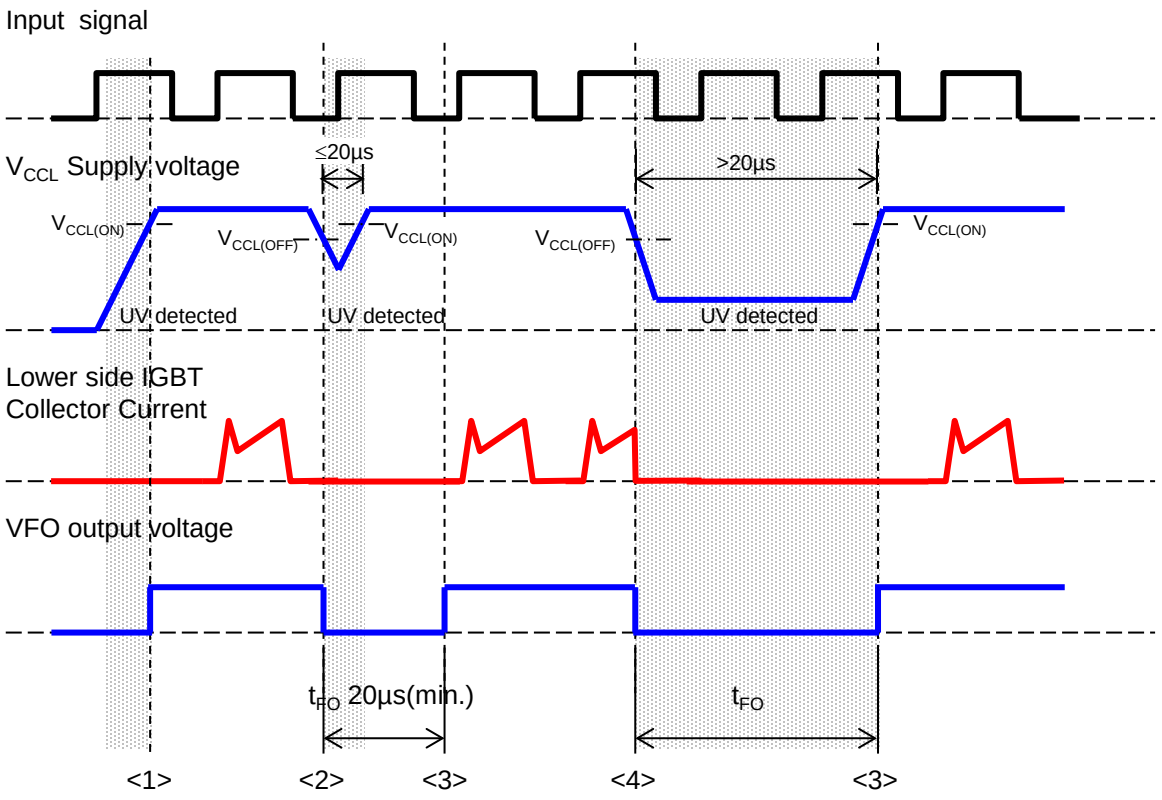

Fig.3-2 Operation sequence of V_{CCL} Under Voltage protection (lower side arm)

<1> When V_{CCL} is lower than $V_{CCL(ON)}$, all lower side IGBTs are OFF state.
After V_{CCL} exceeding $V_{CCL(ON)}$, the fault output VFO is released (high level).
And the LVIC starts to operate, then next input is activated.

<2> The fault output VFO is activated when V_{CCL} falls below $V_{CCL(OFF)}$, and all lower side IGBT remains OFF state.
If the voltage drop time is less than 20µs, the minimum pulse width of the fault output signal is 20µs and all lower side IGBTs are OFF state regardless of the input signal condition.

<3> UV is reset after t_{FO} and V_{CCL} exceeding $V_{CCL(ON)}$, then the fault output VFO is reset simultaneously.
After that the LVIC starts to operate from the next input signal.

<4> When the voltage drop time is more than t_{FO}, the fault output pulse width is generated and all lower side IGBTs are OFF state regardless of the input signal condition during the same time.

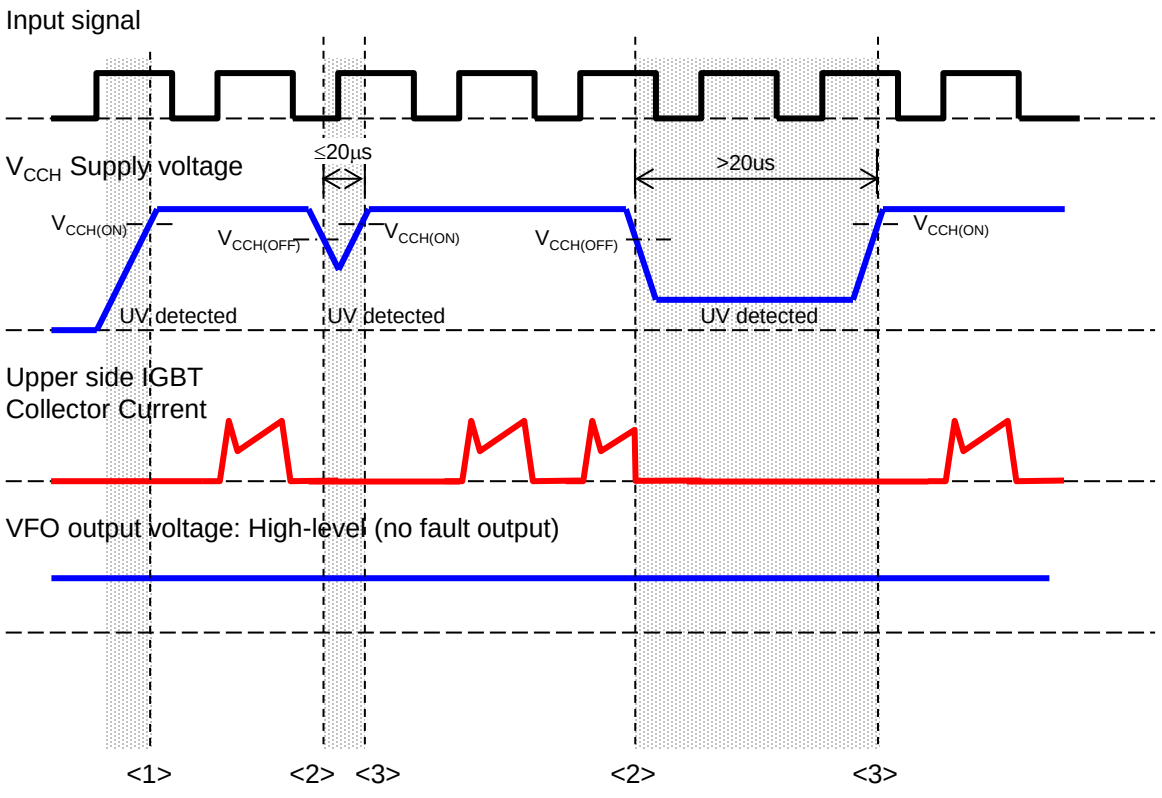

Fig.3-3 Operation sequence of V_{CCH} Under Voltage protection (upper side arm)

<1> When V_{CCH} is lower than $V_{CCH(ON)}$, the upper side IGBT is OFF state.
After V_{CCH} exceeds $V_{CCH(ON)}$, the HVIC starts to operate from the next input signals.
The fault output VFO is constant (high level) regardless V_{CCH}.

<2> After V_{CCH} falls below $V_{CCH(OFF)}$, the upper side IGBT remains OFF state.
But the fault output VFO keeps high level.

<3> The HVIC starts to operate from the next input signal after UV is reset.

2. Power Supply Terminals of High Side VB(U,V,W)

1. Voltage Range of high side bias voltage for IGBT driving terminals VB(U,V,W)

The VB(*) voltage, which is the voltage difference between VB(U,V,W) and U,V,W, provides the supply to the HVICs within the IPM. This supply must be in the range of 13.0~18.5V to ensure that the HVICs can fully drive the upper side IGBTs. The IPM includes UV function for the VB(*) to ensure that the HVICs do not drive the upper side IGBTs, if the VB(*) voltage drops below a specified voltage (refer to the datasheet). This function prevents the IGBT from operating in a high dissipation mode. Please note here, that the UV (under voltage protection) function of any high side section acts only on the triggered channel without any feedback to the control level.

In case of using bootstrap circuit, the IGBT drive power supply for upper side arms can be composed of one common power supply with a lower side arm. In the conventional IPM, three independent insulated power supplies were necessary for IGBT drive circuit of upper side arm.

The power supply of the upper side arm is charged when the lower side IGBT is turned on or freewheel current flows the lower side IGBT. Table 3-2 describes the behavior of the IPM for various control supply voltages. The control supply should be well filtered with a low impedance capacitor and a high frequency decoupling capacitor connected close to the terminals in order to prevent a malfunction of the internal control IC caused by a high frequency noise on the power supply.

When control supply voltage (VB(U)-U,VB(V)-V and VB(W)-W) falls down under UV (Under Voltage protection) level, only triggered phase IGBT is off-state regardless the input signal condition.

Table 3-2 Functions versus high side bias voltage for IGBT driving VB(*)

Control Voltage Range [V]	The IPM function operations
0 ~ 4	HVICs are not activated. UV does not operate. dV/dt noise on the main P-N supply might trigger the IGBTs.
4 ~ 12.5	HVICs start to operate. As the UV is activated, control input signals are blocked.
12.5 ~ 13	UV is reset. The upper side IGBTs are operated in accordance with the control gate input. Driving voltage is below the recommended range, so $V_{CE(sat)}$ and the switching loss will be larger than that under normal condition.
13 ~ 18.5	Normal operation. This is the recommended operating condition.
18.5 ~ 20	The upper side IGBTs are still operated. Because driving voltage is above the recommended rage, IGBT's switching is faster. It causes increasing system noise. And peak short circuit current might be too large for proper operation of the short circuit protection.
Over 20	Control circuit in the IPM might be damaged. It is recommended to insert a zener-diode between each pair of high side power supply terminals.

2. Under Voltage protection of high side power supply terminals VB(U,V,W)

Fig.3-4 shows of high side (VB(U)-U,VB(V)-V and VB(W)-W) UV (Under Voltage protection) circuit block of the control power supply.
Fig.3-5 shows operation sequence of VB(U)-U,VB(V)-V,VB(W)-W Under Voltage operation.

As shown in Fig.3-4, diodes are electrically connected to the VB(U,V,W), U,V,W and COM terminals. These diodes protect the IPM from an input surge voltage. Don't use these diodes for a voltage clamp because the IPM might be destroyed if the diodes are used as a voltage clamp.

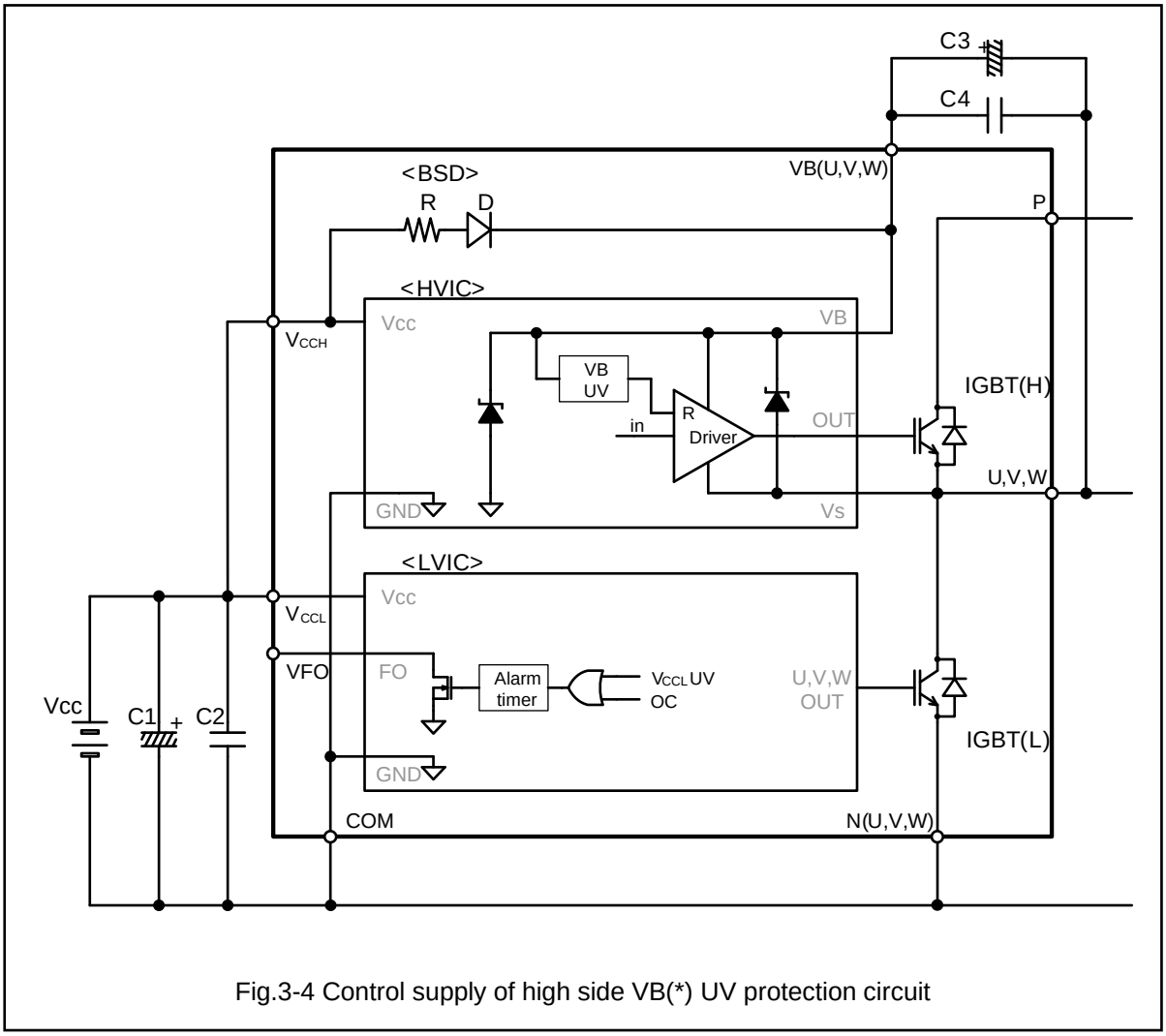

Fig.3-4 Control supply of high side VB(*) UV protection circuit

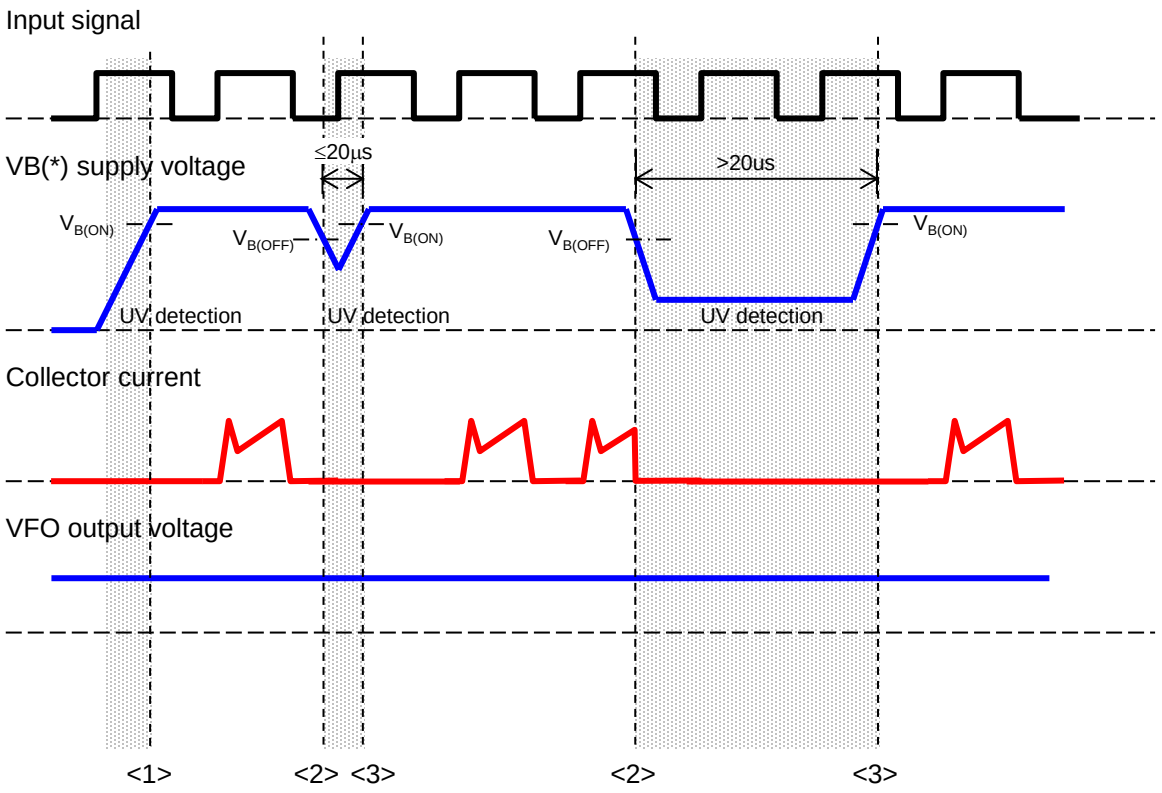

Fig.3-5 Operation sequence of VB(*)*1 Under voltage protection (upper side arm)

<1> When VB(*) is under $V_{B(ON)}$, the upper side IGBT is OFF state.
After VB(*) exceeds $V_{B(ON)}$, the HVIC starts to operate from the next input signal.
The fault output VFO is constant (high level) regardless VB(*).

<2> After VB(*) falls below $V_{B(OFF)}$, the upper side IGBT remains OFF state.
But the fault output VFO keeps high level.

<3> The HVIC starts to operate from the next input signal after UV is reset.

*1 VB(*) : VB(U)-U,VB(V)-V,VB(W)-W

3. Function of Internal BSDs (bootstrap Diodes)

There are several ways in which the VB(*)*1 floating supply can be generated. Bootstrap method is described here. The boot strap method is a simple and cheap solution. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. As show in the Fig. 3-6, Fig. 3-8 and Fig. 3-11, the boot strap circuit consists of bootstrap diode and resistor whish are integrated in the IPM and an external capacitor.

1.Chargin and Discharging of Bootstrap Capacitor During Inverter Operation

a) Charging operation timing chart of bootstrap capacitor (C)

<Sequence (Fig.3-7) : lower side IGBT is turned on in Fig.3-6>

When lower side IGBT is ON state, the charging voltage on the bootstrap capacitance Vc(t1) is calculated by the following equations.

$VC(t1) = V_{CC}-V_F-V_{CE(sat)}-Ib\cdot R$ …… Transient state
$VC(t1) \approx V_{CC}$ …… Steady state

V_F : Forward voltage of Boost strap diode (D)
$V_{CE(sat)}$: Saturation voltage of lower side IGBT
R : Bootstrap resistance for inrush current limitation (R)
Ib : Charge current of bootstrap

When lower side IGBT is turned off, then the motor current flows through the free-wheel path of the upper side FWD. Once the electric potential of VS rises near to that of P terminal, the charging of C is stopped, and the voltage of C gradually declines due to a current consumed by the drive circuit.

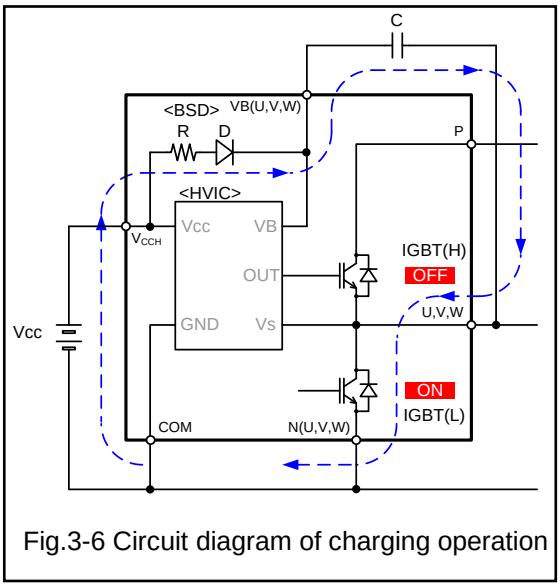

Fig.3-6 Circuit diagram of charging operation

*1 VB(*) : VB(U)-U,VB(V)-V,VB(W)-W

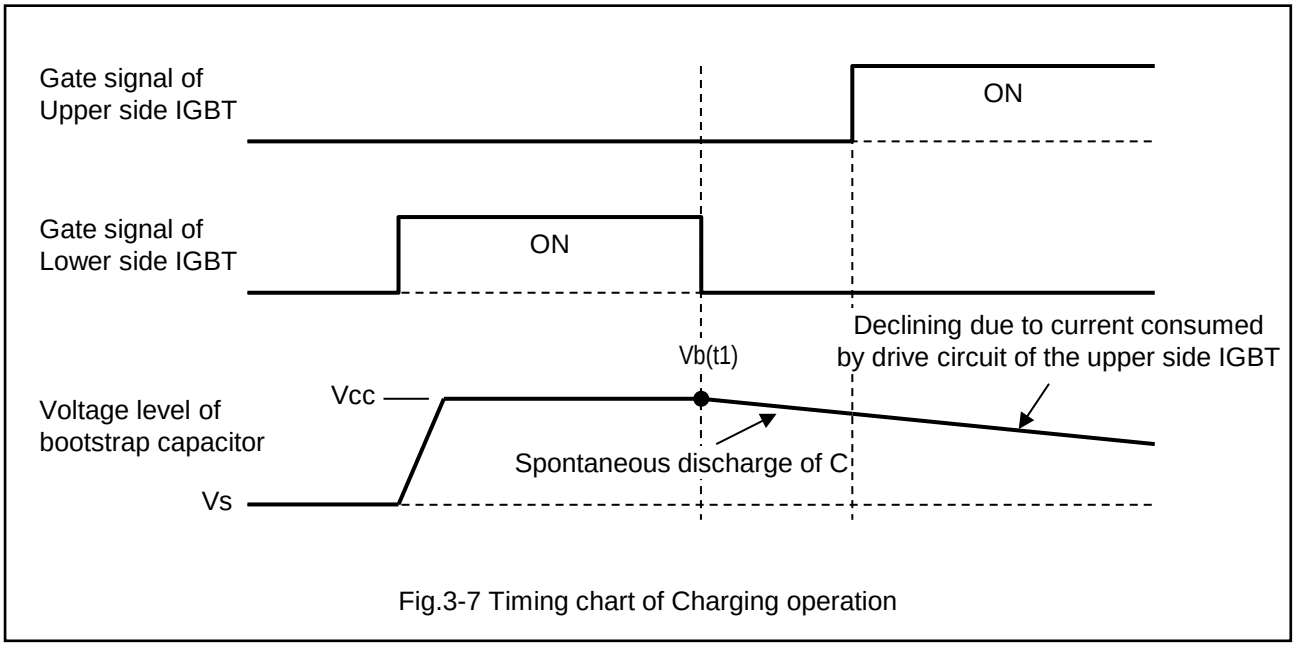

Fig.3-7 Timing chart of Charging operation

<Sequence (Fig.3-9): Lower side IGBT is OFF and Lower side FWD is ON (Freewheel current flows) in Fig.3-8 >

When the lower side IGBT is OFF and the lower side FWD is ON, a free wheeling current flows the lower side FWD. The voltage on the bootstrap capacitance Vc(t2) is calculated by the following equations:

$Vc(t2) = V_{CC}-V_F+V_{F(FWD)} - Ib \cdot R$ ……Transient state
$Vc(t2) \approx V_{CC}$ ……Steady state

V_F : Forward voltage of Boost strap diode (D)
$V_{F(FWD)}$: Forward voltage of lower side FWD

R : Bootstrap resistance for inrush current limitation (R)
Ib : Charge current of bootstrap

When both the lower side IGBT and the upper side IGBT are OFF, a regenerative current flows continuously through the freewheel path of the lower side FWD. Therefore the potential of V_S drops to $-V_F$, then the bootstrap capacitor is re-charged to restore the declined potential. When the upper side IGBT is turned ON and the potential of V_S exceeds Vcc, the charging of the bootstrap capacitor stops and the voltage on the bootstrap capacitor gradually declines due to consumption of the stored energy by the drive circuit.

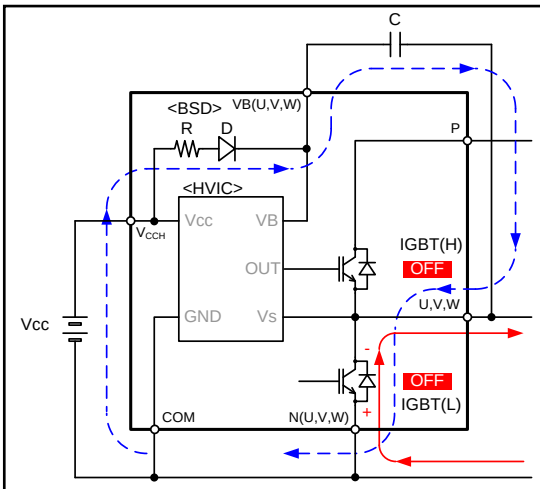

Fig.3-8 Circuit diagram of Charging operation under the lower side arm FWD is ON

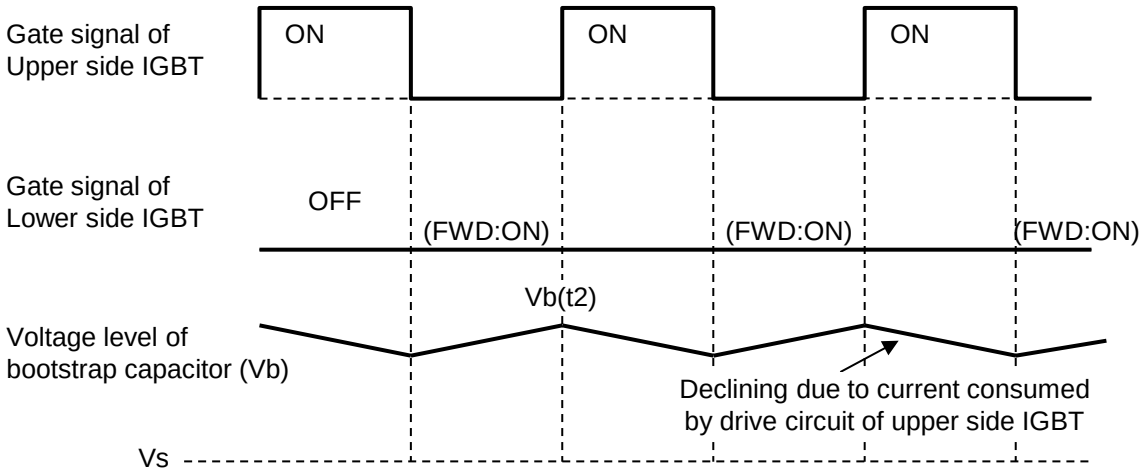

Fig.3-9 Timing chart of Charging operation under the lower side arm FWD is ON

2) Setting the bootstrap capacitance and minimum ON/OFF pulse width

The parameter of bootstrap capacitor can be calculated by the following equation:

$$C = Ib \cdot \frac{t1}{dV}$$

* t1 : the maximum ON pulse width of the upper side IGBT
* Ib : the drive current of the HVIC (depends on temperature and frequency characteristics)
* dV: the allowable discharge voltage. (see Fig.3-10)

A certain margin should be added to the calculated capacitance.
The bootstrap capacitance is generally selected as large as 2~3 times of the calculated value.

The recommended minimum ON pulse width (t2) of the lower side IGBT should be basically determined such that the time constant C·R will enable the discharged voltage (V) to be fully charged again during the ON period.
However, if only upper side IGBT has an ON-OFF-ON control mode (Sequence Fig.3-10), the time constant should be set so that the consumed energy during the ON period can be charged during the OFF period.

The minimum pulse width is decided by the minimum ON pulse width of the lower side IGBT or the minimum OFF pulse width of the upper side IGBT, whichever is shorter.

$$t_2 \geq \frac{R \cdot C \cdot dV}{Vcc - Vb_{(\min)}}$$

* R : Series resistance of Bootstrap diode ΔRF(BSD)
* C : Bootstrap capacitance
* dV: the allowable discharge voltage.
*V_{CC} : Voltage of HVICs and LVIC power supply (ex.15V)
*Vb(min) : the minimum voltage of the upper side IGBT drive (Added margin to UV. ex. 14V)

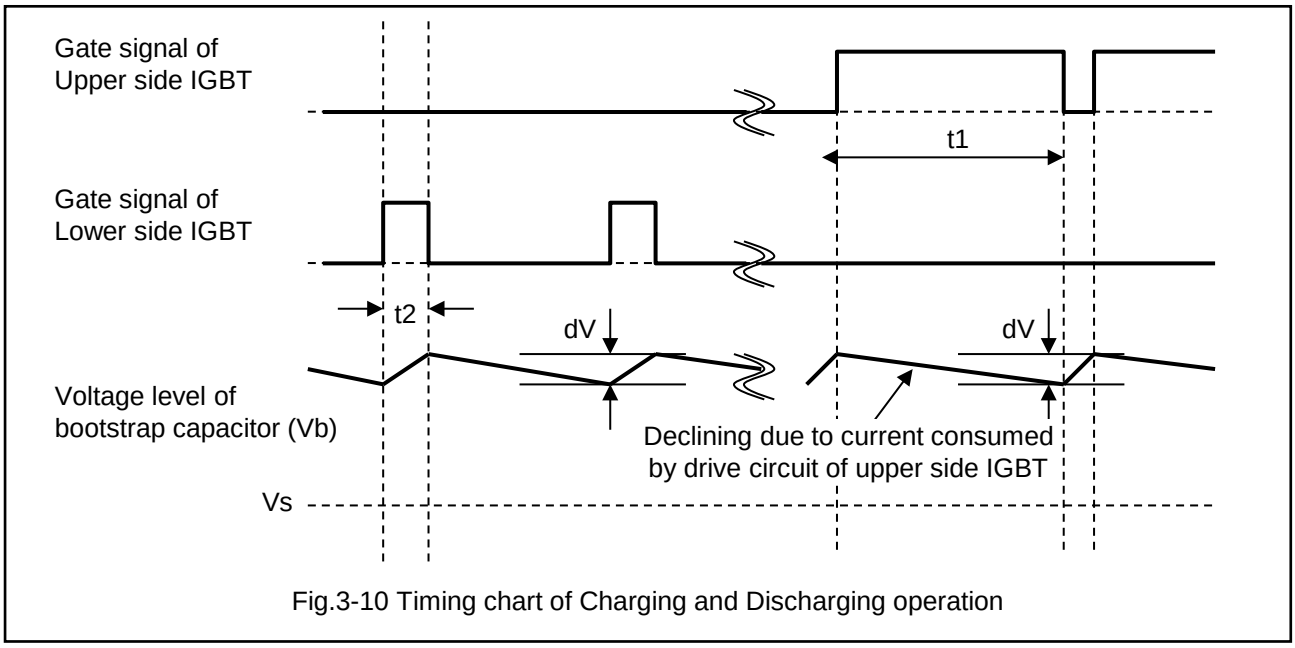

Fig.3-10 Timing chart of Charging and Discharging operation

3) Setting the bootstrap capacitance for Initial charging

The initial charge of the bootstrap capacitor is required to start-up the inverter.
The pulse width or pulse number should be large enough to make a full charge of the bootstrap capacitor.

For reference, the charging time of 10μF capacitor through the internal bootstrap diode is about 2ms.

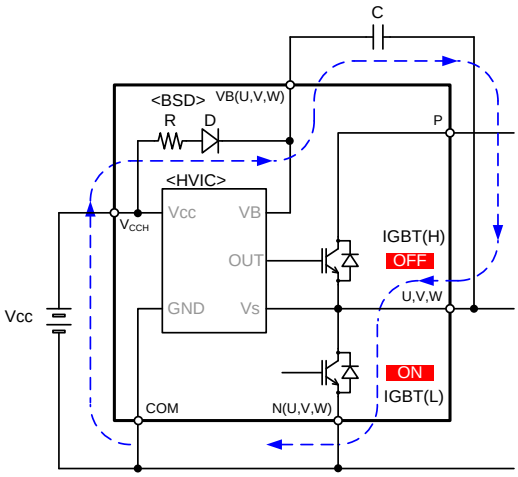

Fig.3-11 Circuit diagram of initial charging operation

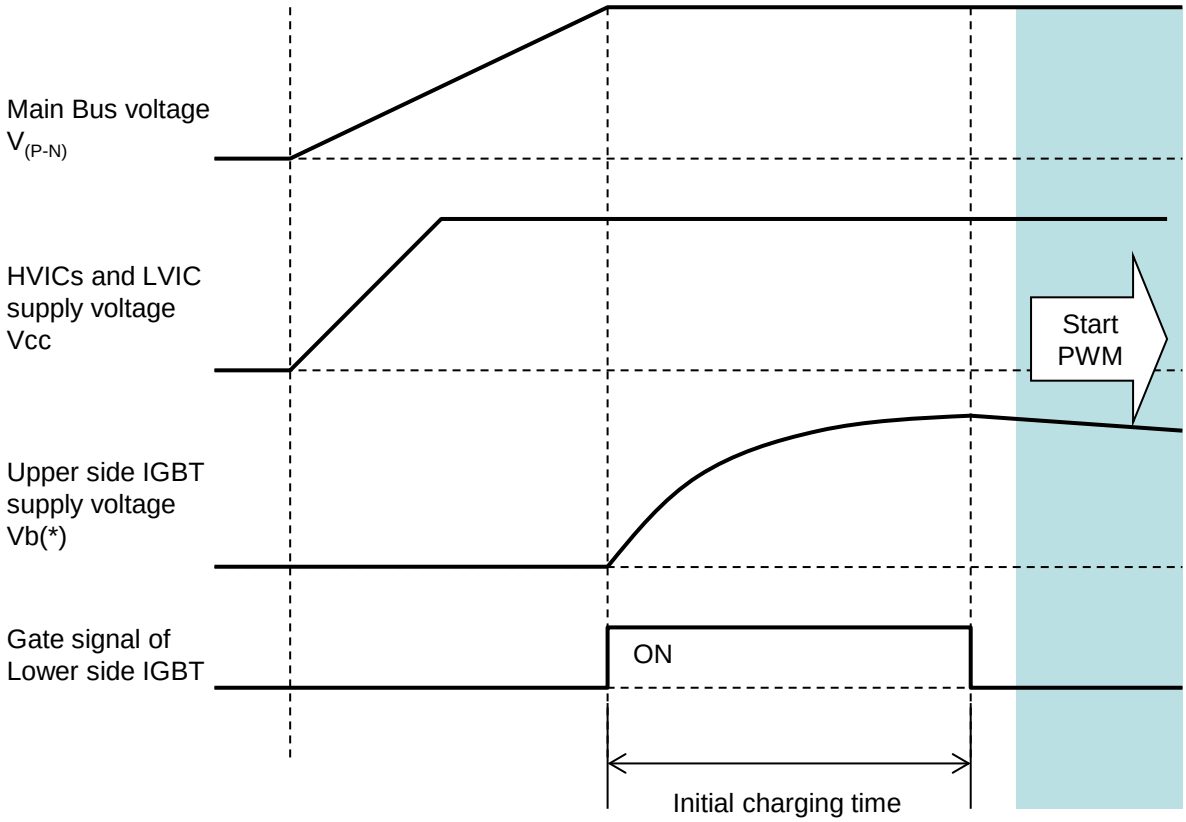

Fig.3-12 Timing chart of initial charging operation

4. Input Terminals IN(HU,HV,HW), IN(LU,LV,LW)

1. Input terminals Connection

Fig.3-13 shows the input interface circuit between the MPU and the IPM. It is possible that the input terminals connect directly to the MPU. It should not need the external pull up and down resistors connected to the input terminals, input logic is active high and the pull down resistors are built in.

The RC coupling at each input (parts shown dotted in Fig.3-13) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's PCB layout.

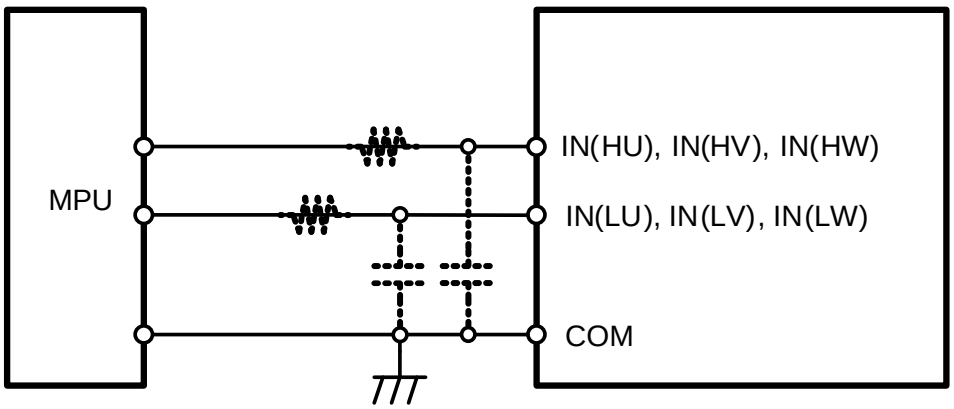

Fig.3-13 Recommended MPU I/O Interface Circuit of IN(HU,HV,HW), IN(LU,LV,LW) terminals

2. Input terminal circuit

The input logic of this IPM is active high. This logic has removed the sequence restriction between the control supply and the input signal during startup or shutdown operation. Therefore it makes the system failsafe. In addition, the pull down resistors are built in to each input terminals in Fig.3-14. Thus, external pull-down resistors are not needed reducing the required external component. Furthermore, a direct connection to 3.3V-class MPU by the low input signal threshold voltage.

As shown in Fig.3-14, the input circuit integrates a pull-down resistor. Therefore, when using an external filtering resistor between the MPU output and input of the IPM, please care to the signal voltage drop at the input terminals to satisfy the turn-on threshold voltage requirement. For instance, R=100Ω and C=1000pF for the parts shown dotted in Fig.3-13.

Fig.3-14 shows that the internal diodes are electrically connected to the V_{CCL}, IN(HU, HV, HW, LU, LV, LW) and COM terminals. They should not be used for the voltage clamp intentionally to prevent major problems and destroy the IPM.

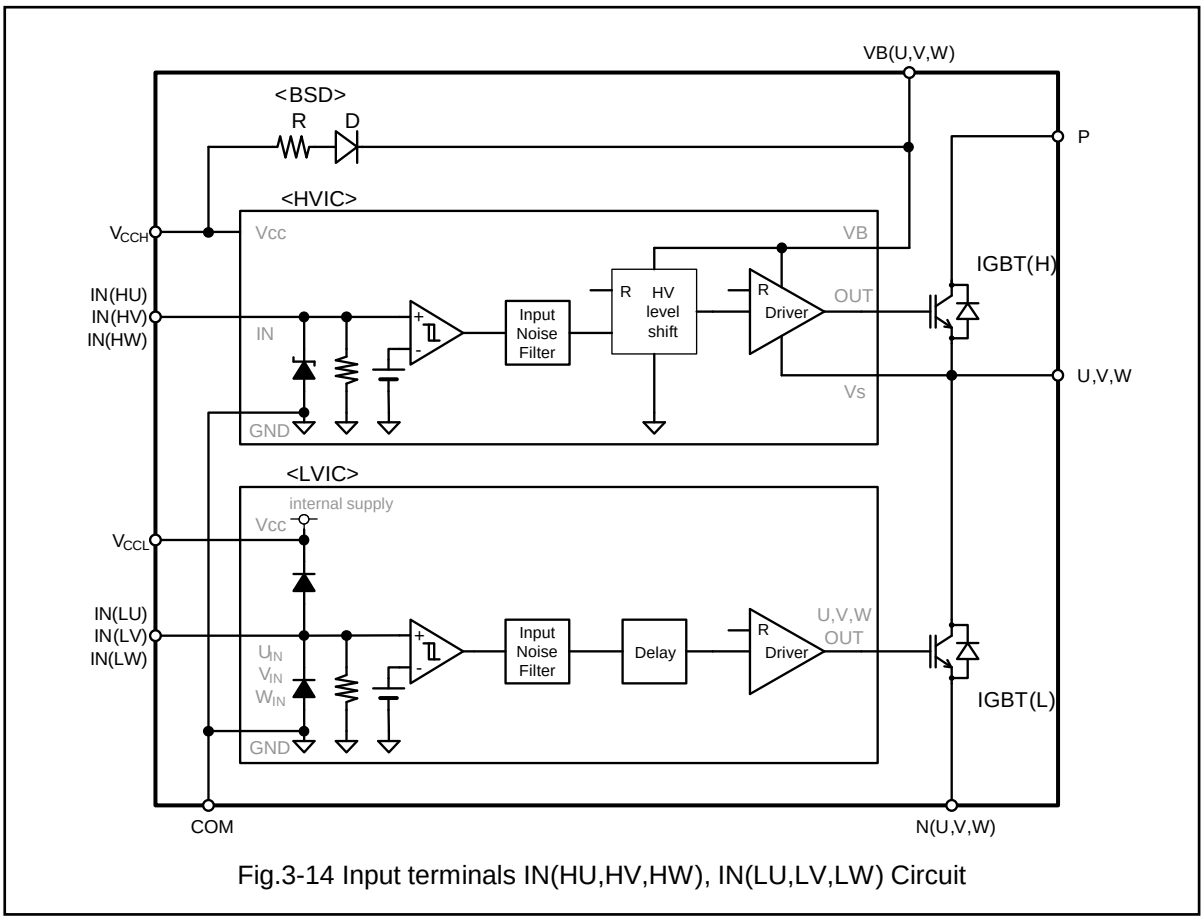

Fig.3-14 Input terminals IN(HU,HV,HW), IN(LU,LV,LW) Circuit

3. IGBT drive state versus Control signal pulse width

$t_{IN(ON)}$ is a recommended minimum turn-on pulse width for changing the IGBT state from OFF to ON, and $t_{IN(OFF)}$ is a recommended minimum turn-off pulse width for changing the IGBT state from ON to OFF. Fig.3-15 and Fig.3-16 show IGBT drive state for various control signal pulse width.

state A : IGBT may turn on occasionally, even when the ON pulse width of control signal is less than minimum $t_{IN(ON)}$. Also if the ON pulse width of control signal is less than minimum $t_{IN(ON)}$ and voltage is applied below -5V between U-COM,V-COM,W-COM , it may not turn off by the malfunction of the control circuit.

state B : IGBT can turn on and is saturated under normal condition.

state C : IGBT may turn on occasionally, even when the ON pulse width of control signal is less than minimum $t_{IN(OFF)}$. Also if the OFF pulse width of control signal is less than minimum $t_{IN(OFF)}$ and voltage is applied below -5V between U-COM, V-COM, W-COM , it may not turn on by the malfunction of the control circuit.

state D : IGBT can turn fully off under normal condition.

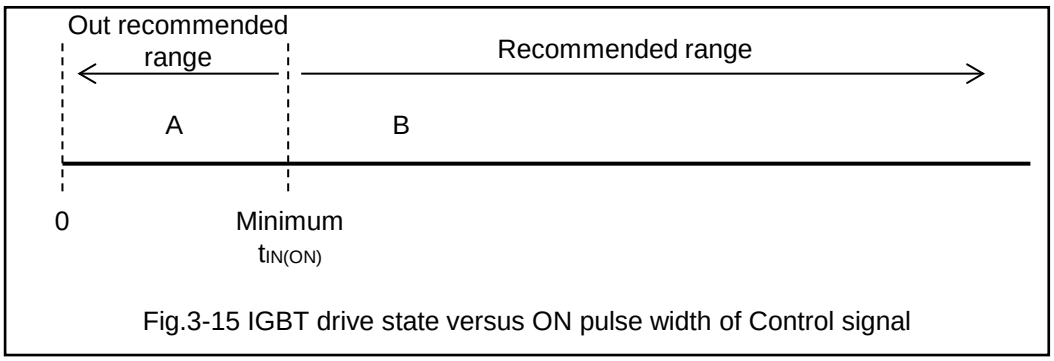

Fig.3-15 IGBT drive state versus ON pulse width of Control signal

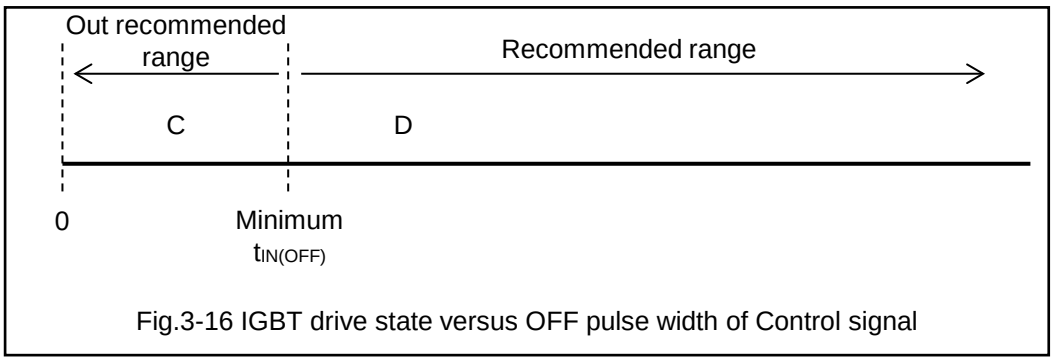

Fig.3-16 IGBT drive state versus OFF pulse width of Control signal

5. Over Current Protection Input Terminal IS

Over current protection (OC) is a function of detecting the IS voltage determined with the external shunt resistor, connected to N(*)*1 and COM.

Fig.3-17 shows the over current sensing voltage input IS circuit block, and Fig.3-18 shows the OC operation sequence.

To prevent the IPM erroneous from the normal switching noise or recovery current, it is necessary to set an external R-C filter (time constant is approximately 1.5μs) to the IS terminal. Also the IPM and the shunt resistor should be wired as short as possible.

Fig.3-17 shows that the diodes in the IPM are electrically connected to the V_{CCL}, IS and COM terminals. They should not be used for the voltage clamp intentionally to prevent major problems and destroy the IPM.

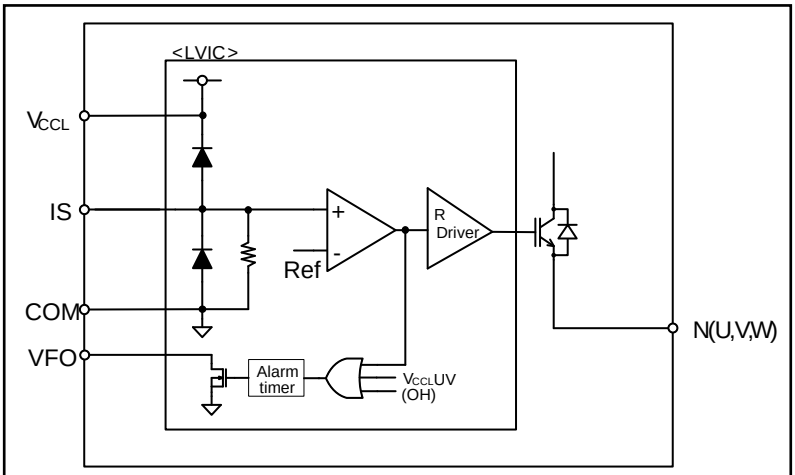

Fig.3-17 Over current sensing voltage input IS circuit

*1 N(*) : N(U), N(V), N(W)

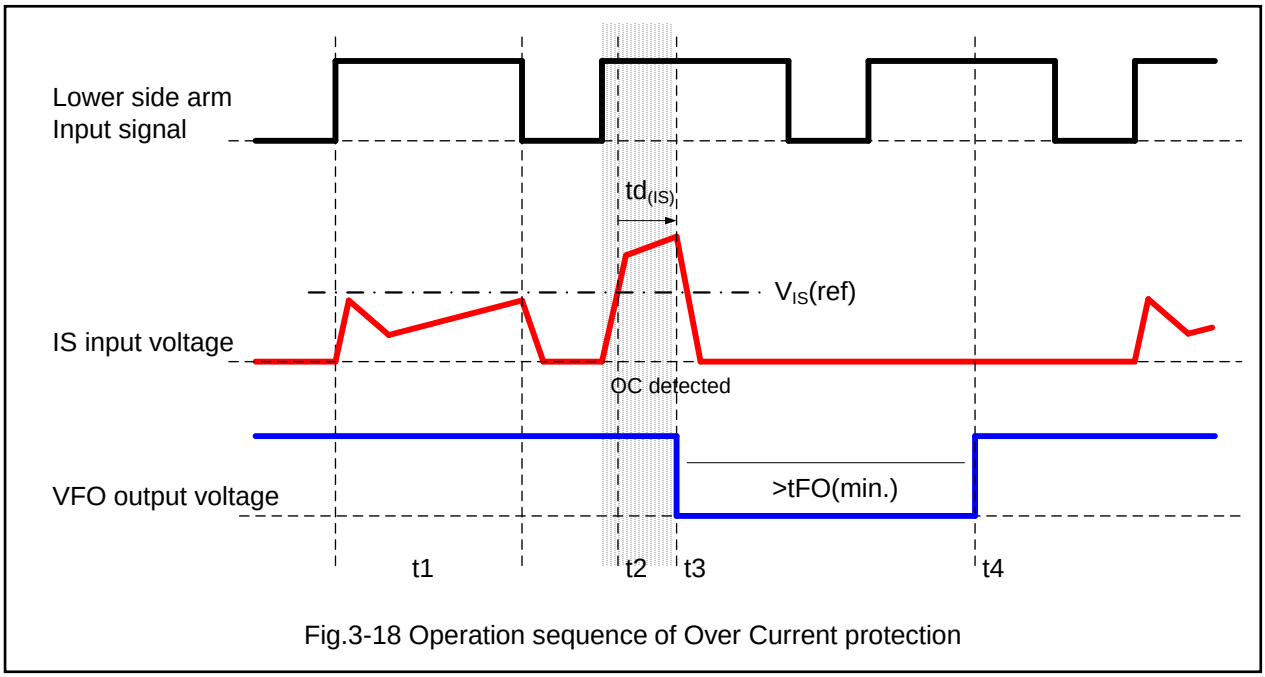

Fig.3-18 Operation sequence of Over Current protection

t1 : IS input voltage does not exceed V_{IS}(ref), while the collector current of the lower side IGBT is under the normal operation.

t2 : When IS input voltage exceeds V_{IS}(ref), the OC is detected.

t3 : The fault output VFO is activated and all lower side IGBT shut down simultaneously after the over current protection delay time $td_{(IS)}$. Inherently there is dead time of LVIC in $td_{(IS)}$.

t4 : After the fault output pulse width tFO, the OC is reset. Then next input signal is activated.

6. Fault Status Output Terminal VFO

As shown in Fig.3-19, it is possible that the fault status output VFO terminal connects directly to the MPU. VFO terminal is open drain configured, thus this terminal should be pulled up by a resistor of approximate 10kΩ to the positive side of the 5V or 3.3V external logic power supply, which is the same as the input signals. It is also recommended that the by-pass capacitors C1 should be connected at the MPU, and the inrush current limitation resistance R1, which is more than 5kΩ, should be connected between the MPU and the VFO terminal. These signal lines should be wired as short as possible to each device.

Fault status output VFO function is activated by the UV of V_{CCL}, OC and OH.
(OH is applied to “6MBP15VSH060-50”, “6MBP20VSC060-50” and “6MBP30VSC060-50”.)

Fig.3-19 shows that the diodes in the IPM are electrically connected to the V_{CCL}, VFO and COM terminals. They should not be used for the voltage clamp intentionally to prevent major problems and destroy the IPM.

Fig.3-20 shows the Voltage-current characteristics of VFO terminal at fault state condition. The IFO is the sink current of the VFO terminal as shown in Fig.3-19.

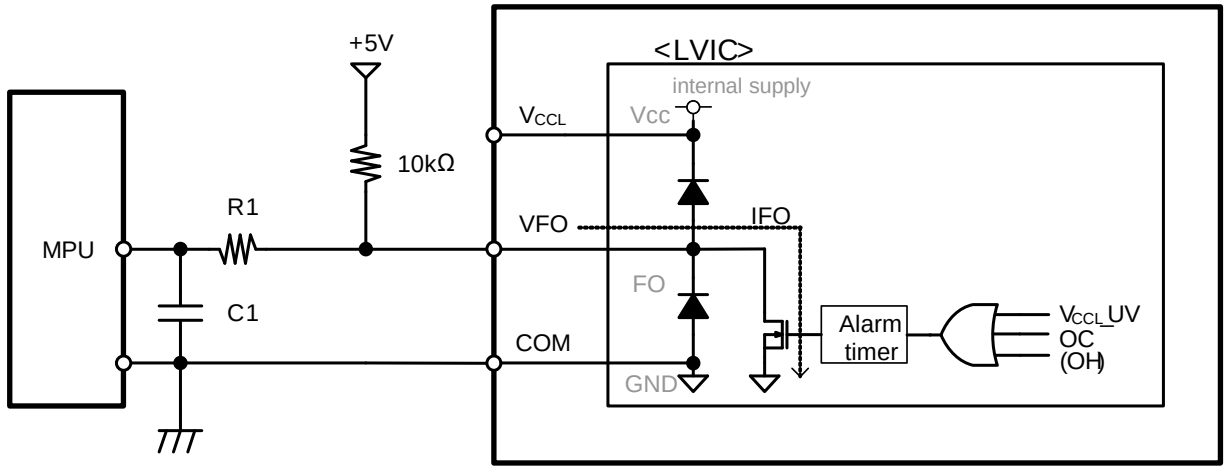

Fig.3-19 Recommended MPU I/O Interface Circuit of VFO terminal

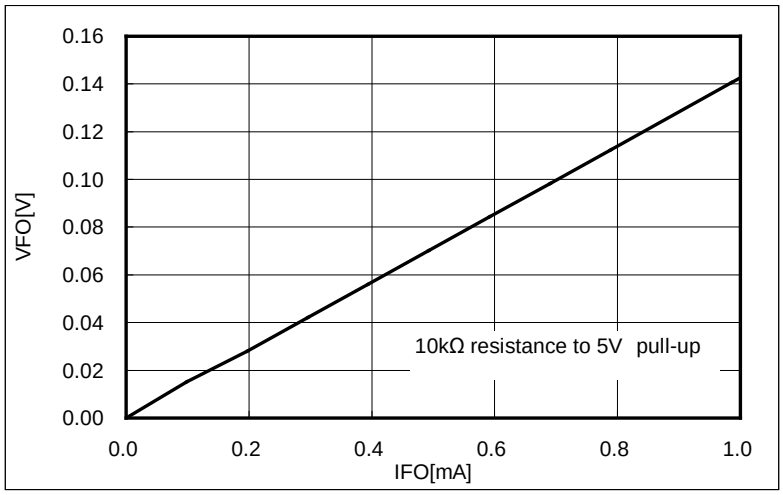

Fig.3-20 Voltage-current Characteristics of VFO terminal at the fault state condition

7. Temperature Sensor Output Terminal TEMP

As shown in Fig. 3-21, the temperature sensor output TEMP can be connected to MPU directly.

It is recommended that a by-pass capacitor and >10kΩ of inrush current limiting resistor are connected between the TEMP terminal and the MPU. These signal lines should be wired as short as possible to each device.

The IPM has a built-in temperature sensor, and it can output an analog voltage according to the LVIC temperature. This function doesn't protect the IPM, and there is no fault signal output.

"6MBP15VSH060-50", "6MBP20VSC060-50" and "6MBP30VSC060-50" have a built-in over-heating protection. If the temperature exceeds TOH, these IPMs output a fault signal by the over-heating protection function.

A diode is electrically connected between TEMP and COM terminal as shown in Fig. 3-12. The purpose of the diode is a protection of the IPM from an input surge voltage. Don't use the diode as a voltage clamp circuit because the IPM might be damaged.

Fig.3-22 shows the LVIC temperature versus TEMP output voltage characteristics. It should be connected the TEMP terminal to a zener diode for the voltage clamp when the power supply of MPU is 3.3V.

Fig.3-23 shows the operation sequence of TEMP terminal at the LVIC startup and shutdown conditions.

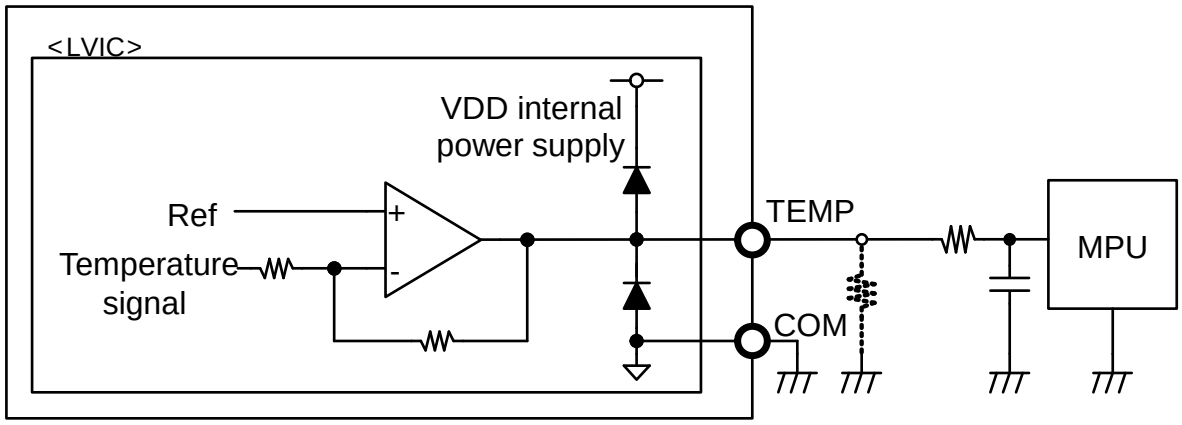

Fig.3-21 Recommended MPU I/O Interface Circuit of TEMP terminal

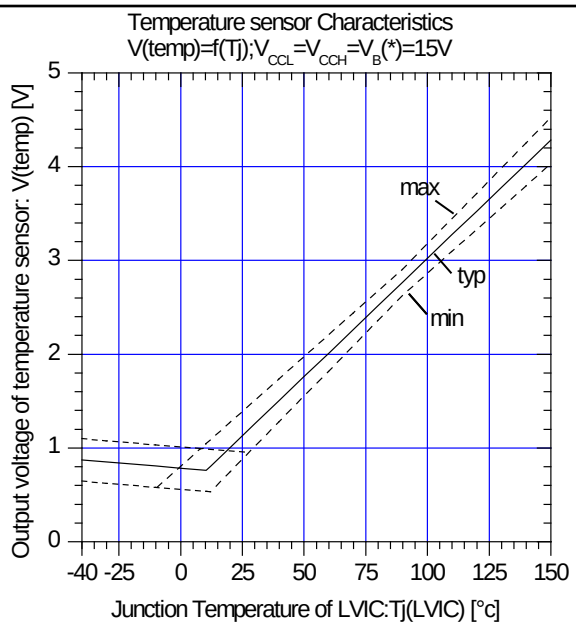

Fig.3-22 LVIC temperature versus TEMP output voltage characteristics

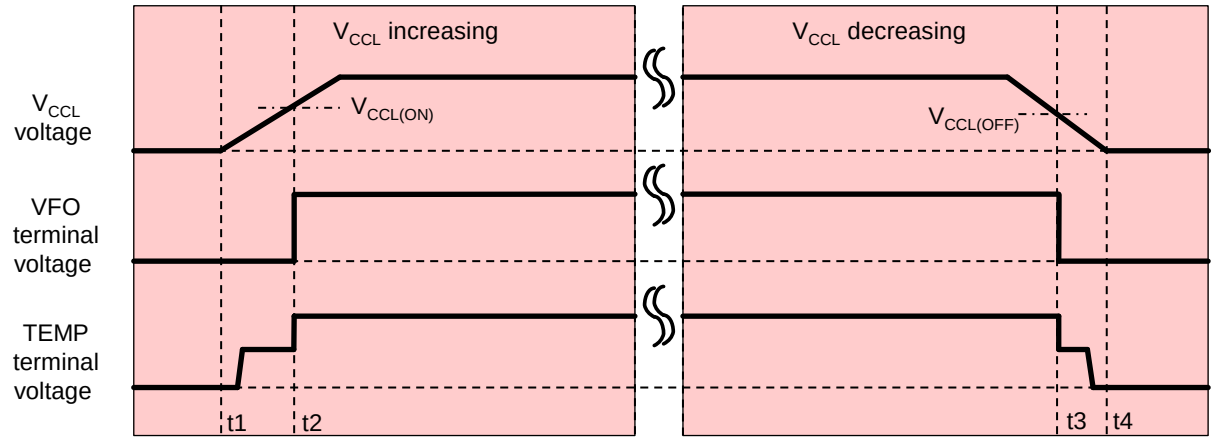

Fig.3-23 Operation sequence of TEMP terminal at the LVIC startup and shutdown conditions

t1-t2 : TEMP function is activated when V_{CCL} exceeds $V_{CCL(ON)}$. If V_{CCL} is less than $V_{CCL(ON)}$, the TEMP terminal voltage is the same as the clamp voltage.

t2-t3 : TEMP terminal voltage rises to the voltage determined with LVIC temperature. In case the temperature is clamping operation, the TEMP terminal voltage is the same as the clamp voltage even though V_{CCL} is less than $V_{CCL(ON)}$.

t3-t4 : TEMP function is reset when V_{CCL} falls below $V_{CCL(OFF)}$. TEMP terminal voltage becomes shutdown and the TEMP terminal voltage is the same as the clamp voltage.

8. Over Heating Protection

The over-heating protection (OH) functions is integrated into "6MBP15VSH060-50", "6MBP20VSC060-50" and "6MBP30VSC060-50".

The OH function monitors the LVIC junction temperature.

The TOH sensor position is shown in Fig.2-2.

As shown in Fig.3-24, the IPM shutdown all lower side IGBTs while the LVIC temperature exceeds TOH. The fault status is reset when the LVIC temperature drops below (TOH-TOH(hys)).

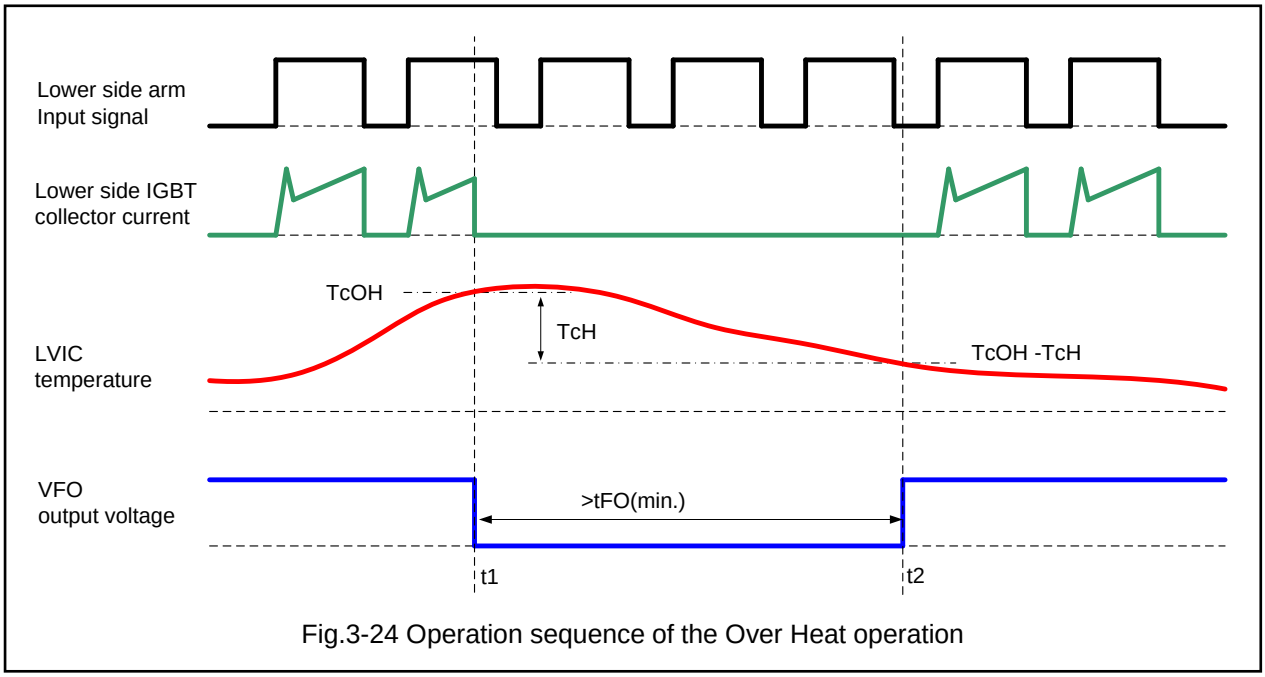

Fig.3-24 Operation sequence of the Over Heat operation

t1 : The fault status is activated and all IGBTs of the lower side arm shutdown, when LVIC temperature exceeds case overheating protection (OH) temperature TOH.

t2 : The fault status, which outputs over t_{FO}, is reset and next input signal is activated, when LVIC temperature falls below TOH – TOH(hys) which is the case overheating protection hysteresis.