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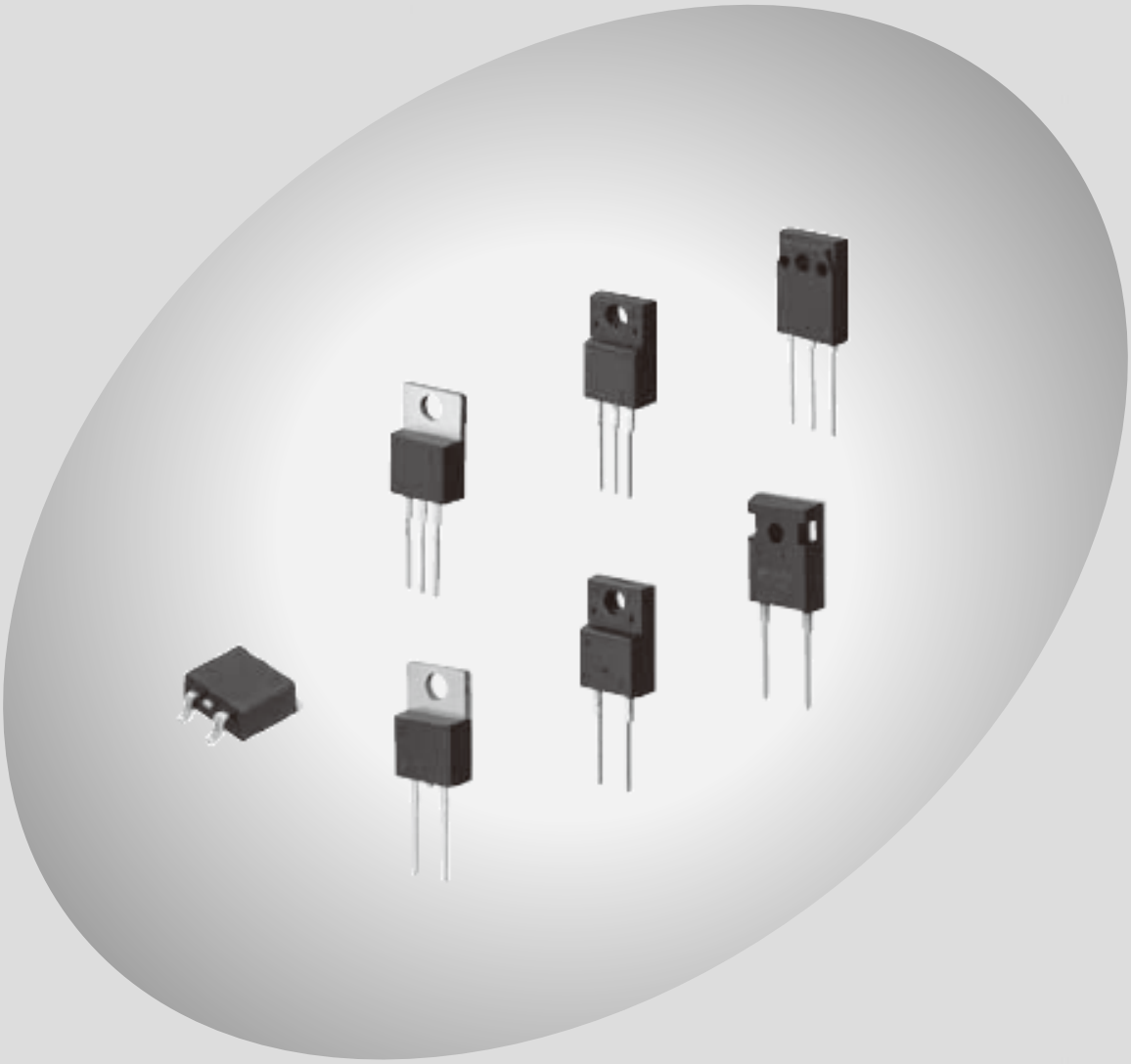

Fuji SiC Schottky Barrier Diode

Application Manual

28th of Feb, 2022 Rev.1_E

Fuji Electric Co., Ltd.

MTET0-3479

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   ・Measurement equipment ・Machine tools ・Audiovisual equipment ・Electrical home appliances
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   ・Emergency equipment for responding to disasters and anti-burglary devices
   ・Safety devices ・Medical equipment

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7.

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Chapter 1 Fuji SiC Schottky Barrier Diode

1. Structure and Characteristics of the Element 1-2
2. Fuji SiC Schottky Barrier Diode Type Name 1-6

1. Structure and Characteristics of the Element

(1) Compatibility between high breakdown voltage and low conduction loss

Silicon carbide (SiC) has an excellent Breakdown Field strength of approximately 10 times that of silicon (Si). Due to this material property, a device with the same breakdown voltage as Si can be realized even when the impurity concentration in the drift layer is increased and the drift layer thickness is reduced, as shown in Figure 1-1. Due to the high concentration of impurities in the drift layer and the thin drift layer, the resistance value when current flows through the drift layer is reduced, and the forward voltage (V_F) can be reduced, as shown in Figure 1-2. This makes it possible to reduce the conduction loss.

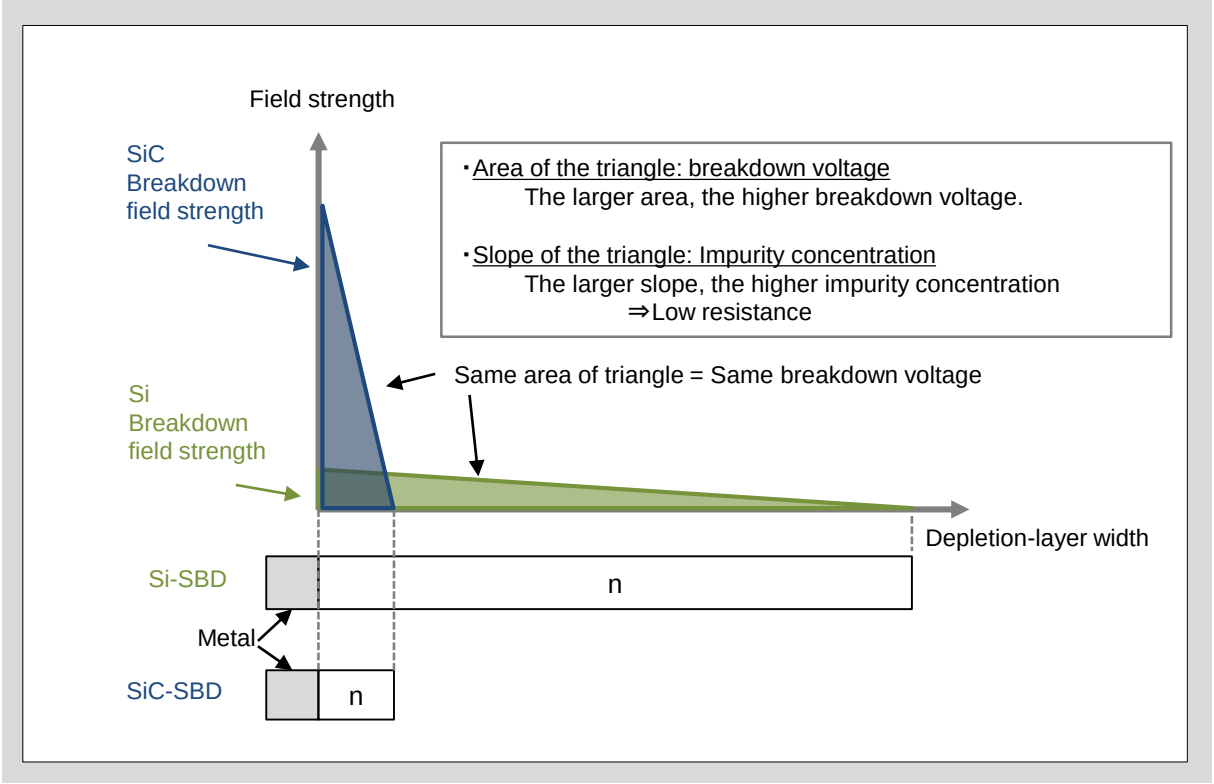


Figure 1-1. Relationship between field strength and depletion layer width of Si-SBD and SiC-SBD

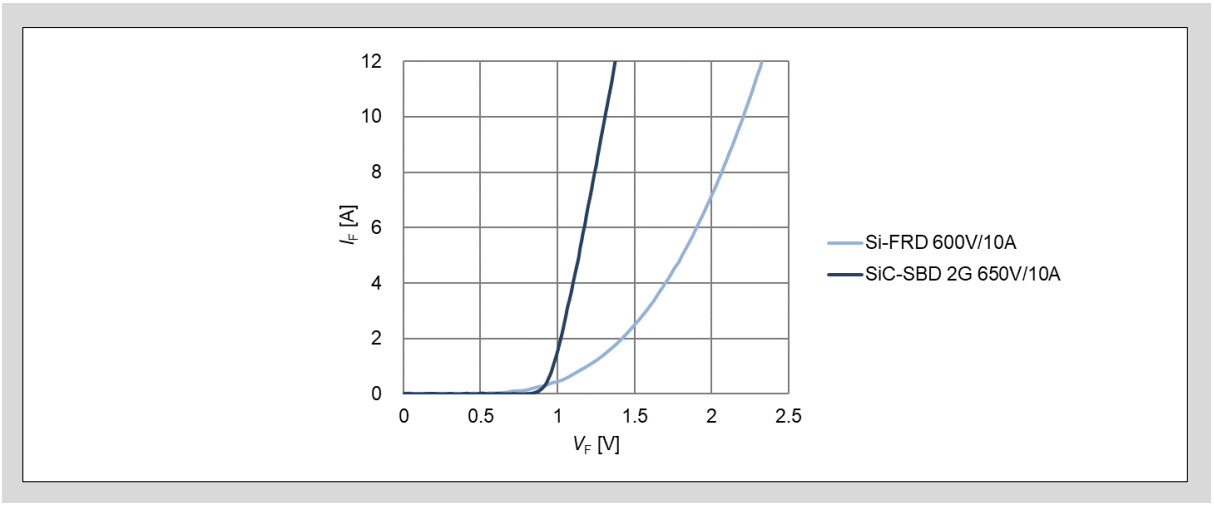


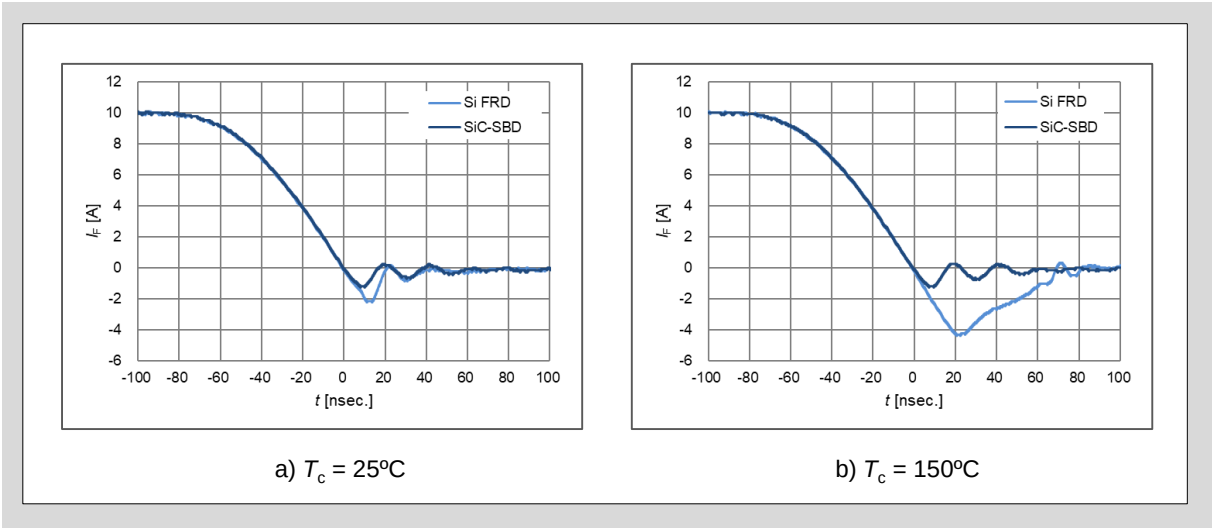
Figure 1-2. Comparison of V_F characteristics (SiC-SBD-2G vs. Si-FRD) (T_c = 25ºC)

(2) High-speed recovery characteristics

High-speed PN junction diodes (Fast Recovery Diode: FRD) of Si with high breakdown voltage are often used for Boost diodes in power factor correction circuits (PFC circuits) and for freewheel diodes in inverter circuits. When a reverse bias is applied to the FRD in which the forward current I_F flows, a large reverse recovery current flows from the cathode to the anode, causing a large switching loss until the minority carriers accumulated disappears. On the other hand, recent power supply circuits require higher efficiency, lower noise, smaller size, and higher power density. In particular, in order to reduce the size of the power supply and increase the power density, the switching frequency tends to be increased, and the ratio of switching loss increases. Therefore, a device which has high breakdown voltage and low recovery loss is required. SiC-SBD can achieve this.

As described earlier, it has high breakdown voltage. And minority carrier accumulation does not occur in principle, because it is a unipolar device that uses only electron for electrical conduction.

Figure 1-3 shows comparison result of the reverse recovery characteristics between SiC-SBD and Si-FRD. It can be seen that the reverse recovery current of SiC-SBD is significantly reduced compared to Si-FRD.



a) T_c = 25ºC b) T_c = 150ºC

Figure 1-3. Comparison of recovery characteristics of SiC-SBD and Si-FRD

(3) Low leakage current characteristics

Fuji's SiC-SBD uses a JBS(Junction Barrier Schottky) structure to suppress leakage current I_R when a reverse bias voltage is applied.

Since SBD semiconductors and metals junction, there are many defects in the junction surface. When a reverse bias voltage is applied, the depletion layer spreads, and the electric field strength at the junction surface where defects exist becomes the highest, causing leakage current.

On the other hand, in SBD with JBS structure, by forming a p+ layer partially in the n-layer as shown in Figure 1-4, when the reverse bias voltage becomes high, the depletion layers of the p+ layers punch through each other, and the position where the electric field strength becomes highest becomes just below the p+ layer, and the electric field strength at the junction surface of the semiconductor and metal with many defects, etc. is lowered, thereby reducing the leakage current.

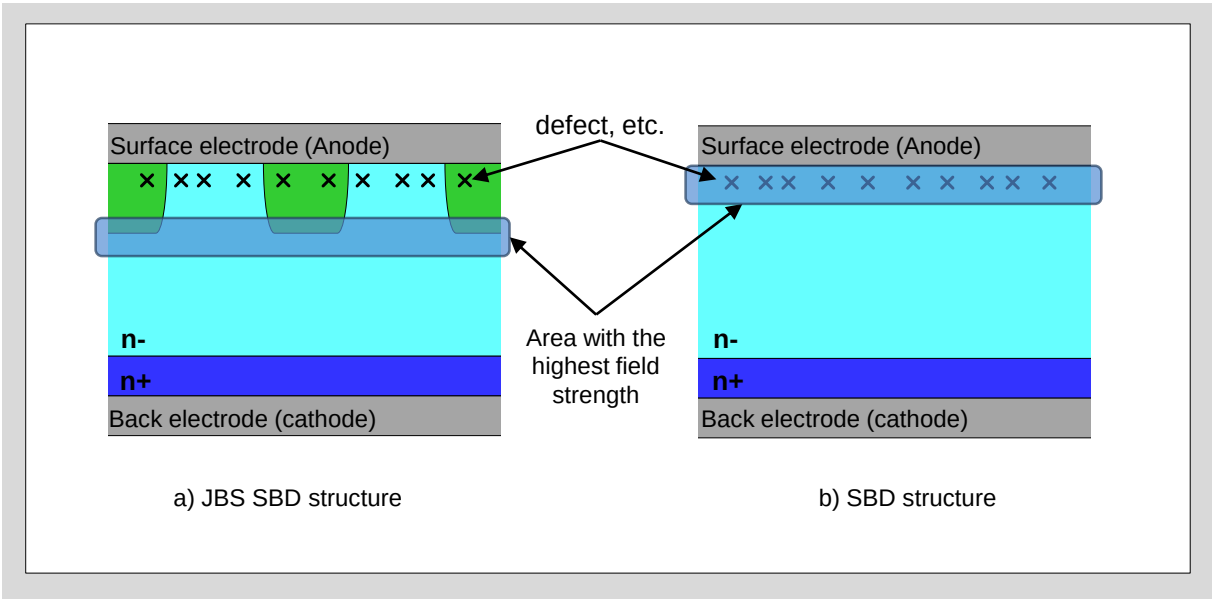
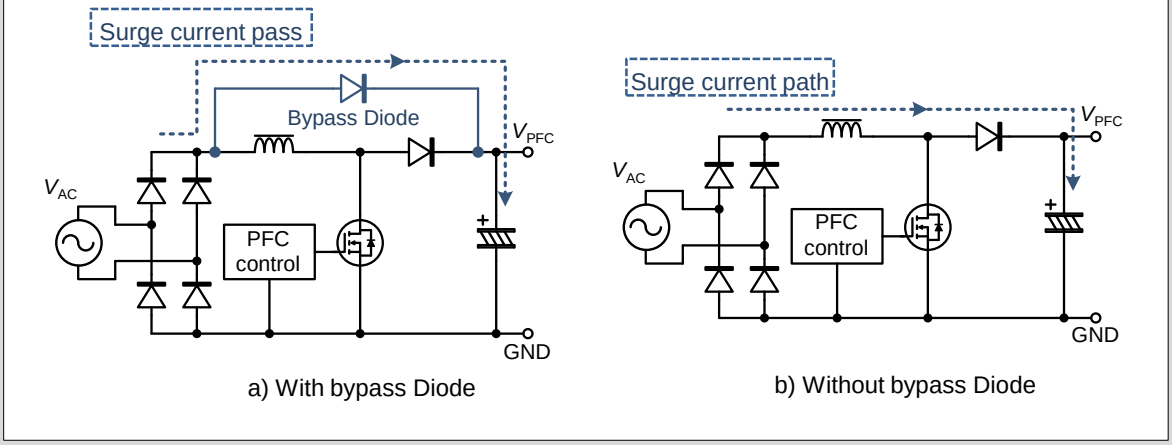


Figure 1-4.JBS SBD and SBD structures

(4) High surge forward current (I_{FSM}) capability

When the power is turned on or when the power is recovered from an instantaneous power failure, a rush current may instantaneously flow in the forward direction to the diode of the PFC circuit in order to charge the smoothing capacitor, as shown in Figure 1-5, and the diode may be damaged. To prevent this, high current is bypassed with high surge Forward Current (I_{FSM}) Diodes. In recent years, there have been an increasing number of circuits without this bypass diode for the purpose of miniaturization and high density. Therefore, SiC-SBD used in PFC circuitry must not be destroyed by a large current flowing instantaneously.

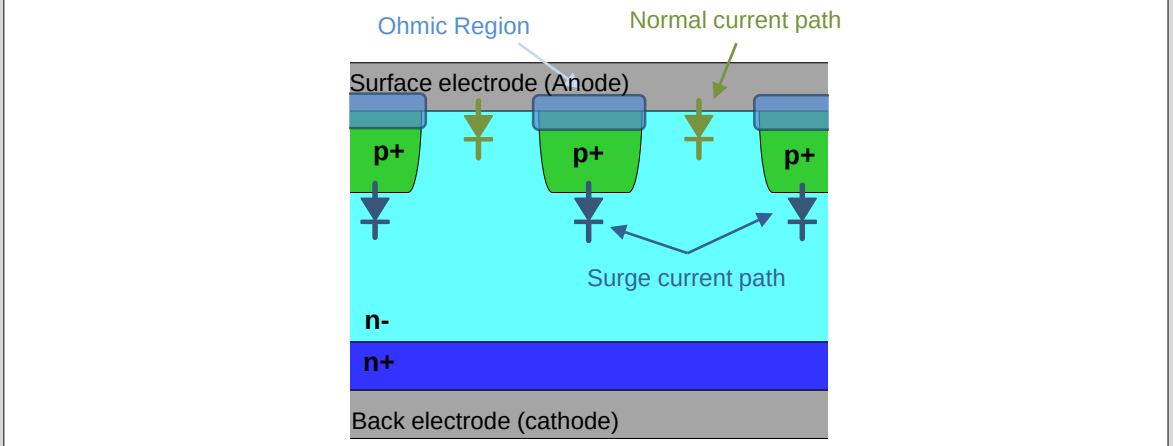
When a large current flows in the forward direction of SiC-SBD instantaneously, a pn junction diode composed of a p+ layer and an n-layer operates, and a large current flows in the ohmic region of the surface electrode (anode) and the p+ layer. In SiC-SBD 2G series, the contact resistance in the ohmic region, which is the interface between the p + layer and the surface electrode (anode) in Figure 1-6, has been reduced by using our unique wafer process technology. By making the pn junction diode easy to operate, the V_F when energized with a large current is reduced and loss is reduced. With this effect, I_{FSM} has been improved.



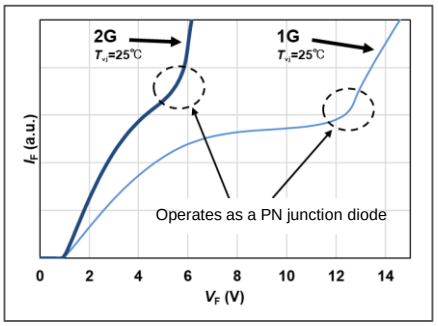
a) With bypass Diode

b) Without bypass Diode

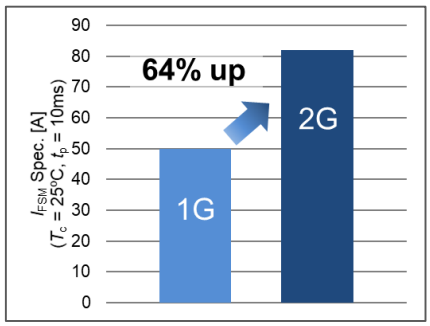
Figure 1-5.Rush current pass



a) SiC-SBD structure



b) $V_F - I_F$ characteristics in the large current range (T_c = 25ºC)



c) Compare I_{FSM} Spec. (650V/10A)

Figure 1-6. Improved I_{FSM} of 2G-SiC-SBD

2. Fuji SiC Schottky Barrier Diode Type Name

Figure 1-7 shows the type name of Fuji SiC-SBD.

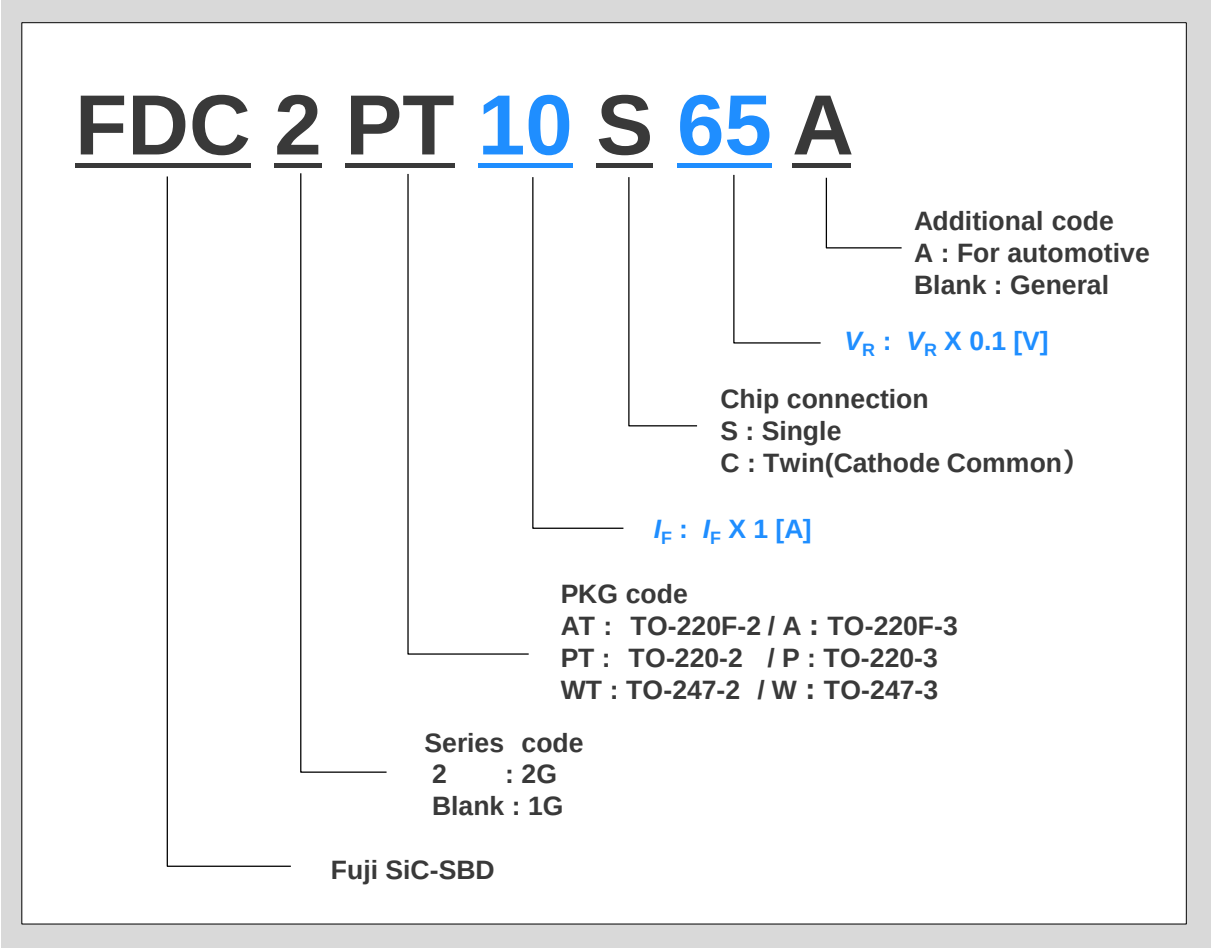


Figure 1-7. Type name of SiC-SBD

Chapter 2 Terms and Definitions of Datasheet

1.	Absolute Maximum Ratings	2-2
2.	Electrical Characteristics	2-3
3.	Thermal Resistance	2-4

The Fuji SiC-SBD data sheet lists the absolute maximum rating, electrical characteristics, and thermal resistance. This chapter explains the terms and characteristics of the data sheet. Some of the series have added or changed terms. Therefore, some terms are not included in the FDC2AT10S65 data sheet provided as a reference example.

1. Absolute Maximum Ratings

Absolute maximum ratings is a value that must be observed in order to use SiC-SBD safely. The values shown in the item of Absolute maximum ratings are the values when the junction temperature T_{vj} is 25ºC unless otherwise specified. It is necessary to refer to the temperature derating graph according to the actual environment temperature and use it so as not to exceed the specification range. For reference, Absolute maximum ratings listed in FDC2AT10S65 data sheet are shown in Fig. 2-1. Table 2-1 shows the definitions and explanations of the terms listed in Absolute maximum ratings.

● **Absolute Maximum Ratings at T_{vj}= 25°C(unless otherwise specified)**

Parameter	Symbol	Value	Unit	Remarks
Repetitive peak reverse voltage	V_{RRM}	650	V	
Continuous forward current	I_F	10	A	T_c < 115 °C, D = 1
Surge non-repetitive forward current (half sine wave)	I_{FSM}	82	A	T_c = 25 °C, t_p= 10 ms
		61.5	A	T_c = 150 °C, t_p= 10 ms
I^2t value	$\int I^2dt$	33.6	A^2s	T_c = 25 °C, t_p= 10 ms
		18.9	A^2s	T_c = 150 °C, t_p= 10 ms
Max. Power Dissipation	P_{tot}	54	W	T_c = 25 °C
Operating junction temperature	T_{vj}	175	°C	
Storage temperature	T_{stg}	-55 ~ +175	°C	
Isolation Voltage	V_{iso}	2	kVrms	t = 60sec, f = 60Hz

Figure 2-1. FDC2AT10S65 Data Sheet excerpt (Absolute Maximum Ratings)

Table 2-1. Absolute Maximum Ratings Term Explanation

∗ Unless otherwise specified, T_{vj} = 25ºC.

Term	Symbol	Definition and Explanation
Repetitive peak reverse voltage	V_{RRM}	Maximum value of the reverse voltage that can be repeatedly applied.
Continuous forward current	I_F	Maximum value of continuous forward current.
Surge non-repetitive forward current (half sine wave)	I_{FSM}	In half cycle of 50Hz sine wave (t_p = 10ms), Maximum value of non-repeating forward surge current.
I^2t value	$\int I^2dt$	The maximum current instantly and its pulse width (1ms ≤ t_p < 10ms) .
Max. Power Dissipation	P_{tot}	Allowable power dissipation on the device.
Operating junction temperature	T_{vj}	Junction temperature at which device operation is allowed.
Storage temperature	T_{stg}	Temperature range that can be stored and transported without electrical load on the device.
Isolation Voltage	V_{iso}	Maximum dielectric strength voltage on the back side of the package; applies only to full-molded packages.

2. Electrical Characteristics

Electrical characteristics of the data sheet include static characteristics and dynamic characteristics. Unless otherwise specified, T_{vj} = 25ºC. Static characteristics are the values measured under the conditions described in the data sheet, and the values in a stable state where the device is ON or OFF are described. Dynamic characteristics describes the values of the switching characteristics when the device switches from on to off. This section explains static and dynamic characteristics, respectively. For reference, Electrical characteristics listed in FDC2AT10S65 data sheet are shown in Fig. 2-2. Table 2-2 and 2-3 shows the definitions and explanations of the terms listed in Electrical characteristics.

● Electrical Characteristics at T_{vj}= 25°C(unless otherwise specified)

Static characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DC blocking voltage	V_{DC}	I_R = 1 mA	650	-	-	V
Forward voltage	V_F	I_F = 10A, T_{vj}= 25 °C	1.10	1.30	1.50	V
		I_F = 10 A, T_{vj}= 150 °C	-	1.48	1.99	V
Reverse current	I_R	V_R= 650 V, T_{vj}= 25 °C	-	0.4	50	μA
		V_R= 650 V, T_{vj}= 150 °C	-	2	200	μA

Dynamic characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Total Capacitive Charge	Q_C	V_R= 400 V, I_F= 10 A, -di/dt= 200 A/μs, T_{vj}= 150 °C	-	9.5	-	nC
Total Capacitance	C	V_R= 400 V, f = 1 MHz	-	44	-	pF

Figure 2-2. FDC2AT10S65 Data Sheet excerpt (Electrical characteristics)

Table 2-2. Electrical characteristics (Static) Term Explanation ∗ Unless otherwise specified, T_{vj} = 25ºC.

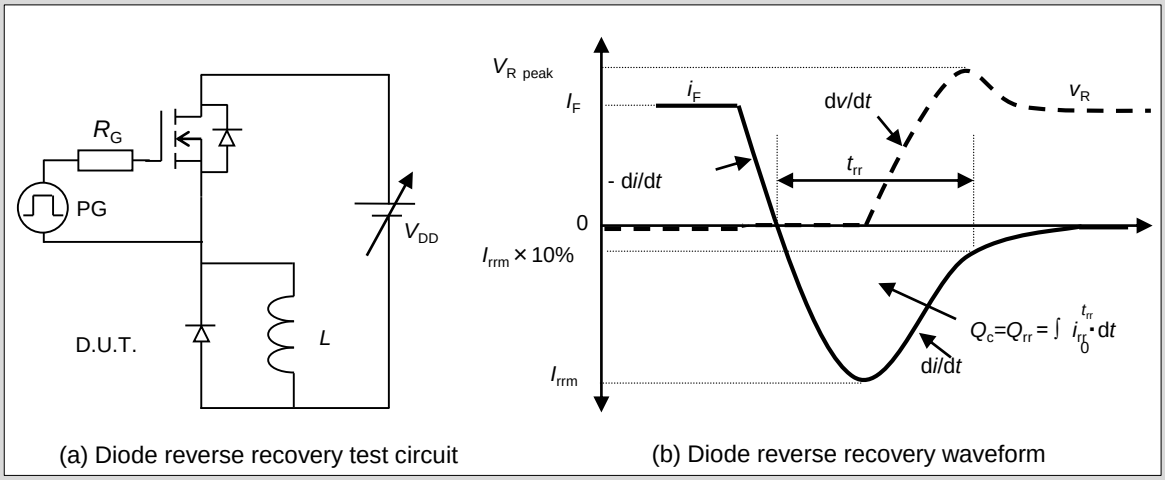
Term	Symbol	Definition and Explanation
DC blocking voltage	V_{DC}	DC reverse voltage that can be applied.
Forward Voltage	V_F	Value of voltage drop when the specified forward current is applied at the specified temperature.
Reverse Current	I_R	Reverse blocking current for reverse voltage at specified temperature.

Table 2-3. Electrical characteristics (Dynamic) Term Explanation ∗ Unless otherwise specified, T_{vj} = 25ºC.

Term	Symbol	Definition and Explanation
Total Capacitive Charge	Q_c	Total amount of charge when charged to the specified reverse voltage.
Total Capacitance	C	Capacitance value between terminals when specified reverse voltage and frequency are applied.

Test circuit for dynamic characteristics

For reference, Figure. 2-3 shows dynamic characteristic test circuit and measurement waveform of Fuji SiC-SBD.



(a) Diode reverse recovery test circuit (b) Diode reverse recovery waveform

Figure 2-3. Test circuit of total Capacitive charge Q_c, measurement waveform

3. Thermal Resistance

Figure 2-4 shows Thermal Resistance described in the FDC2AT10S65 data sheet as a reference example. Table 2-4 explains the terms described in Thermal Resistance.

● Thermal Resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance, Junction –Ambient	$R_{th(j-a)}$	-	-	58	°C/W
Thermal Resistance, Junction –Case	$R_{th(j-c)}$	-	-	2.80	°C/W

Figure 2-4. FDC2AT10S65 Data Sheet excerpt (Thermal Resistance)

Table 2-4. Electrical characteristics (Thermal Resistance) Term Explanation

Term	Symbol	Definition and Explanation
Thermal Resistance, Junction – Ambient	$R_{th(j-a)}$	Thermal resistance from the junction to the ambient that is not affected by temperature rise. It is the thermal resistance when the device is used in standalone without heat sink. A characteristic that has the same value for each package.
Thermal Resistance, Junction – Case	$R_{th(j-c)}$	Thermal resistance from the junction to the device case surface (heat sink mounting surface). It is a characteristic determined by the package and chip size, and the larger the chip size, the smaller the thermal resistance. Use this value for calculating the thermal resistance when mounted to the heat sink.

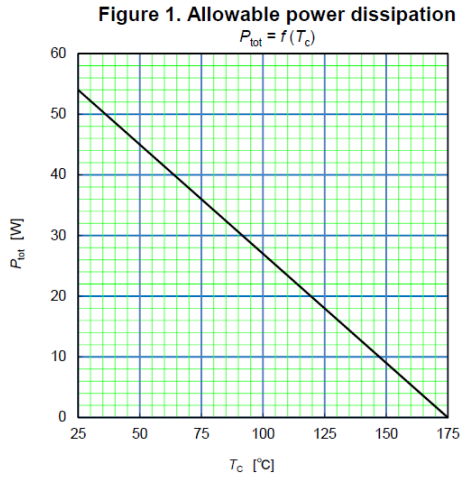
Chapter 3 Device Characteristics

1.	Allowable Power Dissipation	3-2
2.	Peak forward current	3-3
3.	Typical forward characteristics	3-4
4.	Typical reverse characteristics	3-4
5.	Typical capacitance characteristics	3-5
6.	Transient Thermal Impedance	3-6

In order to use SiC-SBD safely, the device characteristics described in the data sheet must also be taken into consideration in the circuit design. This chapter is explained based on the data sheet of FDC2AT10S65 of 2G series.

1. Allowable Power Dissipation

Figure 3-1 is a graph showing the relationship between the Allowable Power Dissipation P_{tot} of the FDC2AT10S65 and the case temperature T_C. P_{tot} represents the power dissipation when the junction temperature T_{vj} reaches the maximum rated value, and the allowable power dissipation decreases as the case temperature increases. In the actual design, it is important not to exceed the P_{tot} at the assumed maximum T_c. In addition, the Allowable Power Dissipation described in the absolute maximum ratings of the data sheet is in the ideal heat dissipation state where the package is attached to the infinite heat sink. The following is an example of calculating the P_{tot} in each state.



Self standing

$$P_{\mathrm{tot}} = \frac{T_{\mathrm{vj(max)}} - T_{\mathrm{a}}}{R_{\mathrm{th(j-a)}}} [\mathrm{W}]$$

Ideal heat dissipation

$$P_{\mathrm{tot}} = \frac{T_{\mathrm{vj(max)}} - T_{\mathrm{c}}}{R_{\mathrm{th(j-c)}}} [\mathrm{W}]$$

P_{tot}: Maximum Allowable Power Dissipation
$T_{\mathrm{vj(max)}}$: Maximum Operating Junction Temperature
T_{a}: Ambient Temperature
T_{c}: Case Temperature
$R_{\mathrm{th(j-a)}}$: Junction to Ambient Thermal Resistance
$R_{\mathrm{th(j-c)}}$: Junction to Case Thermal Resistance

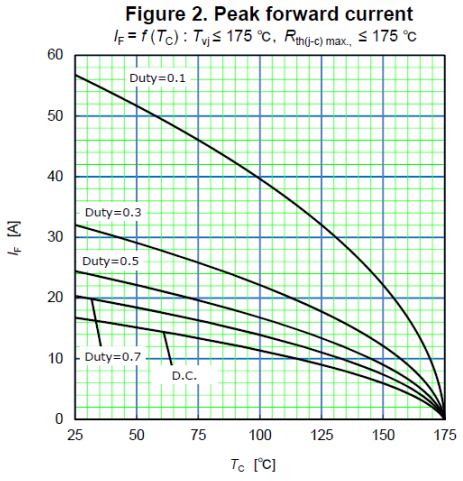
Figure 3-1. Allowable power dissipation of FDC2AT10S65

2. Peak forward current

Figure 3-2 shows the peak forward current characteristics of the FDC2AT10S65. This graph shows the allowable forward current I_F at a given case temperature T_c, and the higher the case temperature, the smaller the I_F. In the actual design, it is important not to exceed the I_F at the assumed maximum T_C.

The condition for the forward current of 10A, which is the absolute maximum rating of FDC2AT10S65, is T_c < 115ºC, Duty = 1 (continuous), and the DC line shown in the graph crosses at the points of I_F = 10A and T_c = 115ºC.

In the case of the graph in Fig. 3-2, the I_F at Duty = 0.5 and T_c = 100ºC is 17.5A.



$$P = V_{F(max)@175°C} \times I_F \times \text{Duty}\ [\text{W}]$$

$$T_c = T_{vj(max)} - R_{th(j-c)} \times P\ [°\text{C}]$$

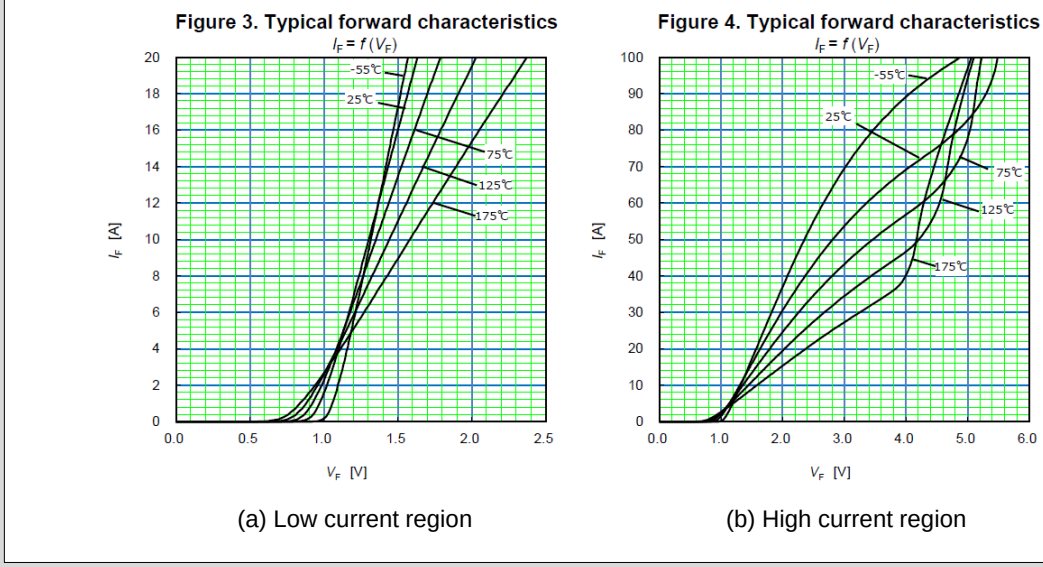
P: Power dissipation
V_F: Forward Voltage
I_F: Forward current
Duty: Time ratio of Forward current
$T_{vj(max)}$: Maximum Operating Junction Temperature
T_a: Ambient Temperature
T_c: Case Temperature
$R_{th(j-c)}$: Junction to Case Temperature

Figure 3-2. Peak Forward current of FDC2AT10S65

3. Typical forward characteristics

Figure 3-3 shows the forward characteristic graph of the FDC2AT10S65. This graph shows the relationship between the Forward Voltage V_F and the Forward Current I_F. This characteristic has a positive or negative temperature dependence depending on the current range. The data sheet describes the Low current region (a) and the High current region (b).

In the case of FDC2AT10S65, V_F shows negative temperature dependence in the low current region up to I_F = 4A. Note that if the devices are connected in parallel and used in a negative temperature-dependent region of V_F, the current may concentrate to one device.



(a) Low current region

(b) High current region

Figure 3-3. Typical forward characteristics of FDC2AT10S65

4. Typical reverse characteristics

Figure 3-4 shows the reverse characteristic graph of FDC2AT10S65. This graph shows the Reverse Current I_R when a Reverse Voltage is applied. Since this property is positive temperature dependence, it is important to consider the loss caused by the reverse I_R at the assumed maximum T_C in the actual design.

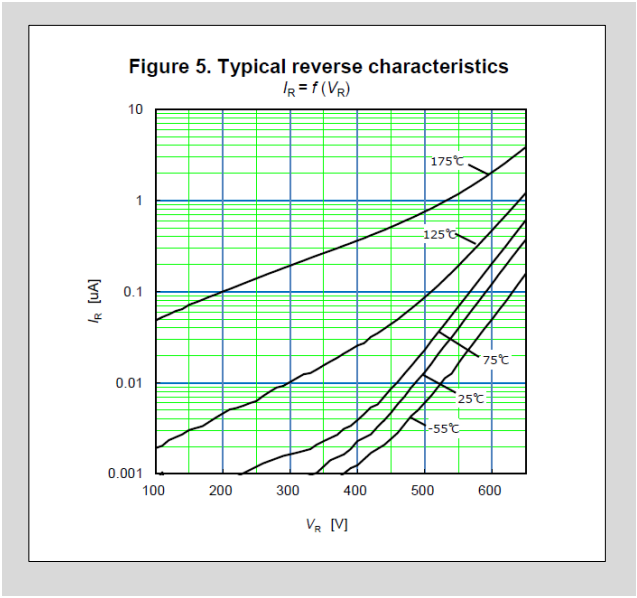
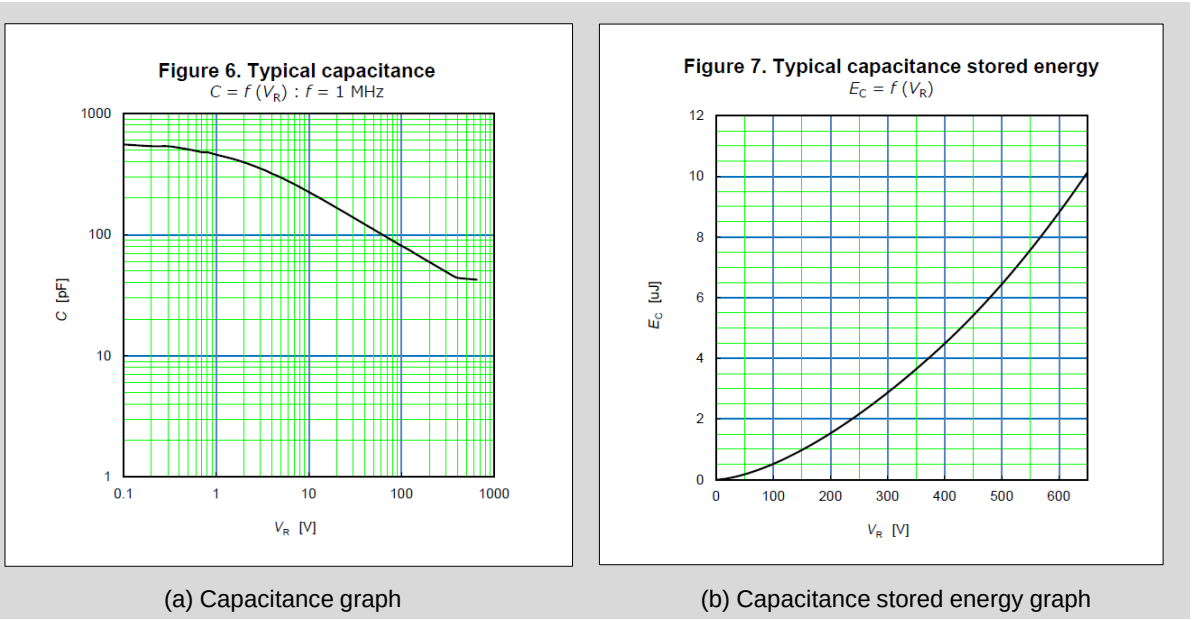


Figure 3-4. Reverse Current characteristics of FDC2AT10S65

5. Typical forward characteristics

Figure 3-5 shows the capacitance characteristic graph of FDC2AT10S65. The Capacitance C shown in (a) has the characteristic that it changes depending on the Reverse voltage V_R. The Capacitance stored energy E_C shown in (b) represents the energy required to charge from V_R = 0V to the specified V_R.



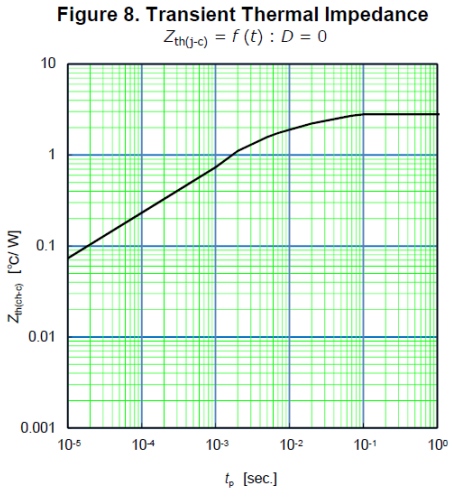
(a) Capacitance graph

(b) Capacitance stored energy graph

Figure 3-5. Capacitance characteristics of FDC2AT10S65

6. Transient Thermal Impedance

Generally, the Thermal Resistance characteristic values described in catalogs and data sheets are steady-state thermal resistance values. When calculating the temperature rise of a device for the thermal design of pulse-operated equipment such as switching power supplies, it is necessary to read the thermal resistance at an arbitrary time from the Transient Thermal Impedance graph (Figure 3-6) described in the data sheet, or to use the calculated value. Although the curve shows the transient thermal impedance of a single pulse with D=0, the transient thermal impedance of repeated pulses can also be calculated as shown in Figure 3-7.



Calculation formula for Transient Thermal Impedance at pulse width t < 1ms

$$Z_{\mathrm{th(j-c)}}(t) = Z_{\mathrm{th(j-c)}}(1\mathrm{ms}) \times \sqrt{t \times 10^3}$$

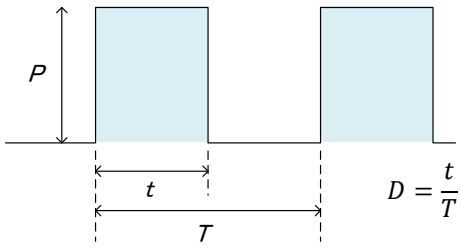
$Z_{\mathrm{th(j-c)}}(1\mathrm{ms})$:Transient Thermal Impedance with a pulse width of 1ms

Figure 3-6. Transient Thermal Impedance of FDC2AT10S65

Calculation formula for Transient Thermal Impedance during repeated loss pulse

$$Z_{\mathrm{th(j-c)(R)}} = D \times R_{\mathrm{th(j-c)}} + (1 - D) \times Z_{\mathrm{th}}(T + t) - Z_{\mathrm{th}}(T) + Z_{\mathrm{th}}(t)$$

Each Transient Thermal Impedance in the above equation is read from the Transient Thermal Impedance curve of a single pulse (D = 0) described in the data sheet, and the Transient Thermal Impedance at the time of repeated loss pulse is calculated.



T: Loss pulse period [s]

t: Loss pulse width [s]

D: Time ratio of Loss pulse, t/T

$Z_{th(j-c)(R)}$: Repeated Transient Thermal Impedance

$R_{th(j-c)}$: Thermal Resistance

$Z_{th}(T + t)$: Transient Thermal Impedance at pulse width $T + t$

$Z_{th}(T)$: Transient Thermal Impedance at pulse width T

$Z_{th}(t)$: Transient Thermal Impedance at pulse width t

Figure 3-7. Calculation formula for Transient Thermal Impedance during repeated loss pulse

Chapter 4 Loss Estimation and Thermal Design

1.	Concept of heat dissipation	4-2
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1. Concept of heat dissipation

Transient Thermal Impedance and Thermal Resistance

There are two methods to dissipate heat from the loss generated at the Junction of the devices, one is to attach it to the Heat sink and the other is self standing. In the former case, the heat dissipation path can be simulated by an electric circuit with the thermal resistance R_{th} and the heat capacity C_{th}. Figure 4-1 shows the heat dissipation path simulated by an electric circuit.

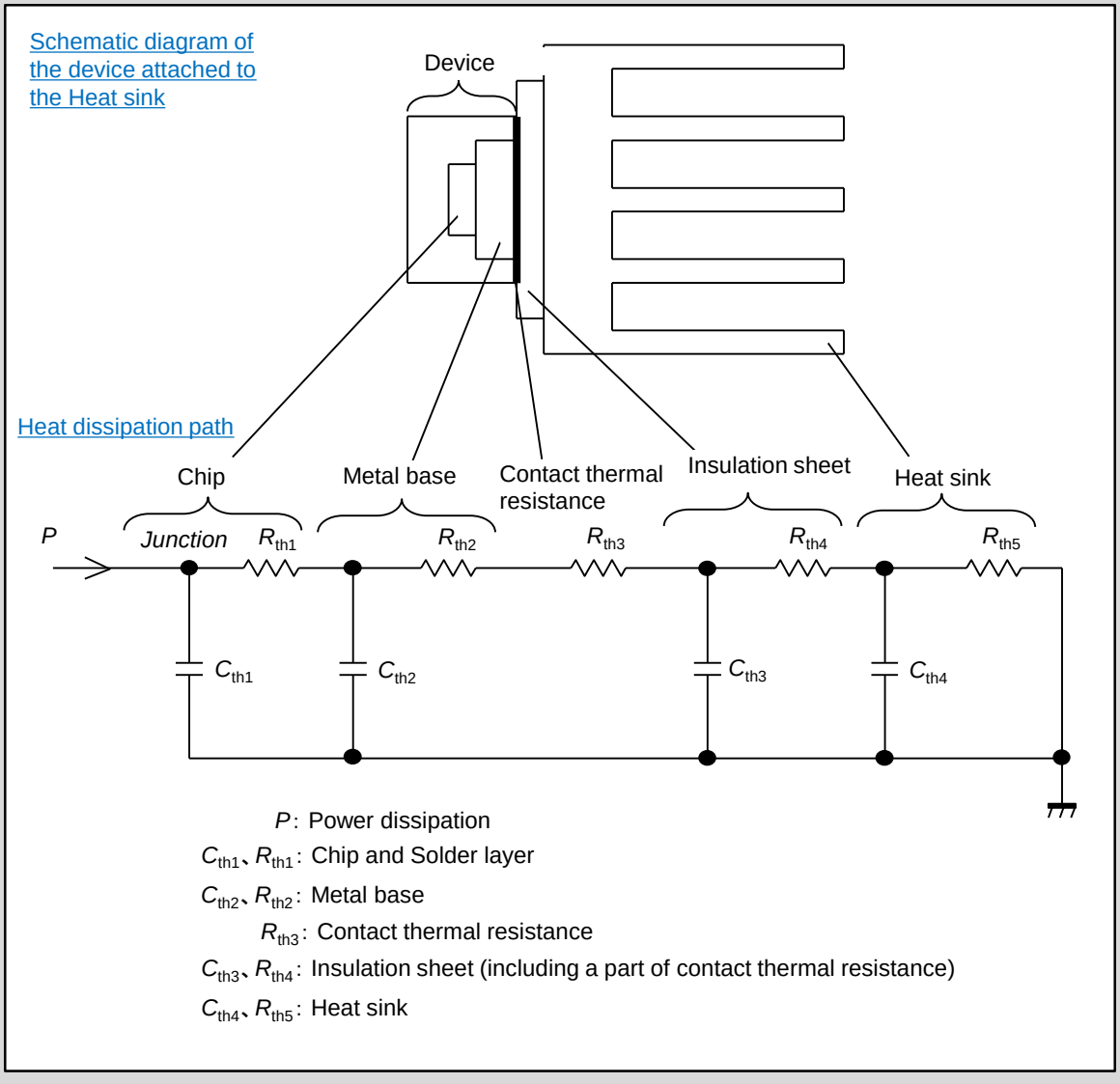


Figure 4-1. Heat dissipation path expressed by an electric circuit

The Transient Thermal Impedance (Z_{th}) is the Thermal Resistance until the heat capacities C_{th1} to C_{th4} shown in the heat dissipation path in Figure 4-1 are saturated, and is a function of time. The maximum value of the Transient Thermal Impedance characteristics of each element when the loss is a single pulse (D = 0 *) is specified on the data sheet. (* $D = t / T$, t: Pulse-on time, T: Time of one cycle ; for a single pulse is $T = \infty$, $D = 0$.)

Figure 4-2 shows the equation for the transient thermal resistance of the Heat sink.

$$Rf(t) = R_{\mathrm{th(f-a)}} \times \left(1 - \varepsilon^{-\frac{t}{\tau_f}}\right)$$

where, $\tau_f = R_{\mathrm{th(f-a)}} \times V \times \gamma \times C$

$R_{\mathrm{th(f\text{-}a)}}$: Heat sink steady thermal resistance [ºC/W]
t : Time [sec]
τ_f : Thermal time constant of the Heat sink [sec]
V : Heat sink volume [cm³]
γ : Specific gravity [g/cm³]
C : Specific heat [W・sec/g・deg]

Figure 4-2. Transient Thermal Impedance of Heat sink

Table 4-1 shows the specific gravity and specific heat of the materials required for this calculation, and Figure 4-3 shows the steady thermal resistance of the aluminum Heat sink (black painted).

Table 4-1. Specific gravity and specific heat of each material

Material	Specific gravity γ [g/cm³]	Specific heat [W・s/g・deg]
Aluminum	2.71	0.895
Copper	8.96	0.383

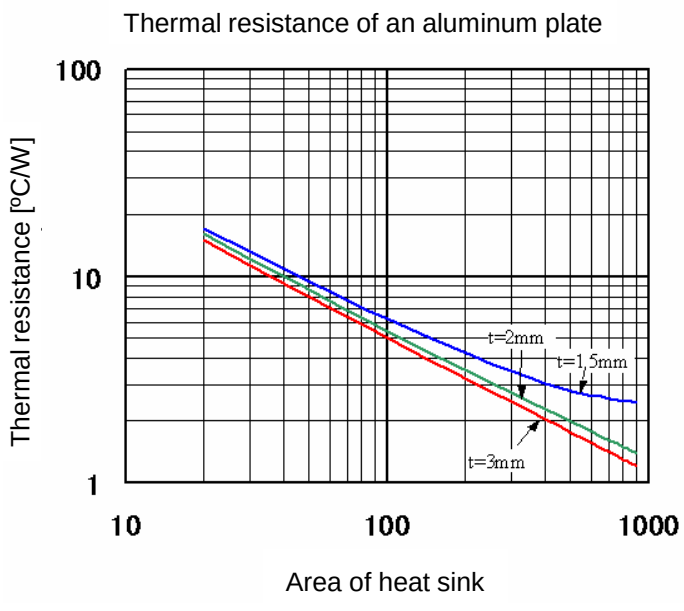


Figure 4-3. Steady-state thermal resistance of aluminum heat sink

Since the steady-state thermal resistance (R_{th}) is not affected by thermal capacitance, the junction temperature can be calculated easily. The calculation formula is shown in Figure 4-4.

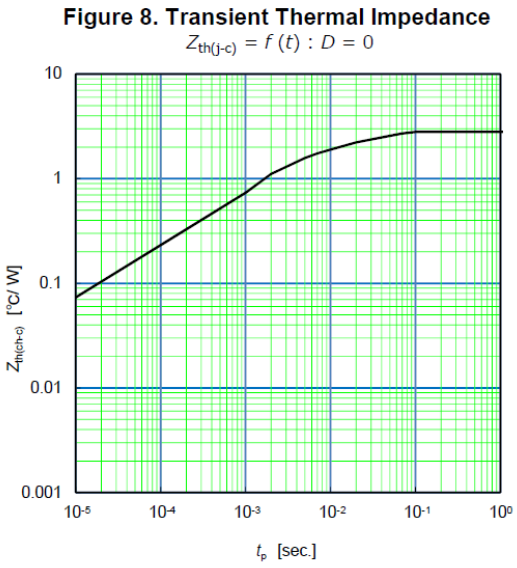
$$T_{vj} = T_a + \left(R_{th(j-c)} + R_{th(c-i)} + R_{th(i)} + R_{th(i-f)} + R_{th(f-a)}\right) \times P$$

T_{vj}: Junction temperature
T_a: Ambient temperature
$R_{th(j-c)}$: Thermal resistance between junction and case
$R_{th(i)}$: Insulation sheet thermal resistance
$R_{th(c-i)}$、$R_{th(i-f)}$: Contact thermal resistance
$R_{th(f-a)}$: Thermal resistance of heat sink
P: Generated power dissipation

Figure 4-4. Formula for calculating the junction temperature

2. Transient Thermal Impedance characteristics of the device

The device specifications describe the transient thermal impedance characteristics between the junction and case of the device to aid in thermal design. Figure 4-5 shows the transient thermal impedance characteristics of the FDC2AT10S65 as an example.



This graph shows the transient thermal impedance $Z_{th(j-c)}$ at the time of a single pulse (D=0). For example, $Z_{th(j-c)}$ with a pulse width of 1ms is approximately 0.7 [ºC/W].

When the device is attached to heat sink, the forward current I_F is 10.8A for 1ms, and the forward voltage V_F is 1.5V (T_{vj} = 125ºC), the transient temperature rise ΔT_{vj} from the case to the junction will be as follows.

$$\Delta T_{vj} = V_F \times I_F \times Z_{th(j-c)}\,(1\text{ms})$$

$$= 1.5[\text{V}] \times 10.8[\text{A}] \times 0.7[\text{°C/W}]$$

$$\cong 11.4[\text{degree}]$$

This transient thermal impedance characteristic is effective only when attached to the heat sink.

Figure 4-5. Transient thermal impedance characteristics

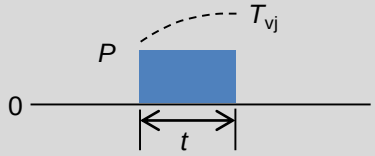
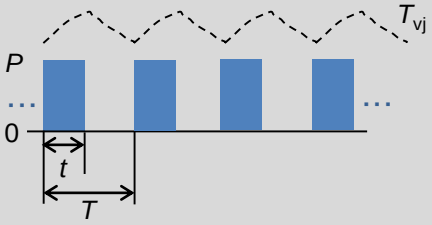
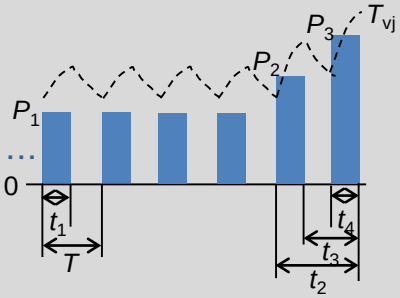
3. Calculation of Junction Temperature

When using a device, it is important that the junction temperature in its used state is within the maximum rating. Therefore, the junction temperature is verified from the operating waveform to confirm whether or not it can be used.

(1) Calculation of junction temperature for forward square wave power loss

Table 4-2 shows the junction temperature calculation formula for continuous loss, single pulse loss, continuous pulse loss, and irregular pulse loss following continuous pulse loss.

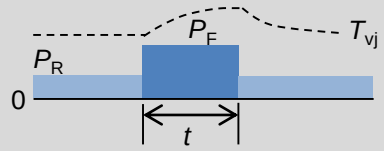
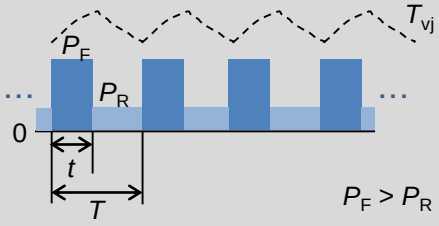
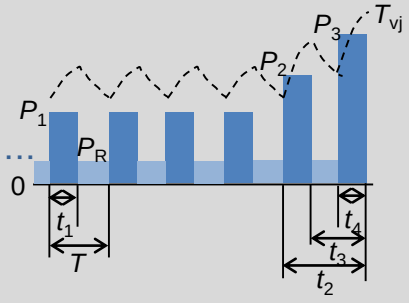
Table 4-2. Junction temperature calculation formula

Loads	Junction temperature calculation formula
Continuous Loss Dashed line is junction temperature 	$T_{vj} = T_c + P \times R_{th(j-c)}$
Single Pulse Loss 	$T_{vj} = T_c + P \times Z_{th(t)}$
Continuous Pulse Loss 	$T_{vj} = T_c + P \times \frac{t}{T} \times R_{th(j-c)}$ $+P \times \left(1 - \frac{t}{T}\right) \times Z_{th}(t+T)$ $-P \times Z_{th}(T)$ $+P \times Z_{th}(t)$
Irregular Pulse Loss following Continuous Pulse Loss 	$T_{vj} = T_c + P_1 \times \frac{t_1}{T} \times R_{th(j-c)}$ $+P_1 \times \left(1 - \frac{t_1}{T}\right) \times Z_{th}(t_1+T)$ $-P_1 \times Z_{th}(T)$ $+P_2 \times Z_{th}(t_2)$ $-P_2 \times Z_{th}(t_3)$ $+P_3 \times Z_{th}(t_4)$

(2) Calculation of junction temperature with reverse power loss

Table 4-3 shows the junction temperature calculation formula when the power loss due to the reverse current by the reverse voltage is added.

Table 4-3. Formula for calculating junction temperature with reverse loss added

Loads	Junction temperature calculation formula
Single Pulse Loss 	$T_{vj} = T_c + (P_F - P_R) \times Z_{th(t)}$ $+P_R \times R_{th(j-c)}$
Continuous Pulse Loss 	$T_{vj} = T_c + (P_F - P_R) \times \frac{t}{T} \times R_{th(j-c)}$ $+(P_F - P_R) \times \left(1 - \frac{t}{T}\right) \times Z_{th}(t+T)$ $-(P_F - P_R) \times Z_{th}(T)$ $+(P_F - P_R) \times Z_{th}(t)$ $+P_R \times R_{th(j-c)}$
Irregular Pulse Loss following Continuous Pulse Loss 	$T_{vj} = T_c + (P_1 - P_R) \times \frac{t_1}{T} \times R_{th(j-c)}$ $+(P_1 - P_R) \times \left(1 - \frac{t_1}{T}\right) \times Z_{th}(t_1+T)$ $-(P_1 - P_R) \times Z_{th}(T)$ $+(P_2 - P_R) \times Z_{th}(t_2)$ $-(P_2 - P_R) \times Z_{th}(t_3)$ $+(P_3 - P_R) \times Z_{th}(t_4)$ $+P_R \times R_{th(j-c)}$

(3) Calculation of junction temperature

To calculate the junction temperature of the device, the following is required.

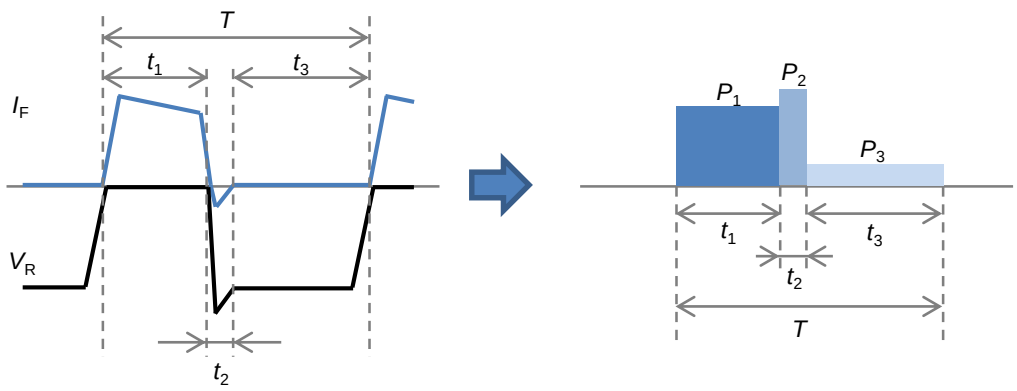
(a) Waveform of one cycle (V_R, I_F and period T can be known)

(b) Enlargement of waveform during reverse recovery

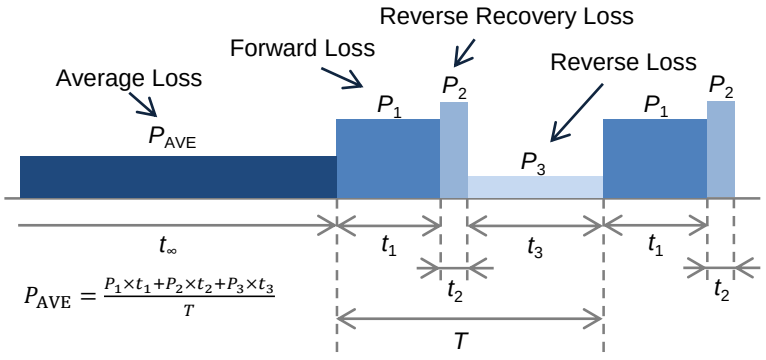
(c) Operating conditions (case temperature T_c, etc.)

The steps for calculating the junction temperature are shown below.

① Obtain the pulse loss of one cycle from the operating waveform



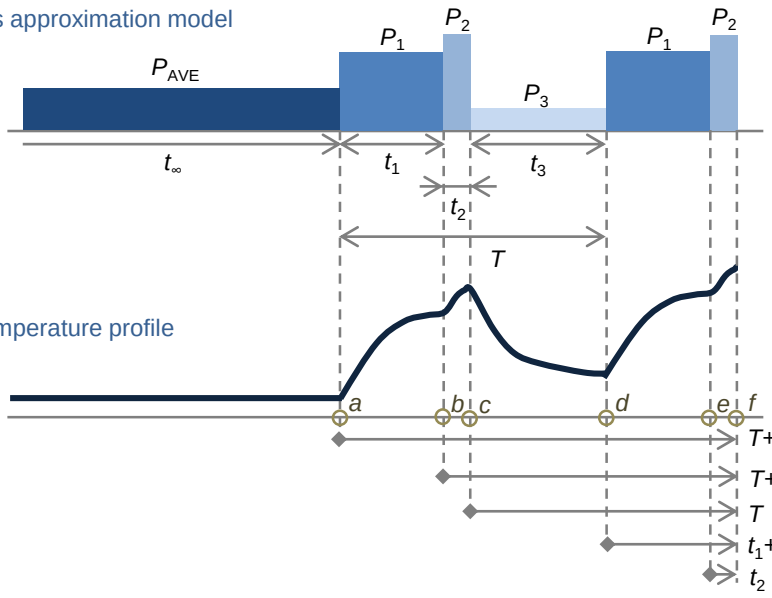
② Loss model approximation



※ This loss model approximation is for the case where the junction temperature is the maximum value at the reverse recovery loss P_2

③ Calculation of junction temperature rise

Loss approximation model



Temperature profile

Junction temperature rise calculation formula

$$\begin{aligned}\Delta T_{\mathrm{j-c}}[\mathrm{degree}] = {} & P_{\mathrm{AVE}} \times R_{\mathrm{th(j-c)}} \\ & -P_{\mathrm{AVE}} \times Z_{\mathrm{th}}(T+t_1+t_2) + P_1 \times Z_{\mathrm{th}}(T+t_1+t_2) \\ & -P_1 \times Z_{\mathrm{th}}(T+t_2) + P_2 \times Z_{\mathrm{th}}(T+t_2) \\ & -P_2 \times Z_{\mathrm{th}}(T) + P_3 \times Z_{\mathrm{th}}(T) \\ & -P_3 \times Z_{\mathrm{th}}(t_1+t_2) + P_1 \times Z_{\mathrm{th}}(t_1+t_2) \\ & -P_1 \times Z_{\mathrm{th}}(t_2) + P_2 \times Z_{\mathrm{th}}(t_2)\end{aligned}$$

$P_{\mathrm{AVE}} \times R_{\mathrm{th(j-c)}}$ ··· Temperature rise up to time *a*

$-P_{\mathrm{AVE}} \times Z_{\mathrm{th}}(T+t_1+t_2) + P_1 \times Z_{\mathrm{th}}(T+t_1+t_2)$ ··· Temperature drop and rise from time *a* to *f*

$-P_1 \times Z_{\mathrm{th}}(T+t_2) + P_2 \times Z_{\mathrm{th}}(T+t_2)$ ··· Temperature drop and rise from time *b* to *f*

$-P_2 \times Z_{\mathrm{th}}(T) + P_3 \times Z_{\mathrm{th}}(T)$ ··· Temperature drop and rise from time *c* to *f*

$-P_3 \times Z_{\mathrm{th}}(t_1+t_2) + P_1 \times Z_{\mathrm{th}}(t_1+t_2)$ ··· Temperature drop and rise from time *d* to *f*

$-P_1 \times Z_{\mathrm{th}}(t_2) + P_2 \times Z_{\mathrm{th}}(t_2)$ ··· Temperature drop and rise from time *e* to *f*

Chapter 5 Precautions for Design

1.	Parallel Connection of SiC-SBD	5-2
2.	Series Connection of SiC-SBD ＜Not Recommended＞	5-2
3.	Surge current and temperature derating	5-2
4.	Surge voltage protection	5-4

1. Parallel Connection of SiC-SBD

For SiC-SBD, the Forward Voltage V_F also rises as the junction temperature rises. Therefore, when used in parallel connection, the Forward Current is balanced between the SiC-SBD connected in parallel due to this temperature characteristic. However, when actually using it, consider the following precautions for parallel connection, such as characteristic variations and mounting effects.

① When connecting in parallel, use products of the same lot.
② Mount so that there is no difference in temperature between the devices connected in parallel.
③ Wiring so that the current flows evenly.
④ Select the current rating in consideration of the case where the current is not balanced.

In addition to the above precautions, please check the actual equipment sufficiently.

2. Series Connection of SiC-SBD ＜Not Recommended＞

When SiC-SBDs are connected in series, the reverse voltage applied to each SiC-SBD differs depending on the Total capacitance *C* and Reverse Current I_R. It is supposed that the reverse voltage balance of each SiC-SBD will be momentarily lost due to the deviation of the operation during reverse recovery such as switching. Due to the above, we do not recommend connecting SiC-SBD in series.

3. Surge current and temperature derating

Forward surge current I_{FSM} is defined as the maximum value of non-repeating surge forward current in a commercial frequency sinusoidal half cycle (t_p = 10ms). However, in most of the circuits that are actually used, currents other than this definition flow. Therefore, it is necessary to calculate I_{FSM} according to the actual usage conditions (pulse width, temperature).

I_{FSM} is expressed by the current squared time product I^2t in the region where the pulse width t_p is 1ms or more. The I_{FSM} at any pulse width can be obtained from the relational expression between I_{FSM} and I^2t shown below. Figure 5-1 shows a calculation example of FDC2AT10S65.

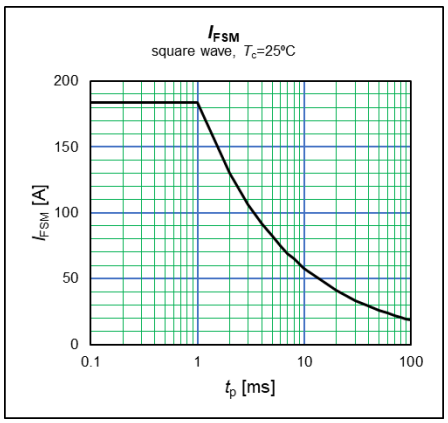
For temperature derating, create a temperature derating curve from the relationship between I_{FSM} of T_c = 25ºC and T_c = 150ºC. Figure 5-2 shows a calculation example of FDC2AT10S65. Please check the data sheet of the product to be used and create the temperature derating.

Relational expression between I_{FSM} (sine wave half cycle with width 10ms) and I^2t

$$\left(I_{\mathrm{FSM}} \div \sqrt{2}\right)^2 \times t_{\mathrm{p}} = I^2t\ [\mathrm{A^2s}] \qquad t_{\mathrm{p}} = 10\ [\mathrm{ms}]$$

I_{FSM} at any pulse width t_p

$$\sqrt{I^2t \div t_{\mathrm{p}}} = I_{\mathrm{FSM}(t_{\mathrm{p}})}\ [\mathrm{A}] \qquad t_{\mathrm{p}} \geq 1\ [\mathrm{ms}]$$



I_{FSM} curve at T_c = 25ºC

Calculate the I_{FSM} of FDC2AT10S65 as an example. From the data sheet of FDC2AT10S65, I^2t at T_c = 25ºC is 33.6A²s. If you calculate I_{FSM} at t_p = 1ms using the relational expression on the previous page, it will be 183.3A.

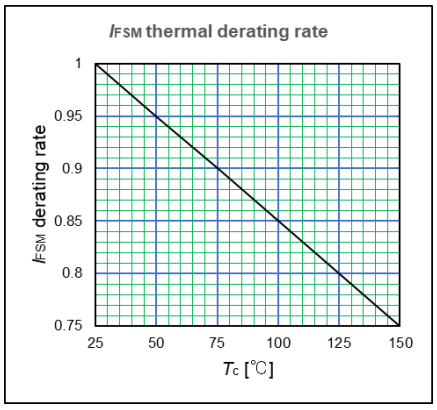
I_{FSM} at T_c=25ºC, t_p=1ms

$$\sqrt{I^2t \div t_p} = I_{FSM(t_p)}[\mathrm{A}]$$

$$\sqrt{33.6 \div 0.001} = 183.3[\mathrm{A}]$$

The graph on the left shows the I_{FSM} curve with t_p of 0.1ms ~ 100ms created using the relational expression.

Figure 5-1. I_{FSM} calculation example of FDC2AT10S65



From the FDC2AT10S65 data sheet, the I_{FSM} at T_c = 25ºC is 82A and the I_{FSM} at T_c=150ºC is 61.5A. The graph on the left shows the temperature derating created from these ratios.

$$\frac{I_{FSM}(T_c = 150°\mathrm{C})}{I_{FSM}(T_c = 25°\mathrm{C})} = \frac{61.5[\mathrm{A}]}{82[\mathrm{A}]} = 0.75$$

Figure 5-2. I_{FSM} temperature derating of FDC2AT10S65

4. Surge voltage protection

Power devices generate surge voltage when the current is cut off, and overvoltage may destroy the device. For example, in the boost converter shown in Fig. 5-3, the MOSFET turns on from the state where the forward current is flowing in the SiC-SBD, the current flows in the MOSFET, and the SiC-SBD operates in reverse recovery. The surge voltage of SiC-SBD is generated by inducing a voltage in the wiring inductance due to a sudden change in the main circuit current. Figure 5-4 shows a typical MOSFET turn-on waveform and Diode reverse recovery waveform. If this surge voltage V_{PEAK} exceeds V_{RRM}, it will become overvoltage and may destroy.

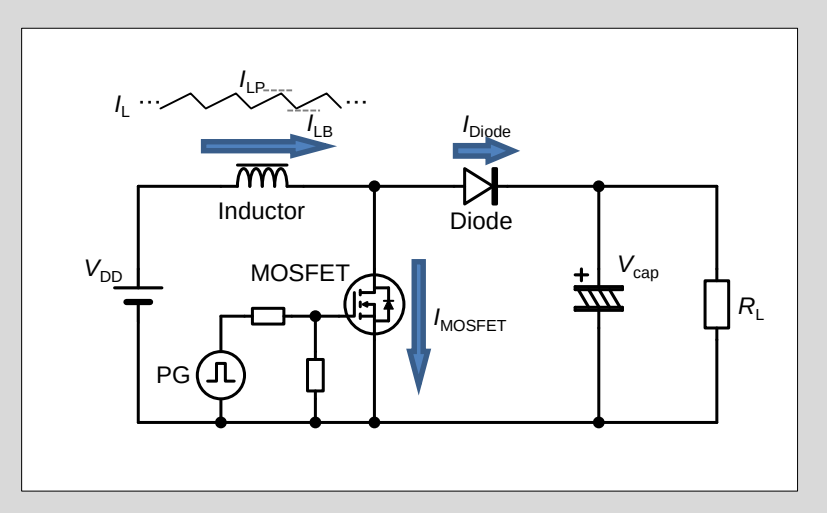
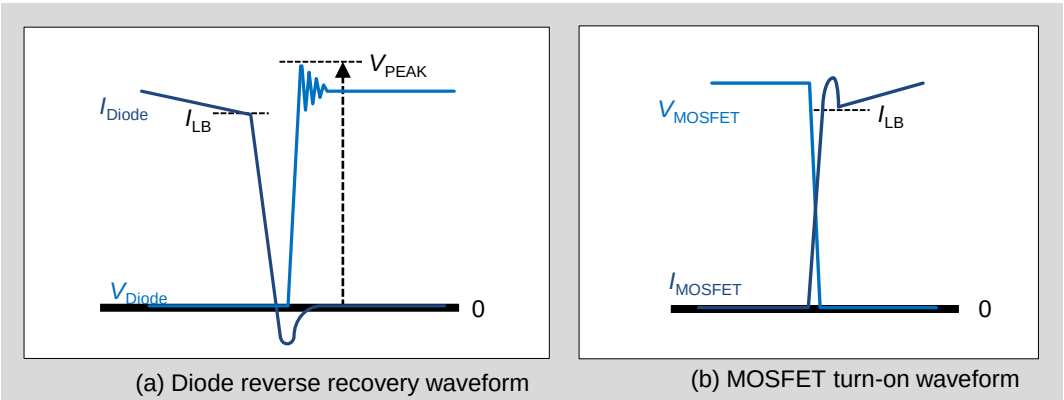


Figure 5-3. Boost converter circuit



(a) Diode reverse recovery waveform (b) MOSFET turn-on waveform

Figure 5-4. Diode reverse recovery waveform and MOSFET turn-on waveform

＜ Surge voltage suppression method ＞

The method for suppressing the surge voltage is shown below.

(a) Connect a Snubber to the SiC-SBD

Mount the Snubber near the terminal of the SiC-SBD in order to reduce the influence of wiring inductance.

(b) Adjustment of main circuit wiring

Surge voltage can be suppressed by shortening the wiring and widening the cross-sectional area to reduce the inductance.

Chapter 6 Precautions for Mounting and Handling

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3.	Cleaning	6-6
4.	Mounting to Heat Sink	6-6
5.	Storage	6-7
6.	Transportation	6-8
7.	Working Environment	6-8

This chapter describes handling precautions that require special attention in order to ensure stable operation over a long period of time.

1. Soldering

When soldering a product, heat is applied to the leads that exceeds the absolute maximum rating of storage temperature. The quality assurance regarding heat resistance during soldering is confirmed under the conditions described below (Table 6-1, Table 6-2, Table 6-3, Fig. 6-1, Fig. 6-2). , Please solder within the range.

◆The immersion depth of the terminal should be 1.5 mm away from the package.
◆Be careful not to immerse the product in the soldering liquid when mounting the device by the solder flow method.
◆When using flux, it is desirable to use rosin-based flux, and not chlorine-based flux.

Table 6-1. Recommended mounting condition

Category	Packege	Soldering Methods				
		Wave Soldering (Full dipping)	Wave Soldering (Only terminal)	Infrared Reflow	Air Reflow	Soldering iron (Re-work)
Through hole package	TO-220	U	P2	U	U	P1
	TO-220-2	U	P2	U	U	P1
	TO-220F	U	P2	U	U	P1
	TO-220F-2	U	P2	U	U	P1
	TO-247	U	P2	U	U	P1
	TO-247-2	U	P2	U	U	P1
Surface Mount Package	T-Pack(S)	U	U	P2	P2	U

P2: Possible (within 2 times) P1: Possible (Only 1 time) U: Unable

Table 6-2. Soldering condition of Through-Hole Package

Methods	Soldering Temp.	Immersion time
Wave Soldering	260±5ºC	10±1sec
Soldering iron(Re-work)	350±10ºC	3.5±0.5 sec

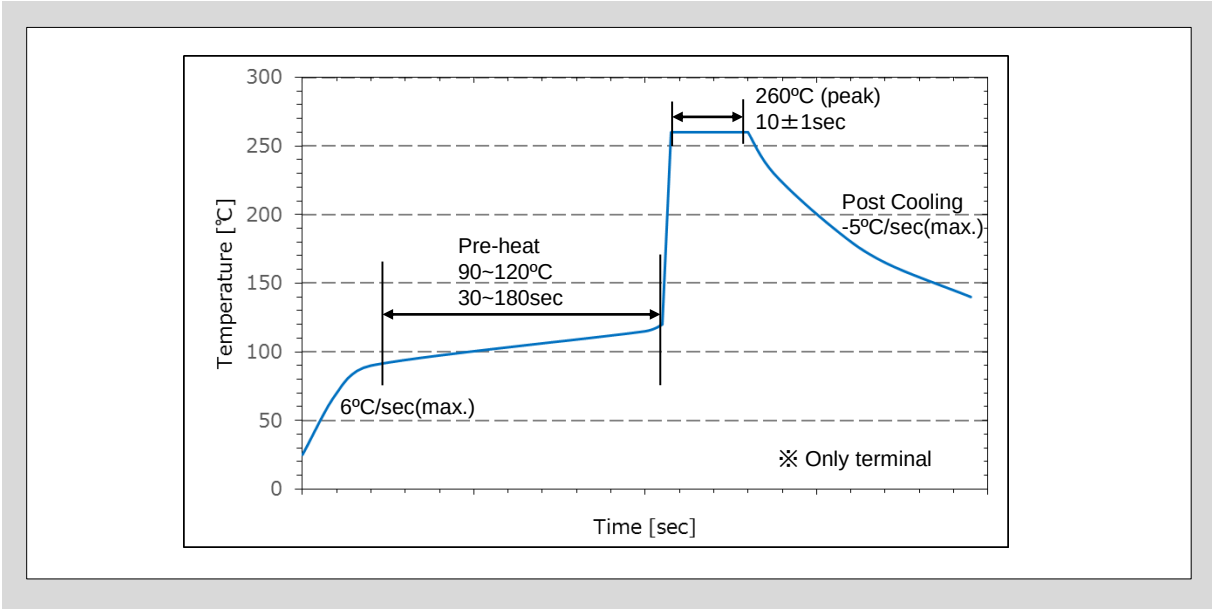

Figure 6-1. Recommended Flow profile

Table 6-3. Soldering condition of Surface Mount Package

Number of times(Reflow)	Soldering temp. & Time	Package surface Peak temp. & Time
Twice	≥ 23ºC ≤ 50sec	≤ 26ºC ≤ 10sec

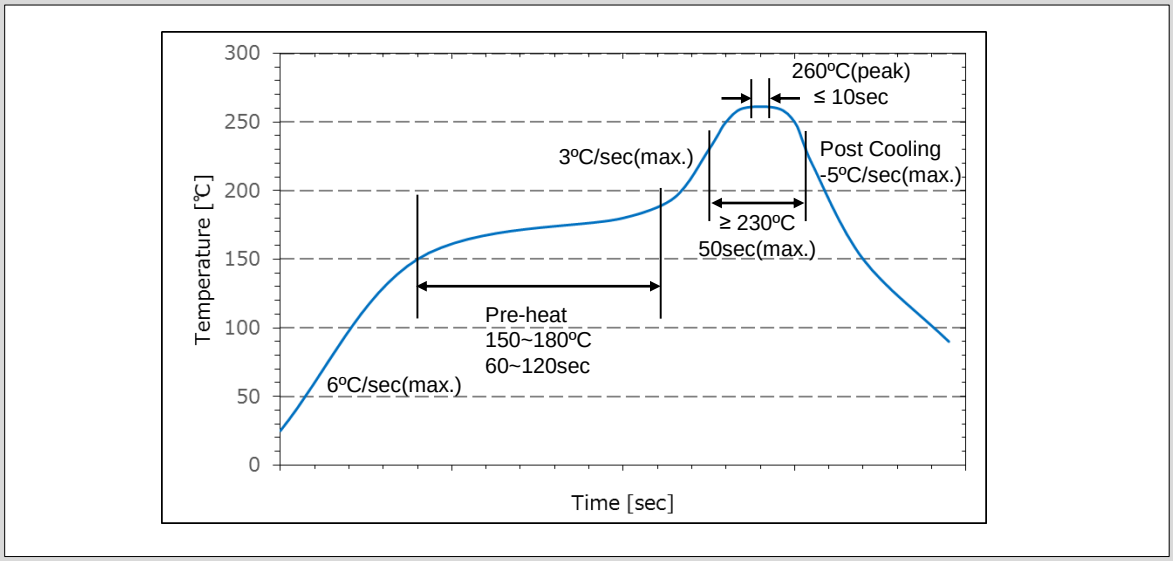

Figure 6-2. Recommended Reflow profile

2. Processing and Mounting of Through Hole Terminal

(a) Stress to the terminals

Applying unnecessary stress to the terminals will damage the internal chip and external package. The load applied in the direction shown in Fig. 6-3 should be 1 kg or less.

(b) Cautions in forming terminals

If there is no other choice but to forming terminals for convenience of parts layout, pay attention to the following:

◆Use special jigs that does not put stress on the internal chip and external package, as shown in Figure 6-3.

◆When bending the terminal in the horizontal direction, bend it at a distance of 4mm or more away from the package, and keep the bending angle within 30º (Fig.6-3).

◆When bending the terminal at right angle against the package, bend it at a point that is at least 4mm or more away from the package.

◆Forming should be performed only once at a place, and do not perform re-forming or restore to the original shape.

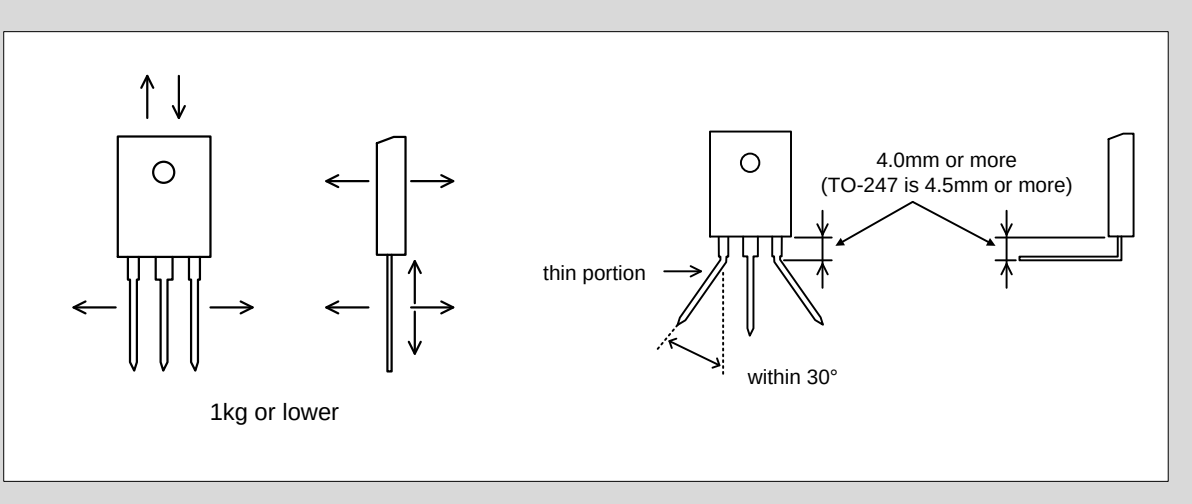

Figure 6-3.Recommended forming terminals

(c) Insertion into printed circuit board

When inserting terminals into printed circuit board, coincide the distance between terminals and that of insertion holes to prevent excessive stress from being applied to the base of the terminals. Also, it should be avoided to attach to heat sink after soldering so that terminal will not be bent forcibly. Be sure to attach in advance before soldering.

3. Cleaning

When soldering is performed with using flux, cleaning with solvent is required. In this case, pay attention to the following :

(a) Solvent

◆Do not use flammable, toxic, and corrosive solvent.

◆Never use trichloroethylene series solvent because it contains chlorine.

(b) Cleaning method

Soaking is recommended. When conducting ultrasonic cleaning, set the frequency to avoid the resonance point (several tens of kHz), and be careful not to let the device or printed circuit board to come into contact with the oscillation source directly.

4. Mounting to Heat Sink

When mounting to a heat sink, if the screw torque is too small, the thermal resistance will increase, and if it is too large, excessive stress will be applied to the product, which may lead to product destruction. Set the tightening torque within the appropriate range shown in Table 6-4. The flatness of the heat sink should be ± 30 μm or less, and the surface roughness should be ± 10 μm or less.

Incorrect handling such as taper processing of the attached hole may cause dielectric breakdown such as package cracking, which may lead to a serious accident.

Table 6-4. Tightening torque

Packages	Screw	Tightening torques	Note
TO-220 TO-220-2 TO-220F TO-220F-2	M3	30 – 50 N･cm	Flatness : ≤ ±30μm Roughness : ≤ 10μm Plane off the edge : C ≤ 1.0mm
TO-247 TO-247-2	M3	40 – 60 N･cm	

Applying thermal compound

It is recommended to use heat conductive grease such as thermal compound to enhance the heat dissipation effect. As a method of filling the gap between the device and the heat sink with a compound, as shown in Fig. 6-4, apply an appropriate amount of compound in dots on the case part directly under the semiconductor element chip mounting part, and screw the heat sink with an appropriate tightening torque. When tightened, the compound spreads to fill the gap, making it easy to form a layer with few bubbles.

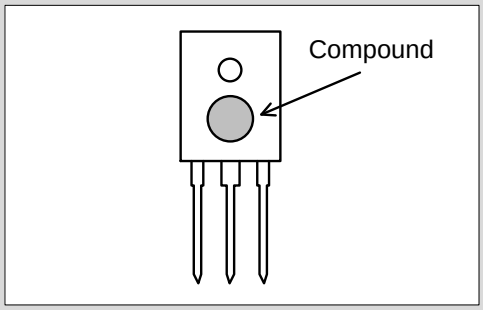

Figure 6-4. Thermal compound application

5. Storage

Table 6-5 shows the precautions for storage.

Table 6-5. Storage precautions

i	It is desirable that devices be stored in a place of normal temperature and humidity. Temperature and humidity are approximately 5 to 35ºC and 45 to 75%, respectively. When storing molded type power transistors in area that becomes extremely dry in winter, humidification by a humidifier is required. If tap water is used for humidification, chlorine contained in it may cause corrosion of the terminals of the device. To prevent this, use pure water or boiled water for humidification.
ii	Avoid storing devices in a place where corrosive gas is generated or subjected to much dust.
iii	Avoid storing devices in a place subjected to sharp temperature change. Otherwise condensation may occur to the devices. Store the devices in a place having min. temperature change.
iv	Pay attention not to apply load to devices during storage. In particular, if they are stored, stacked on top of each other, unexpected load may be applied. Also, avoid placing heavy objects on top.
v	Store the devices with each terminal unprocessed to avoid occurrence of corrosion, which may result in soldering defect at the time of processing.
vi	Store the devices in containers that is not affected by static electricity easily, or the one used for the delivery of the product.
vii	All storage shelves should be made of metal. Be sure to ground them.
viii	The storage period is one year after delivery in the above storage and packaging state.

6. Transportation

Table 6-6 shows the precautions for transportation.

Table 6-6. Transportation precautions

i	Be careful not to cause impact on the devices such as dropping them, etc.
ii	When transporting large number of devices in boxes, arrange the devices by using soft spacers to prevent the contact electrode surface, etc. from being damaged, shown in Figure 6-5.
iii	Take measures against static electricity by using conductive bags or aluminum foil to prevent static electricity being applied to A-C terminals, shown in Figure 6-6.
iv	When transporting stick-packed products, be careful not to expose them to high temperatures. The stick may be deformed if it is exposed to direct sunlight or left in the car.

Figure 6-5. Conductive foam

Figure 6-6. Conductive bag and aluminum foil

7. Working Environment

Table 6-7 shows the precautions for the working environment.

Table 6-7. Working Environment precautions

i	The person who handles the Diode should use ground their body. Wear a wrist strap, copper ring, etc., attach a resistor of approximately 1MΩ, and ground it to prevent electric shock.
ii	At the working environment, lay a conductive floor mat or tablemat, etc. and ground it.
iii	When using measuring devices such as curve tracer, ground the measuring devices as well.
iv	When soldering, ground the solder bath to prevent the leakage voltage from the soldering iron or bath being applied to the Diode.