Chapter 7

Gate Drive circuit Design

CONTENTS

This section explains the drive circuit design.

In order to maximaize the performance of an IGBT, it is important to properly set the drive circuit constants

1 IGBT drive conditions and main characteristics

IGBT drive conditions and main characteristics are shown below. An IGBT's main characteristics change according to the values of VGE and RG, so it is important to use settings appropriate for the intended use of the equipment in which it will be installed.

Table 7-1 IGBT drive conditions and main characteristics

Main characteristics	$+V_{GE}$ rise	$-V_{GE}$ rise	$R_{G(ON)}$ rise	$R_{G(oFF)}$ rise
$V_{CE(sat)}$	Fall	-	-	-
t_{on} E_{on}	Fall	-	Rise	-
t_{off} E_{off}	-	Fall	Rise	Rise
Turn-on surge voltage	Rise	-	Fall	-
Turn-off surge voltage	-	Rise	-	Fall *1
dv/dt malfunction	Rise	Fall	Fall	Fall
Current limit value	Rise	-	-	-
Short circuit withstand capability	Fall	-	-	-
Radiational EMI noise	Rise	-	Fall	Fall

*1: Dependence of surge voltage on gate resistance is different for each series

1.1 $+V_{GE}$ (On state)

A recommended the gate on state voltage value (+ V_{GE}) is +15V. Notes when + V_{GE} is designed are shown as follows.

(1) Set $+V_{GE}$ so that is remains under the maximum rated G-E voltage, V_{GES} =±20V.
(2) It is recommended that supply voltage fluctuations are kept to within ±10%.
(3) The on-state C-E saturation voltage $V_{GE(sat)}$ is inversely dependent on $+V_{GE}$, so the greater the $+V_{GE}$ the smaller the $V_{GE(sat)}$.
(4) Turn-on switching time and switching loss grow smaller as $+V_{GE}$ rises.
(5) At turn-on (at FWD reverse recovery), the higher the $+V_{GE}$ the greater the likelihood of surge voltages in opposing arms.
(6) Even while the IGBT is in the off-state, there may be malfunctions caused by the dv/dt of the FWD's reverse recovery and a pulse collector current may cause unnecessary heat generation. This phenomenon is called a dv/dt shoot through and becomes more likely to occur as $+V_{GE}$ rises.
(7) In V and U series IGBTs, the higher the $+V_{GE}$, the higher the current limit becomes.
(8) The greater the $+V_{GE}$ the smaller the short circuit withstand capability.

1.2 $-V_{GE}$ (Off state)

A recommended the gate reverse bias voltage value ($-V_{GE}$) is –5 to -15V. Notes when $-V_{GE}$ is designed are shown as follows.

(1) Set $-V_{GE}$ so that it remains under the maximum rated G-E voltage, V_{GES} =±20V .
(2) It is recommended that supply voltage fluctuations are kept to within ±10%.
(3) IGBT turn-off characteristics are heavily dependent on $-V_{GE}$, especially when the collector current is just beginning to switch off. Consequently, the greater the $-V_{GE}$ the shorter, the switching time and the switching loss become smaller.
(4) If the $-V_{GE}$ is too small, dv/dt shoot through currents may occur, so at least set it to a value greater than –5V. If the gate wiring is long, then it is especially important to pay attention to this.

1.3 R_G (Gate resistance)

Gate resistance R_G listed in the product specification sheets is the value on the condition so as to decrease the switching losses. So, you must select the optimal R_G according to the circuit or operating condition. Notes when R_G is designed are shown as follows.

(1) The switching characteristics of both turn-on and turn-off are dependent on the value of R_G, and therefore the greater the R_G the longer the longer the switching time and the greater the switching loss. Also, as R_G increases, the surge voltage during switching becomes smaller.
(2) The greater the R_G the more unlikely a dv/dt shoot through current becomes.
(3) Various switching characteristics are varied for stray inductance. Especially, spike voltages when IGBTs are turned off or FWDs are recovered reversibly are influenced on the stray inductance. Therefore, RG need to be designed on the lower stray inductance condition.

Select the most suitable gate drive conditions while paying attention to the above points of interdependence.

1.4 avoid the unexpected turn-on by recovery dv/dt

In this section, the way to avoid the unexpected IGBT turn-on by dv/dt at the FWD's reverse recovery will be described.

Fig.7-1 shows the principle of unexpected turn-on caused by dv/dt at reverse recovery. In this figure, it is assumed that IGBT1 is turned off to on and gate to emitter voltage V_{GE} of IGBT2 is negative biased. In this condition, when IGBT1 get turned on from off-state, FWD on its opposite arm, that is, reverse recovery of FWD2 is occurred. At same time, voltage of IGBT2 and FWD2 with off-state is raised. This causes the dV/dt according to switching time of IGBT1.

Because IGBT1 and 2 have the mirror capacitance C_{GC}, Current is generated by dV/dt through C_{GC}. This current is expressed by C_{GC} x dV/dt. This current is flowed through the gate resistance R_G, results in increasing the gate potential. So, V_{GE} is generated between gate to emitter. If V_{GE} is excess the sum of reverse biased

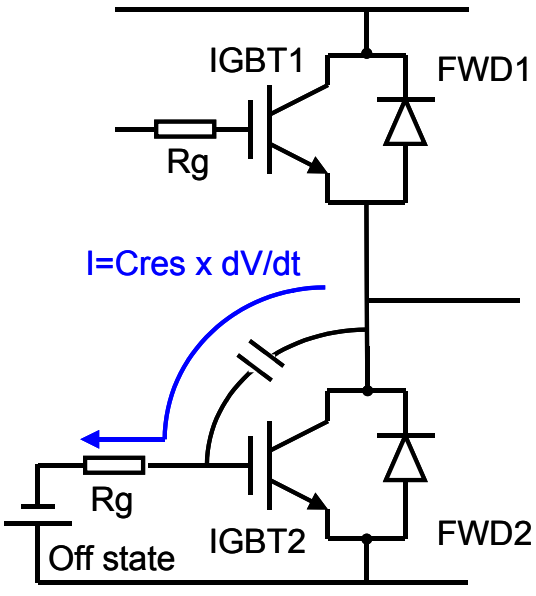
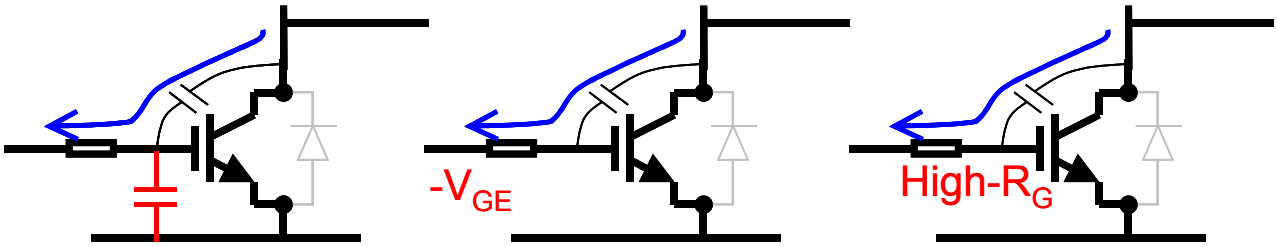


Fig.7-1 Principle of unexpected turn-on

voltage and V_{GE}(th), IGBT2 is turned on. Once IGBT2 is turned on, the short-circuit condition is happened, because both IGBT1 and 2 is under turned-on state.

From this principle, the methods to avoid the unexpected turn-on are shown in Fig.7-0-2. There are three methods, which are the C_{GE} addition, increase of reverse bias voltage and increase of R_G.



(a) additional Cge (b) increase of -Vge (c) increase of RG

Fig. 7-2 Methods to avoid unexpected turn-on

The method to add the C_{GE} is the way to the decrease of unexpected turn-on current by sharing to C_{GE}. Sharing current charges and/or discharges the additional CGE. In order to charge and/or discharge the additional CGE, switching speed gets lower. Just only adding the CGE results in the increase switching losses. However, lower Rg adding CGE at the same time can control switching speed. In other words, both adding the CGE and decreasing the RG can avoid the unexpected turn-on without increasing switching losses.

Driving higher R_G can decrease dV/dt, results in soft-switching. However, it has the disadvantage of increase switching losses as well. Moreover, although the method to enlarge the reverse bias is also effective to avoid the unexpected turn-on, the quantity of the gate charge becomes larger.

From these viewpoints, adding the C_{GE} is recommended to avoid unexpected turn-on. Recommended C_{GE} is two times value on the specification sheet and Recommended R_G is the half before adding C_{GE}. In this case, you must confirm the various characteristics.

2 Drive current

Since an IGBT has a MOS gate structure, to charge and discharge this gate when switching, it is necessary to make gate current (drive current) flow. Fig.7-3 shows the gate charge (dynamic input) characteristics. These gate charge dynamic input characteristics show the electric load necessary to drive the IGBT and are used to calculate values like average drive voltage and the driving electric power. Fig.7-4 shows the circuit schematic as well as the voltage and current waveforms. In principle, a drive circuit has a forward bias power supply alternately switching back and forth using switch S_1 and S_2. During this switching, the current used to charge and discharge the gate, is the driven current. In Fig. 7-4, the area showing the current waveform (the hatched area) is equivalent to the gate charge from Fig.7-3.

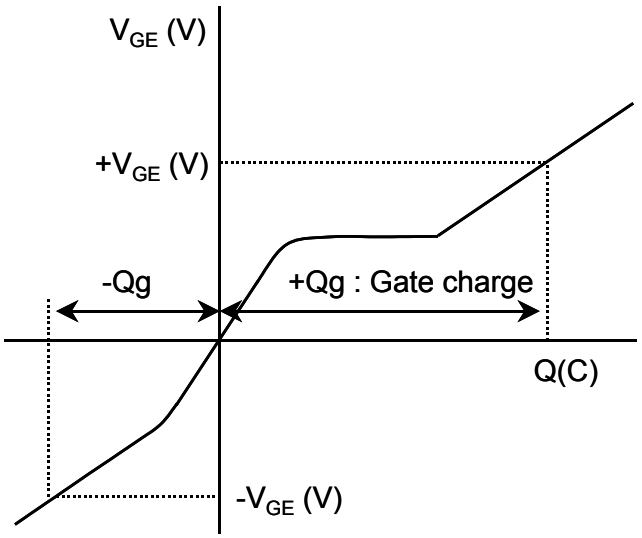


Fig. 7-3 Schematic waveform of gate charge characteristics (Dynamic input characteristics).

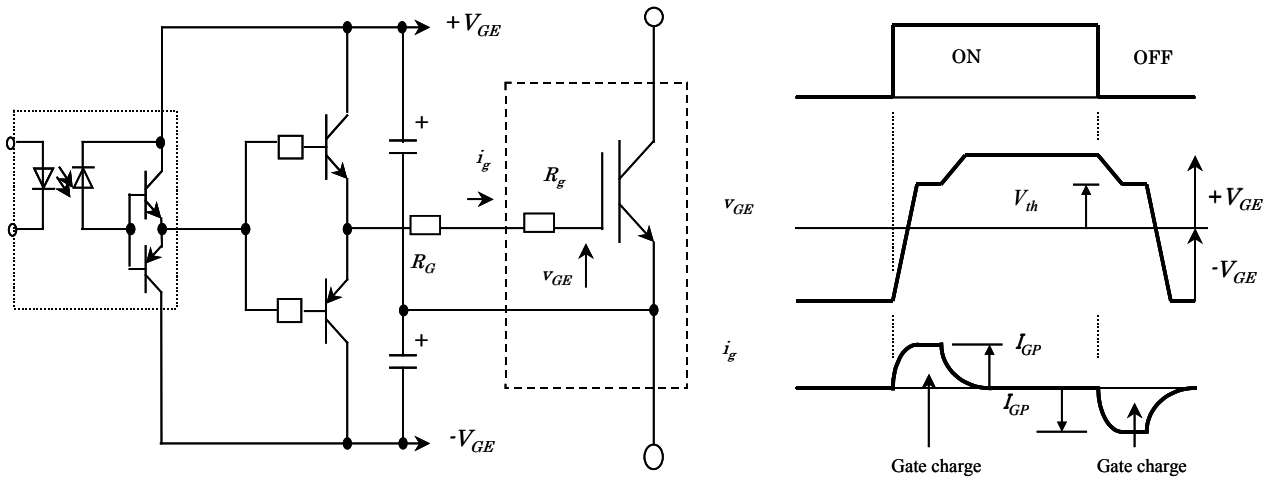


Fig. 7-4 Drive circuit schematic as well as voltage and current waveforms.

The drive current peak value I_{GP} can be approximately calculated as follows:

$$I_{GP} = \frac{+V_{GE} + |-V_{GE}|}{R_G + R_g}$$

$+V_{GE}$: Forward bias supply voltage
$-V_{GE}$: Reverse bias supply voltage
R_G : Drive circuit gate resistance
R_g : Module's internal resistance

Internal gate resistance Rg is various for each typename or series. Therefore, refer to application manual for application manual or technical data.

On the there hand, the average value of the drive current I_G, using the gate charge characteristics (Fig.7-3), can be calculated as follows:

$$+I_G = -I_G = fc \times \left(|+Q_g| + |-Q_g| \right)$$

fc : Carrier frequency
Q_g : Gate charge from 0V to $+V_{GE}$
$-Q_g$: Gate charge from $-V_{GE}$ to 0V

Consequently, it is important to set the output stage of the drive circuit in order to conduct this approximate current flow (I_{GP}, as well as $\pm I_G$).

Furthermore, if the power dissipation loss of the drive circuit is completely consumed by the gate resistance, then the drive power (Pd) necessary to drive the IGBT is shown in the following formula:

$$Pd(on) = fc \bullet \left[\frac{1}{2} \left(|+Q_g| + |-Q_g| \right) \bullet \left(|+V_{GE}| + |-V_{GE}| \right) \right]$$

$$Pd(off) = Pd(on)$$

$$Pd = Pd(off) + Pd(on)$$

$$= fc \bullet \left(|+Q_g| + |-Q_g| \right) \bullet \left(|+V_{GE}| + |-V_{GE}| \right)$$

Accordingly, a gate resistance is necessary that can charge this approximate capacity.

Be sure to design the drive circuit so that the above-mentioned drive current and drive power can be properly supplied.

3 Setting dead-time

For inverter circuits and the like, it is necessary to set an on-off timing “delay” (dead time) in order to prevent short circuits. During the dead time, both the upper and lower arms are in the “off” state. Basically, the dead time (see Fig.7-5) needs to be set longer than the IGBT switching time (toff max.).

For example, if RG is increased, switching time also becomes longer, so it would be necessary to lengthen dead time as well. Also, it is necessary to consider other drive conditions and the temperature characteristics.

It is important to be careful with dead times that are too short, because in the event of a short circuit in the upper or lower arms, the heat generated by the short circuit current may destroy the module.

Therefore, the dead time of more than 3usec would be recommended for IGBT modules. However, appropriate dead time should be settled by the confirmation of practical machine.

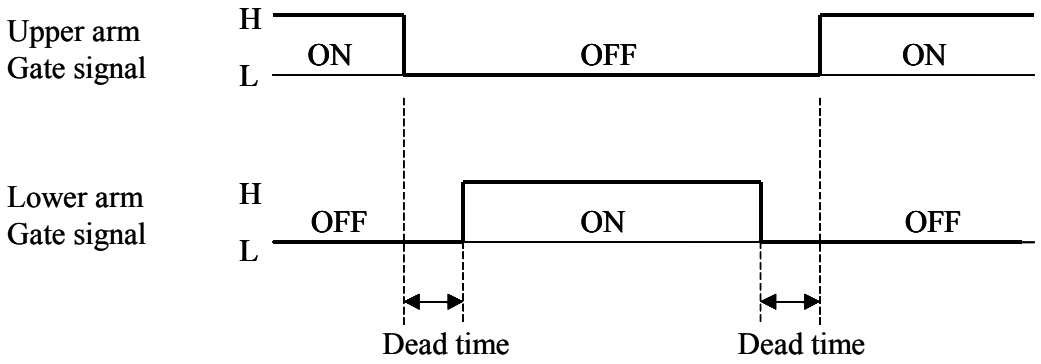
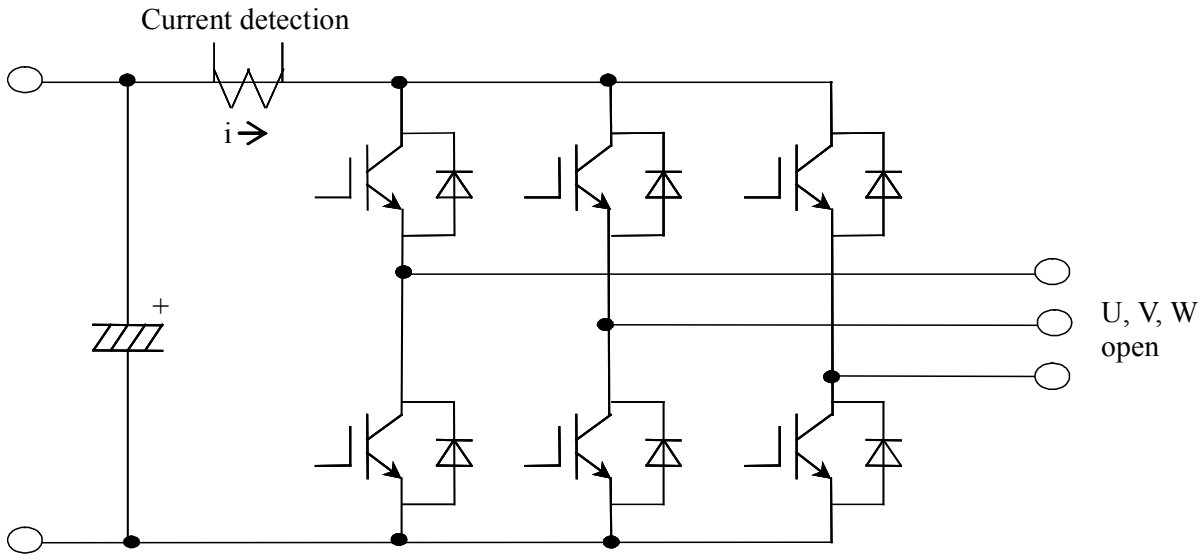


Fig. 7-5 Dead time timing chart.

One method of judging whether or not the dead time setting is sufficient or not, is to check the current of a no-load DC supply line.

In the case of a 3-phase inverter (as shown in Fig.7-4), set the inverter's outputs to open, then apply a normal input signal, and finally measures the DC line current. A very small pulse current (dv/dt current leaving out the module's Miller Capacitance: about 5% of the normal rated current) will be observed, even if the dead time is long enough.

However, if the date time is insufficient, then there will be a short circuit current flow much larger than this. In this case, keep increasing the dead time until the short circuit current disappears. Also, for the same reasons stated above, we recommend testing at high temperatures.



Insufficient dead time makes short circuit current much larger than dv/dt current.

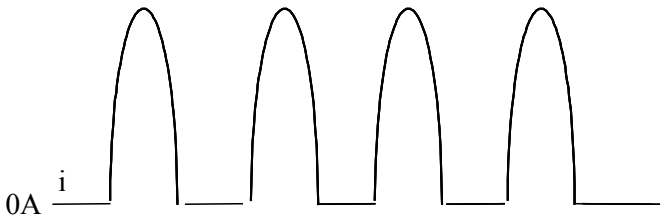


Fig. 7-6 Current detection methods for short circuit cased by insufficient dead time.

4 Concrete examples of drive circuits

For inverter circuits and the like, it is necessary to electrically isolate the IGBT from the control circuit. An example of a drive circuit using this principle, is shown below.

Fig.7-7 shows an example of a drive circuit using a high speed opto-coupler. By using the opto-coupler, the input signal and the module are isolated from each other. Also, since the opto-coupler does not limit the output pulse width, it is suitable for changing pulse widths or PWM controllers, to wide ranges. It is currently the most widely used.

Furthermore, this way the turn-on and turn-off characteristics determined by gate resistance can be set separately, so it commonly used to ensure the best settings.

Aside from the above, there is also a signal isolation method using a pulse transformer. With this method the signal as well as the gate drive power can both be supplied simultaneously from the signal side, thereby allowing circuit simplification. However, this method has the limitations of an on/(off+on) time ratio of max. 50%, and reverse bias cannot be set, so its usefulness as a control method and switching frequency regulator is limited.

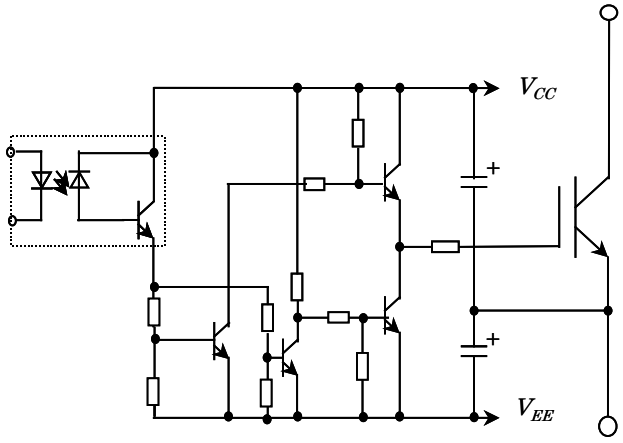


Fig. 7-7 Example of drive circuit using high speed opto-coupler.

5 Drive circuit setting and actual implementation

5.1 Opto-coupler noise ruggedness

As IGBTs are high speed switching elements, it is necessary to select a opto-coupler for drive circuit that has a high noise ruggedness (e.g. HCPL4504). Also, to prevent malfunctions, make sure that the wiring from different sides doesn't cross. Furthermore, in order to make full use of the IGBT's a high speed switching capabilities, we recommend using a opto-coupler with a short signal transmission delay.

5.2 Wiring between drive circuit and IGBT

If the wiring between the drive circuit and the IGBT is long, the IGBT may malfunction due to gate signal oscillation or induced noise. A countermeasure for this is shown below in Fig.7-8.

(1) Make the drive circuit wiring as short as possible and finely twist the gate and emitter wiring. (Twist wiring)
(2) Increase RG. However, pay attention to switching time and switching loss.
(3) Separate the gate wiring and IGBT control circuit wiring as much as possible, and set the layout so that they cross each other (in order to avoid mutual induction).
(4) Do not bundle together the gate wiring or other phases.

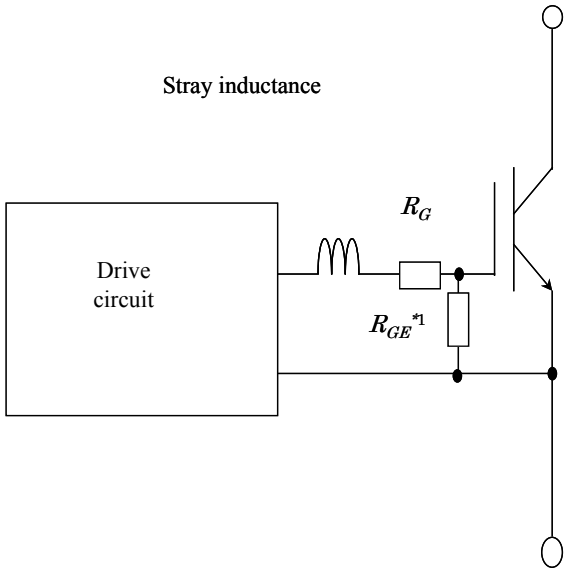


Fig. 7-8 Gate signal oscillation countermeasure

*1 R_{GE}

If the gate circuit is bad or if the gate circuit is not operating (gate in open state)*2 and a voltage is applied to the power circuit, the IGBT may be destroyed. In order to prevent this destruction, we recommend placing a 10kΩ resistance R_{GE} between the gate and emitter.

*2 Switch-on

When powering up, first switch on the gate circuit power supply and then when it is fully operational, switch on the main circuit power supply.

5.3 Gate overvoltage protection

It is necessary that IGBT modules, like other MOS based elements, are sufficiently protected against static electricity. Also, since the G-E absolute maximum rated voltage is ±20V, if there is a possibility that a voltage greater than this may be applied, then as a protective measure it is necessary to connect a zenner diode between the gate and emitter as shown in Fig.7-9.

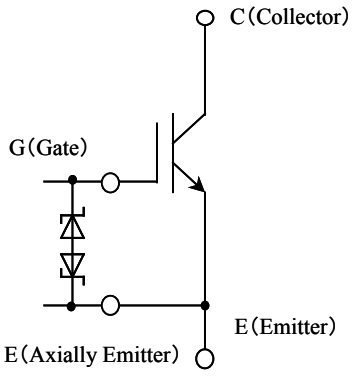


Fig. 7-9 G-E overvoltage protection circuit example.

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