Chapter 5

Recommended wiring and layout

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1. Examples of Application Circuits

In this chapter, a recommended wiring and layout are explained
At first, hints and cautions in design are described with example of application circuit in section 1.

Fig. 5-1 and Fig.5-2 show examples of application circuit, and its Notes.
In these figure, although two method of current sense are shown, these Notes are common.

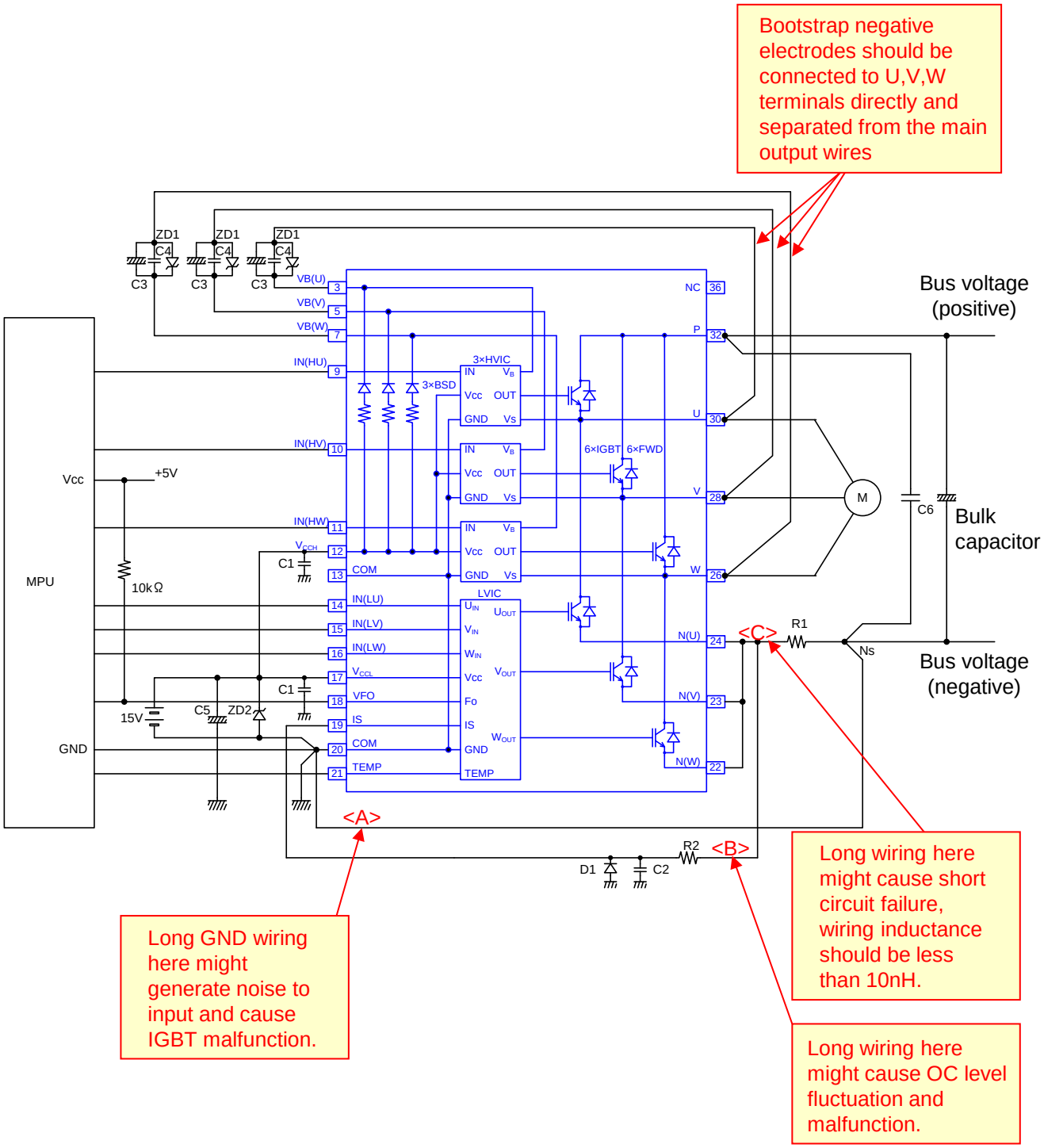


Fig. 5-1 Example of application circuit
(Sensing currents at once with 1 shunt resistor)

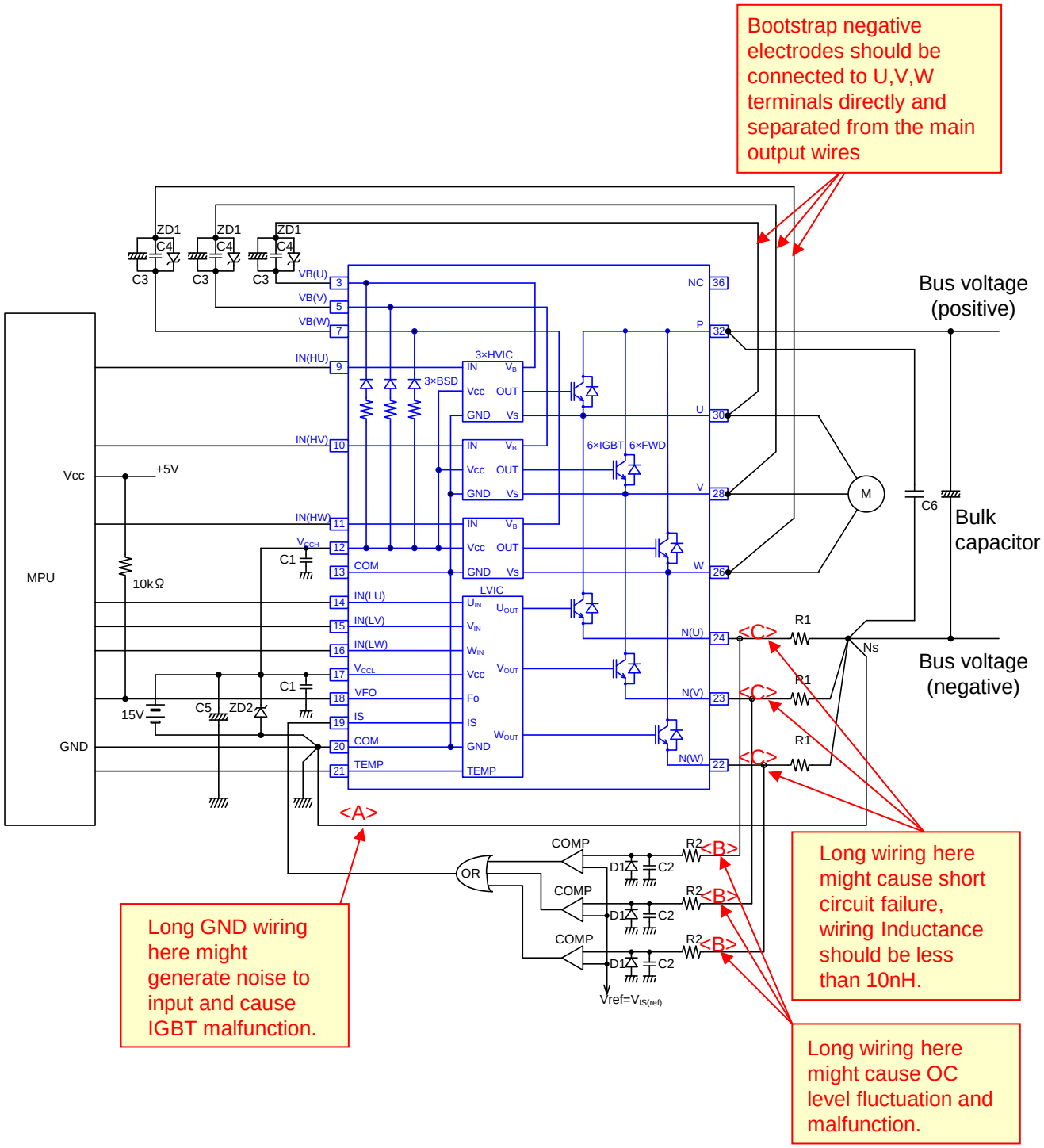


Fig. 5-2 Another example of application circuit
(Sensing currents of each phase using external protection circuit)

<Note>

1. Input signal for IGBT driving is High-Active. The input circuit of the IC has a built-in pull-down resistor. To prevent a malfunction, the wiring of each input should be as short as possible. When using R-C coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
2. The IPM has a built-in HVIC and it is possible to be connected to a microprocessor (MPU) directly without any photo-coupler or pulse-transformer isolation.
3. VFO output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10kΩ.
4. To prevent erroneous protection, the wiring of (A), (B), (C) should be as short as possible.
5. The time constant R2-C2 of the protection circuit should be selected approximately 1.5μs. Over current (OC) shutdown time might vary due to the wiring pattern. Tight tolerance, temp-compensated type is recommended for R2, C2.
6. Please recommended to set the threshold voltage of the comparator reference input to be same as the IPM OC trip reference voltage $V_{IS(ref)}$.
7. Please use high speed type comparator and logic IC to detect OC condition quickly.
8. If negative voltage is applied to R1 during the switching operation, a schottky barrier diode D1 is recommended to be connected.
9. All capacitors should be connected as close to the terminals of the IPM as possible. (C1, C4 : narrow temperature drift, higher frequency and DC bias characteristic ceramic type are recommended, and C3, C5: narrow temperature drift, higher frequency and electrolytic type.)
10. To prevent surge destruction, the wiring between the snubber capacitor and the P terminal, Ns node should be as short as possible. Generally 0.1μ to 0.22μF snubber capacitor (C6) between the P terminal and Ns node is recommended.
11. Two COM terminals (9 & 16 pin) are electrically connected inside the IPM, it must be connected either one to the signal GND outside and leave another one open.
12. It is recommended to insert a zener-diode (22V) between each pair of control supply terminals to prevent surge destruction.
13. If signal GND is connected to power GND by broad pattern, it may cause a malfunction by power GND fluctuation. It is recommended to connect signal GND and power GND at one point.

2. Recommendation and Precautions in PCB design

In this section, the recommended pattern layout and precautions in PCB design are described.
Fig.5-3 to Fig.5-7 show the image of recommended PCB layout, referring Fig.5-1 and Fig.5-2.
In these Fig., the input signals from system control are represented with "IN(HU)".

The recommendation and precautions are as follows,

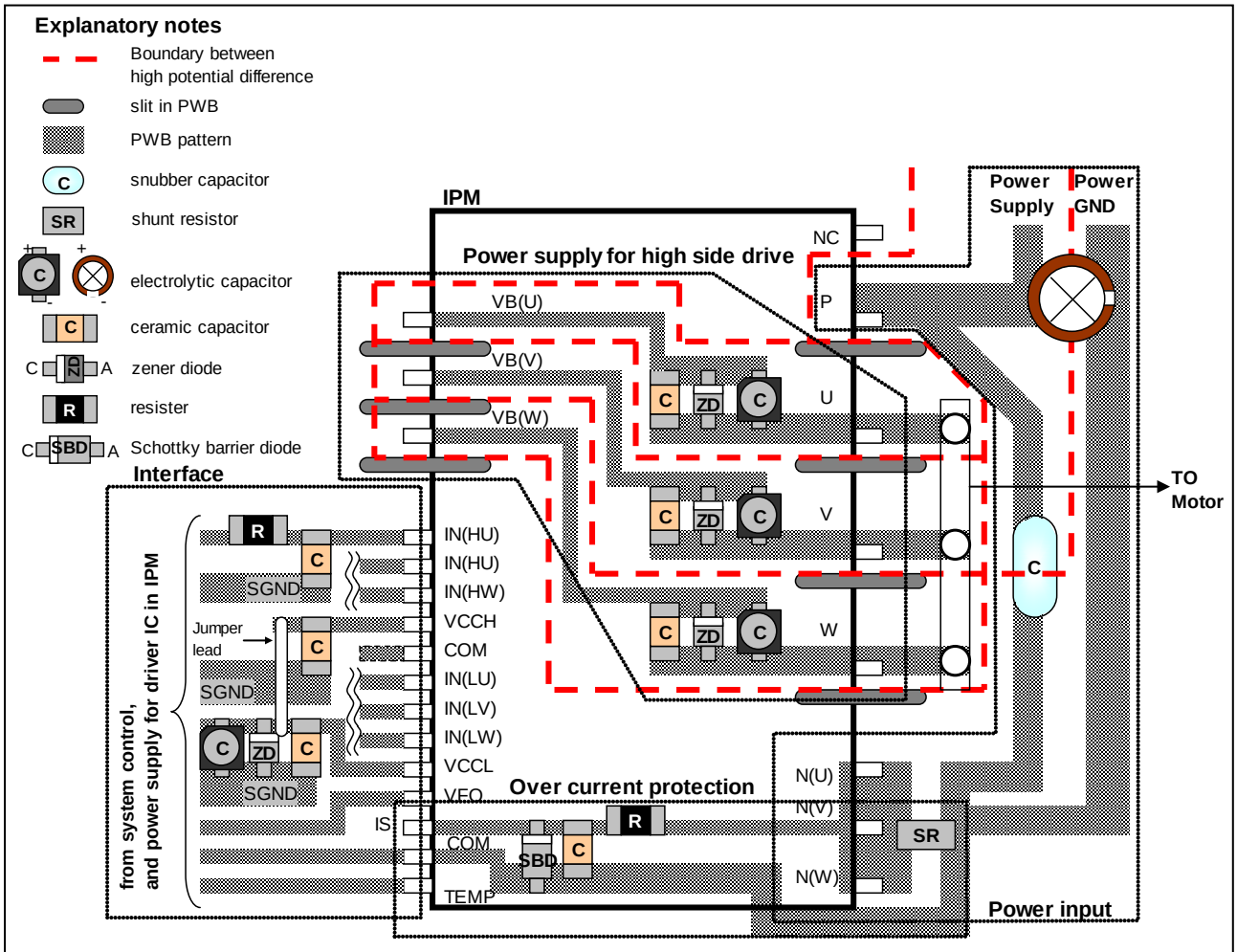
(1) Whole design in circumference of the IPM

(A) Keep a relevant creepage distance at the boundary.
(Place a slit between there if needed.)

(B) The pattern of the power input (DC bus voltage) part and the power supply for high side drive part
should be separated each other to prevent increasing the conduction noise.
Please care to stray capacitance and insulating performance of PCB if these patterns cross using multi layer PCB.

(C) The pattern of the power supply for high side drive part and the interface circuit part should be separated each other to avoid a malfunction of system. It is strongly recommended to lay out without crossing each other using multi layer PCB.

More detail in each part are described in next page.



note) The input signals are represented with "IN(HU)".

Fig.5-3 Image of recommended PCB layout
(Whole design in circumference of the IPM)

2. Recommendation and Precautions in PCB design

(2) Power input part

(A) Locate the snubber capacitor between P terminal and the negative node of the shunt resister as close as possible.
The pattern between the snubber capacitor and P terminal and shunt resister should be short as possible to avoid the influence of the pattern inductance.

(B) Pattern from the bulk capacitor and pattern of the snubber capacitor should be separated each other near the P terminal and close the shunt resister.

(C) The pattern of Power GND and the pattern from COM terminal should be connected shortly the shunt resister with single-point-grounding.

(D) The shunt resister should be chosen low-inductance type.

(E) The pattern between N(U),N(V),N(W) terminals and the shunt resister should be as short as possible.

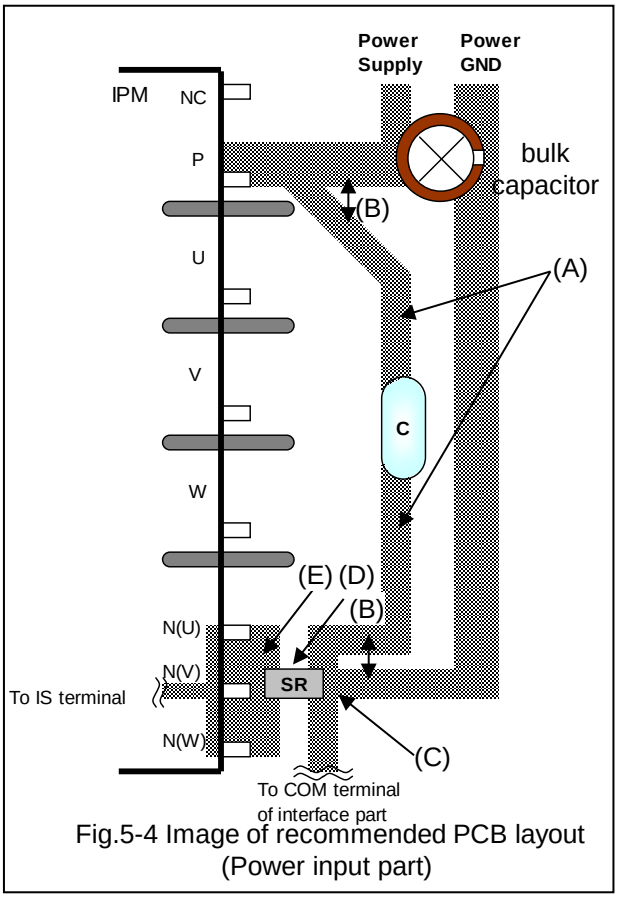


Fig.5-4 Image of recommended PCB layout (Power input part)

(3) Power supply for high side drive part.

(A) The pattern length from VB(U,V,W) and the components (ceramic capacitor, electrolytic capacitor and zener diode) of its nodes should be as short as possible to avoid the influence of the pattern inductance.

(B) Please use a relevant capacitance by the applications. And especially, please place the ceramic capacitor or low-ESR capacitor closely to the VB(U,V,W) terminals.

(C) The pattern to Motor output and the pattern to negative pole of the capacitor for VB(U,V,W) should be separated each other close the U,V and W terminals to avoid a malfunction by common impedance of these patterns.

(D) If the stray capacitance between VB(U) and Power GND (or equal potential) is large, the voltage between VB(U) and U might be over or under voltage when IGBT turns on and off with high dV/dt. Therefore, placing the zener diode between VB(U) and U are recommended. And it should be placed close VB(U) terminal.
(VB(V), VB(W) are also same as VB(U).)

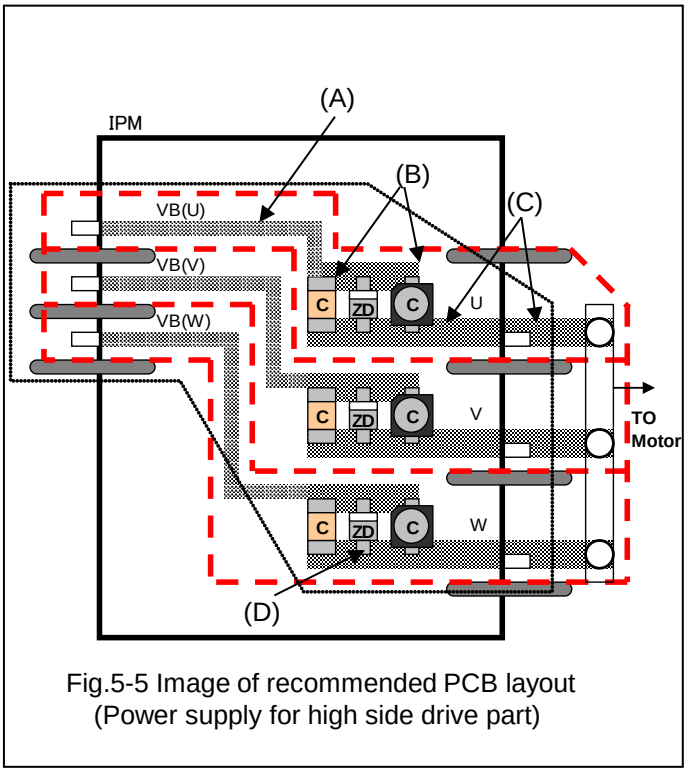


Fig.5-5 Image of recommended PCB layout (Power supply for high side drive part)

(4) Interface part

(A) Inserting the capacitor between the input signal and COM pattern are recommended if the influence of noise from the power supply for high side drive part (and so forth) can't be negligible. And the negative pole of the capacitor should be connected to the pattern of signal GND near the terminal of COM as possible.
If the series resister or the capacitor are inserted, please consider the internal pull down resisters in this IPM and please confirm signal quality in actual system.

(B) The IPM has two COM terminals. These two terminals are connected inside, so must be used either one.

(C) Electrolytic capacitor and ceramic capacitor should be connected between V_{CCL} and COM patterns, V_{CCH} and COM patterns. These should be as close to each terminal as possible.

(D) The signal from TEMP terminal should be located parallel with Signal GND to suppress noise influence.

(E) The pattern of signal GND from system control and the pattern from COM terminal should be connected together at one point ground. The one point ground should be as close to the COM terminal as possible.

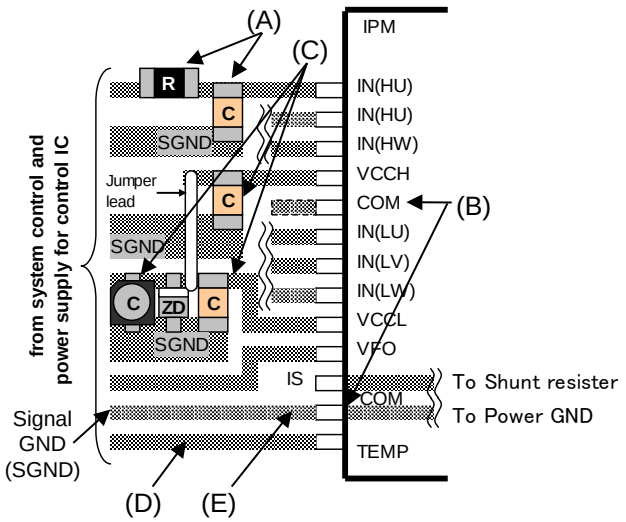


Fig.5-6 Image of recommended PCB layout (Interface part)
note) The input signals are represented with "IN(HU)".

(5) Over Current Protection part

Like Fig.5-1 and Fig. 5-2, to detect and protect the OC condition, 2 methods of current-sense are shown by example. One is "One-shunt type" (Fig.5-7 (a)) and the other is "3-shunt type" (Fig.5-7 (b)).

In Fig.5-7 (a)

(A) The pattern between negative pole of the shunt resister and the COM terminal is very important.
It plays a role of not only the reference zero level of internal control IC, but also the pass of bootstrap charging current of high side and the pass of gate driving current of low side IGBTs.
So, to make the influence of common impedance of them minimum, this pattern should be as short as possible.

(B) The pattern of IS signal should be as short as possible to avoid OC level fluctuation and malfunction.

(C) Inserting the RC filter between the IS signal is needed to prevent the miss detection of OC at the timing of switching. And the negative pole of this capacitor should be connected to the pattern of signal GND near the terminal of COM.

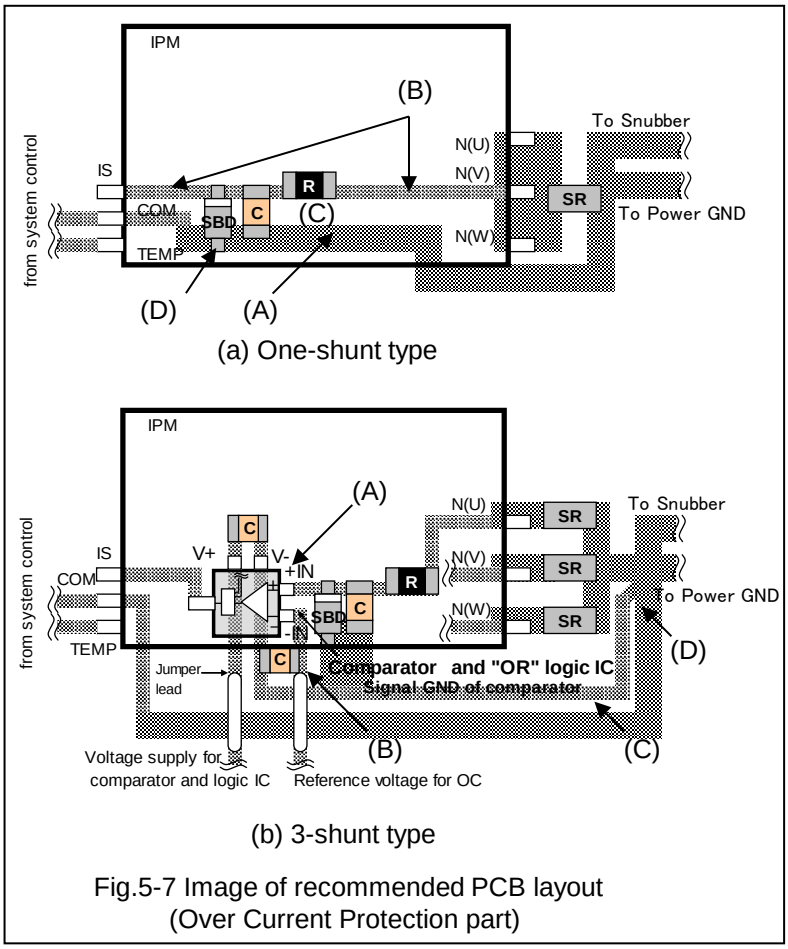


Fig.5-7 Image of recommended PCB layout
(Over Current Protection part)

(D) If a negative voltage at the switching timing is applying to IS terminal, the schottky barrier diode should be inserted between IS terminal and COM terminal or parallel to the shunt resister .

In Fig.5-7 (b)

(A) Please use high speed type comparator and logic IC to detect OC condition quickly.

(B) The reference voltage level of OC which is inputted to the comparator should be coupled by capacitor to signal GND. And it should be as close to comparator as possible.

(C) The pattern of signal GND for COM terminal and the pattern of signal GND for the comparator should be separated each other.

(D) The pattern of signal GND from COM and the pattern of signal GND of the comparator should be connected together at one point ground. The one point ground should be as close to the negative pole of the shunt resisters.

(E) The other precautions and recommendations are same as Fig.5-7 (a).

For more detail of determination circuit parameters please refer to Chapter 4 section 2.