Chapter 4 Drive Circuit Design

This chapter describes the drive circuit design. The drive circuit consists of a forward bias circuit that turns on the IGBT and a reverse bias circuit that keeps the IGBT off stably. The main characteristics of the IGBT, such as switching operation, change according to the value of V_{GE} and R_G. Table.4-1 shows the general relationship between IGBT drive conditions and the main characteristics. Since the main characteristics of the IGBT change depending on V_{GE}, R_G, etc., it is necessary to set them according to the design goal of the device.

Table.4-1 IGBT drive conditions and main characteristics

Main characteristic	$+V_{GE}$ increase	$-V_{GE}$ increase	$R_{G(on)}$ increase	$R_{G(off)}$ increase
$V_{CE(sat)}$	↓	–	–	–
t_{on} E_{on}	↓	–	↑	–
t_{off} E_{off}	–	↓	–	↑
Turn-on FWD overvoltage	↑	–	↓	–
Turn-off IGBT overvoltage	–	↑	–	↓ *1
d*v*/d*t* shoot through	↑	↓	↓	↓
Saturation current value	↑	–	–	–
Short circuit withstand capability	↓	–	↑	↓
Radiation noise	↑	–	↓	↓

*1 Dependence of overvoltage on R_G is different for each series

1. Forward Bias Gate Voltage $+V_{GE}$ (On-State)

The recommended gate voltage value ($+V_{GE}$) is +15V. Notes when designing $+V_{GE}$ are shown as follows.

(1) Design the $+V_{GE}$ below the max. rated voltage of ±20V.
(2) It is recommended that supply voltage fluctuation is kept to within ±10%.
(3) The on-state $V_{CE(sat)}$ is dependent on the $+V_{GE}$, so the higher the $+V_{GE}$, the lower $V_{CE(sat)}$.
(4) The higher the $+V_{GE}$, the smaller the turn-on switching time and switching loss.
(5) At turn-on (at FWD reverse recovery), the higher the $+V_{GE}$, the greater the likelihood of overvoltage in opposing arms.
(6) Even while the IGBT is in off-state, there may be malfunctions caused by the d*v*/d*t* of the FWD's reverse recovery and a pulse I_C may cause unnecessary heat generation. This phenomenon is called a d*v*/d*t* shoot through and becomes more likely to occur as the $+V_{GE}$ increases.
(7) Generally, the higher the $+V_{GE}$, the higher the saturation current becomes.
(8) The higher the $+V_{GE}$, the shorter the short circuit withstand capability.

2. Reverse Bias Gate Voltage -V_{GE} (Off-State)

One way to prevent dv/dt shoot through is to apply -V_{GE}. Notes when designing -V_{GE} are shown as follows.

(1) Design the -V_{GE} below the max. rated voltage of ±20V.

(2) It is recommended that supply voltage fluctuations are kept to within ±10%.

(3) IGBT turn-off characteristics are heavily dependent on -V_{GE}, especially when I_C is just beginning to switch off.

3. R_G (Gate Resistance)

Gate resistance R_G needs to be adjusted appropriately depending on the circuit configuration and environment. Notes when designing R_G are shown as follows.

(1) The switching characteristics of both turn-on and turn-off are dependent on the value of R_G, and therefore the larger the R_G, the longer the switching time and the larger the switching loss. Also, as R_G increases, the overvoltage during switching becomes smaller.

(2) The larger the R_G, the more unlikely dv/dt shoot through will occur.

(3) Switching characteristics vary greatly depending on the parasitic inductance. In particular overvoltage generated during IGBT turn-off and during FWD reverse recovery are greatly affected. Therefore, R_G needs to be designed with low parasitic inductance.

4. Drive Current

Since the IGBT has a MOSFET gate structure, gate current (drive current) is needed to charge and discharge this gate during switching. Fig.4-1 shows the gate charge (dynamic input) characteristics. The gate charge is the amount of charge required to drive the IGBT and is used to calculate the average drive current and power.

Fig.4-2 shows an example of the drive circuit and the gate voltage / current waveform. The principle of the drive circuit is to switch the forward bias power supply and the reverse bias power supply alternately with switches S1 and S2. The current that charges and discharges the gate during this switching is the drive current, and the area (shaded area) represented by the gate current waveform in Fig. 4-2 is equal to the amount of charge in Fig. 4-1.

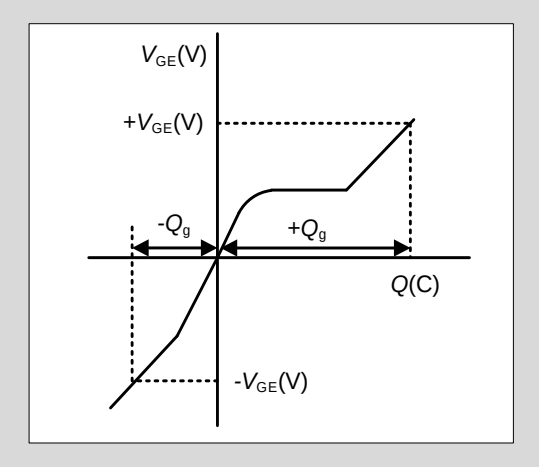


Fig.4-1 Gate charge characteristic (Dynamic input characteristics)

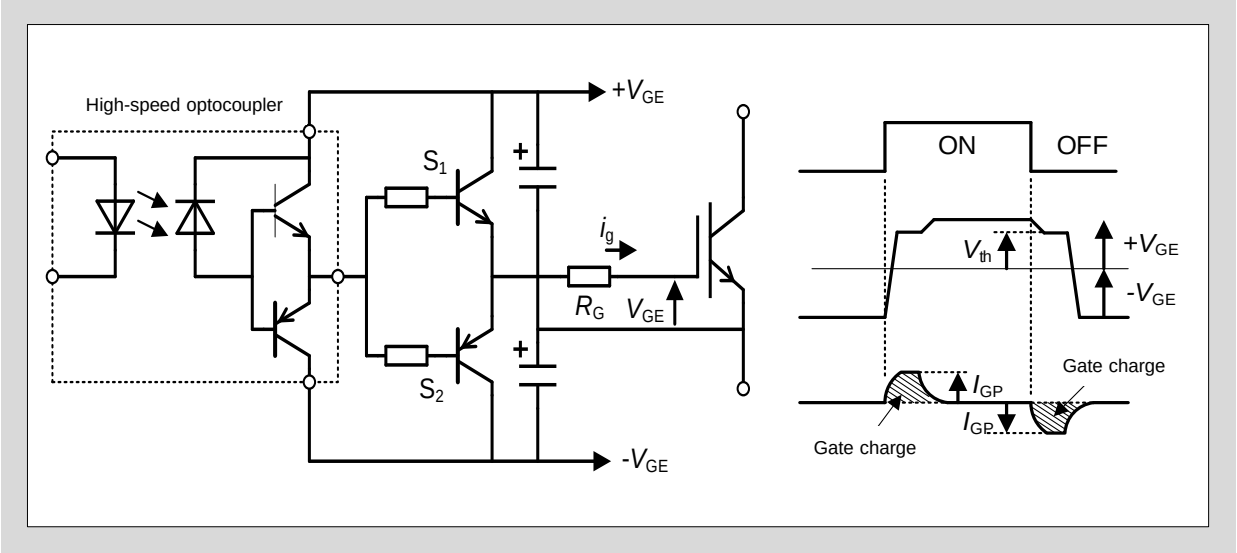


Fig.4-2 Drive circuit schematic and voltage / current waveforms

The drive current peak value I_{GP} can be approximately calculated as follows:

$$I_{GP} = \frac{|+V_{GE}|+|-V_{GE}|}{R_G}$$

$+V_{GE}$: Forward bias supply voltage
$-V_{GE}$: Reverse bias supply voltage
R_G : Drive circuit gate resistance

The average value of the drive current I_G, using the gate charge characteristics (Fig.4-1), can be calculated as follows:

$$+I_G = -I_G = f_c \cdot (|+Q_g| + |-Q_g|)$$

f_C : Carrier frequency
$+Q_g$: Gate charge from 0V to $+V_{GE}$
$-Q_g$: Gate charge from $-V_{GE}$ to 0V

It is important to design the output stage of the drive circuit in consideration of this approximate current (I_{GP} and $\pm I_G$). Furthermore, if the power dissipation loss of the drive circuit is completely consumed by the gate resistance, then the drive power (P_d) necessary to drive the IGBT is shown in the following formula:

$$P_{d(on)} = P_{d(off)} = f_C \cdot \left[\frac{1}{2}(|+Q_g|+|-Q_g|) \cdot (|+V_{GE}|+|-V_{GE}|)\right]$$

$$P_d = P_{d(on)} + P_{d(off)} = f_C \cdot (|+Q_g|+|-Q_g|) \cdot (|+V_{GE}|+|-V_{GE}|)$$

It is necessary to select gate resistance that can tolerate the loss generated by this approximation formula.

5. Setting Dead Time

In inverter circuits, etc., dead time is set for on / off switching timing to prevent short circuits between the upper and lower arms. As shown in Fig.4-3, both the upper and lower arms are in the "off" state during the dead time. Basically, the dead time needs to be set longer than the max. value of the IGBT switching time ($t_{d(off)}+t_f$). If the dead time is short, short circuit may occur between the upper and lower arms, and the heat generated by the short circuit current may destroy the device.

Also, increasing R_G will increase the switching time, so it is necessary to increase the dead time. In addition, it is necessary to consider other drive conditions, device variations, temperature characteristics, etc..

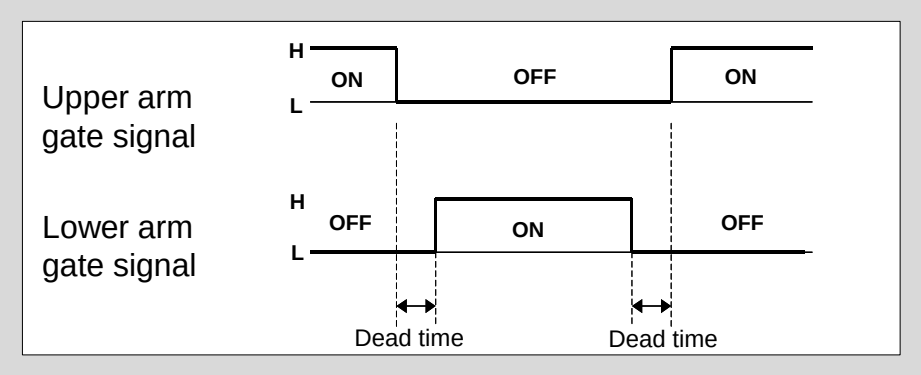


Fig.4-3 Dead time timing chart

Whether the dead time setting is sufficient is judged by checking the current of the DC supply line when there is no load. In the case of 3-phase inverter (as shown in Fig.4-4), set the inverter's outputs to no load, then apply normal input signal, and finally measures the DC line current. Very small pulse current (d*v*/d*t* current through the IGBT's miller capacitance: about 5% of the normal rated current) will be observed, even if the dead time is long enough. However, if the dead time is insufficient, then there will be a much larger short circuit current. In this case, keep increasing the dead time until the short circuit current disappears. It is recommended to perform this test at high temperature because the higher the temperature, the longer the turn-off time. Also, if $-V_{GE}$ is insufficient, the short circuit current will increase due to d*v*/d*t* shoot through. If the short circuit current does not decrease even if the dead time increases, increase $-V_{GE}$.

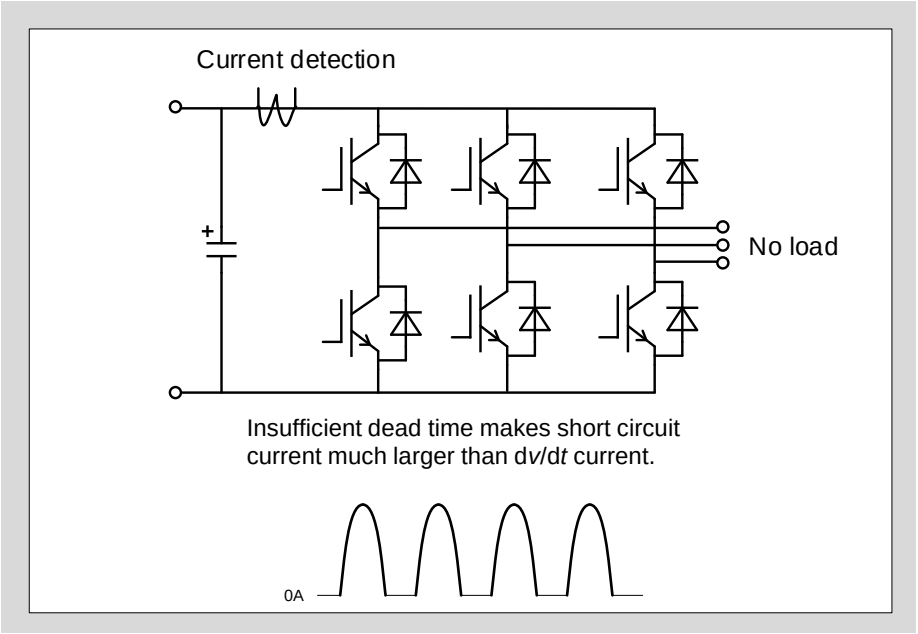


Fig.4-4 How to detect short circuit current due to insufficient dead time

6. Example of Drive Circuits

Fig.4-5 shows an example of a drive circuit using high-speed optocoupler. By using optocoupler, the input signal and the IGBT are isolated from each other. Also, since the optocoupler does not limit the output pulse width, it is suitable for applications where the pulse width change over a wide range, such as PWM controller, and is currently the most widely used. Furthermore, the turn-on and turn-off characteristics determined by gate resistance can be set separately, so it is commonly used to ensure the best settings.

In addition, there is a drive method that uses a pulse transformer for signal isolation. This method simplifies the circuit because both the signal as well as the gate drive power can be supplied simultaneously from the signal side. However, this method has the limitations of on / (off+on) time ratio of max. 50%, and reverse bias cannot be set, so it's usefulness as a control method and switching frequency regulator is limited.

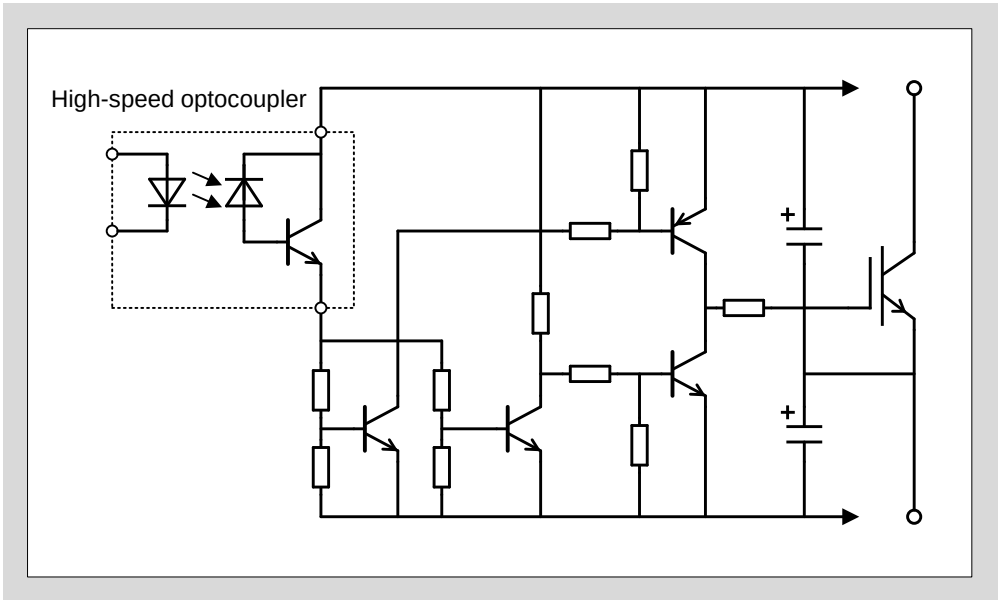


Fig.4-5 Example of drive circuit using high-speed optocoupler

7. Precautions for Drive Circuit Design and Mounting

＜Optocoupler noise tolerance＞

IGBT is a high-speed switching device, thus it is necessary to select optocoupler that has high noise tolerance for the drive circuit. Also, to prevent malfunctions, make sure that the wiring from on the primary and secondary side of the optocoupler do not cross. Furthermore, in order to make full use of the IGBT's high-speed switching capabilities, we recommend using a optocoupler with short signal transmission delay.

＜Wiring between drive circuit and IGBT＞

If the wiring between the drive circuit and the IGBT is long, the IGBT may malfunction due to gate signal oscillation or induced noise. A countermeasure for this is shown below in Fig.4-6.

(1) Make the drive circuit wiring as short as possible and finely twist the gate and emitter wiring. (Twisted wiring)

(2) Increase R_G. However, pay attention to switching time and switching loss.

(3) Separate the gate wiring and IGBT main circuit wiring as much as possible, and set the layout so that they cross each other (in order to avoid mutual induction).

(4) Do not bundle together the gate wiring or other phases.

(5) If voltage is applied to the main circuit when the gate drive circuit is defective or not operating completely (gate open), the IGBT may be destroyed. As a prevention measure, it is recommended to connect a G-E resistance R_{GE} of about 10 kΩ (see Fig. 4-6).

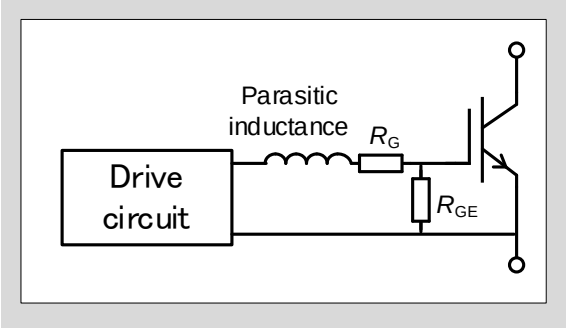


Fig.4-6 Precautions for mounting the gate drive circuit

＜Gate overvoltage protection＞

It is necessary that IGBT, like other MOSFET, are sufficiently protected against static electricity. Also, since V_{GE} max. is ±20V, if there is a possibility that voltage greater than this may be applied. As a protective measure it is necessary to connect a G-E zener diode as shown in Fig.4-7.

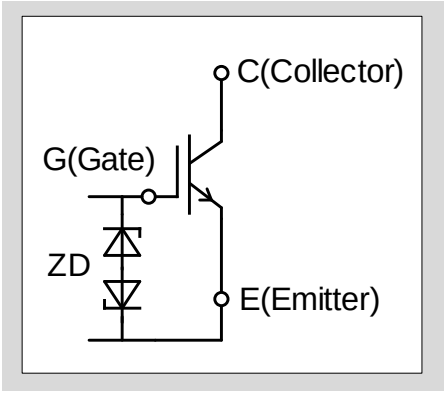


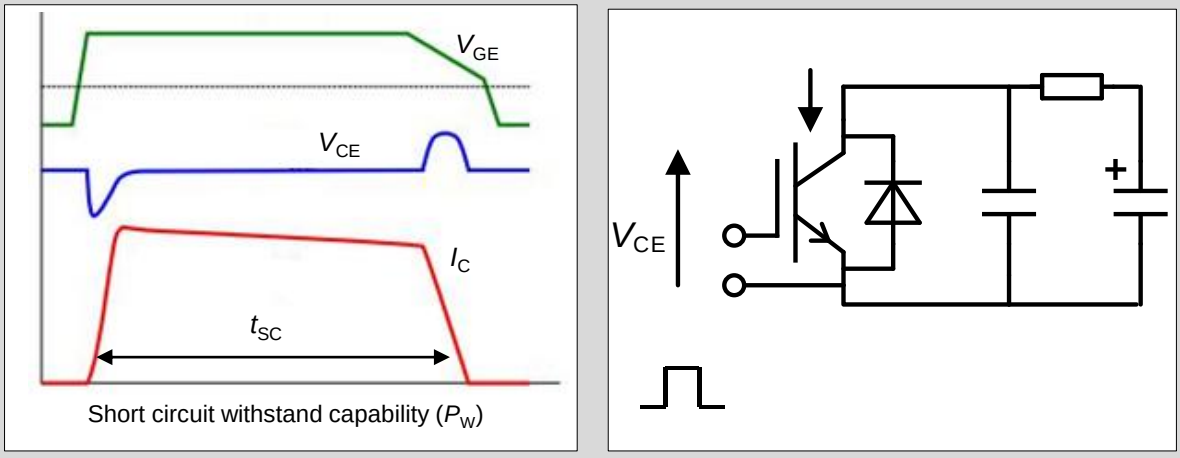
Fig.4-7 G-E overvoltage protection circuit example

＜Short circuit withstand capability＞

Overcurrent may flow in the IGBT due to the short circuit. If the overcurrent continues to flow, the temperature of the device will rise sharply, resulting in permanent destruction. As shown in Fig.4-8 (a), the short circuit withstand capability is specified by the time (t_{SC}) from the start of the short circuit current until the current is safely cut off. The short circuit withstand capability (t_{SC}) depends on conditions such as V_{CE}, V_{GE}, and T_{vj}. Generally, the higher the power supply voltage E_d and the higher the T_{vj}, the smaller the t_{SC}.

In our Discrete IGBT lineup, the V series is for applications that require long short circuit withstand capability, and High-Speed V, High-Speed W series and XS series for applications that require lower switching loss and lower saturation voltage instead of long short circuit withstand time. The short circuit withstand capability of the High-Speed W series 650V series and XS series is not guaranteed.

Fig.4-8(b) shows the circuit diagram for measuring short circuit withstand capability. When the load is short circuited, the IGBT will be subjected to high voltage / high current.



(a) Typical waveform at the time of short circuit　　(b) Measuring circuit diagram

Fig.4-8　Measuring circuit and waveform

＜Short circuit protection by V_{CE} detection＞

In this method, the operation from overcurrent detection to protection is performed on the drive circuit side, thus high-speed protection operation is possible. The short circuit protection schematic is shown in Fig.4-9. This circuit uses D1 to constantly monitor V_{CE}, so if during operation the IGBT's V_{CE} rises above the voltage limit set by D2, short circuit condition will be detected and T1 will be switched on while T2 and T3 are switched off. At this time, the accumulated charge at the gate is slowly discharged through R_{GE}, so overvoltage is suppressed when the IGBT is turned off. Fig.4-10 shows the IGBT waveform during short circuit protection.

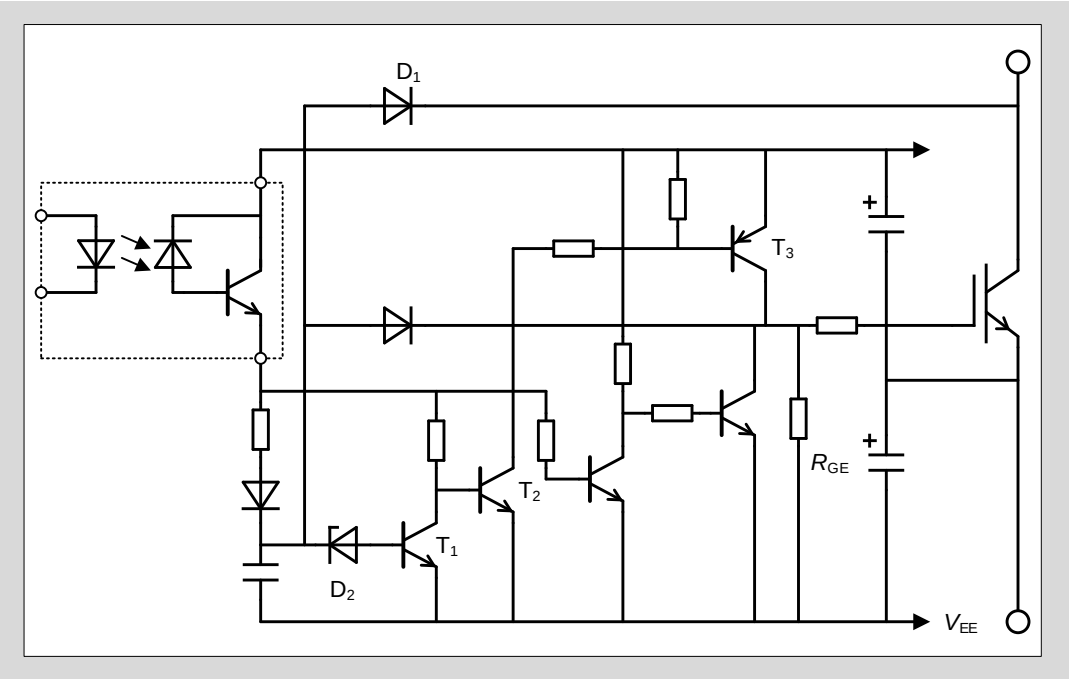
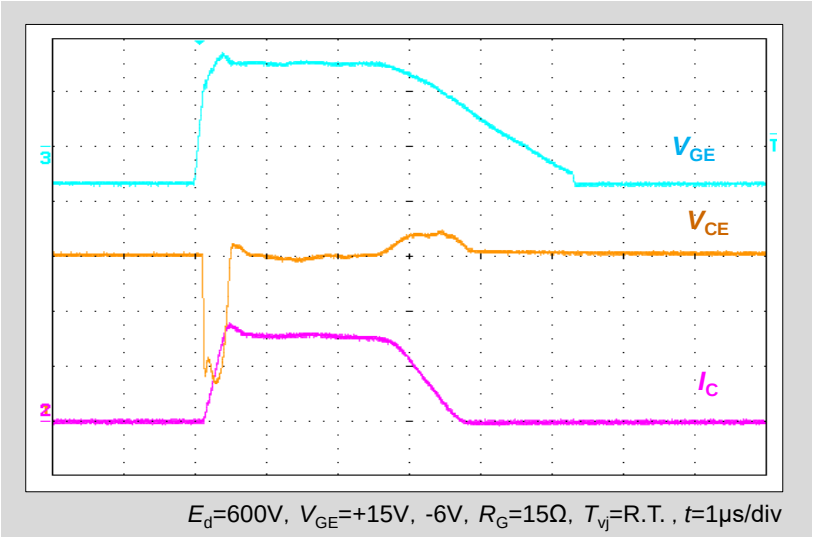


Fig.4-9 Short circuit protection schematic by V_{CE} detection



E_d=600V, V_{GE}=+15V, -6V, R_G=15Ω, T_{vj}=R.T. , t=1μs/div

Fig.4-10 Waveforms during short circuit protection