PrimePACK™

Parallel Connection

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This document explains the notes when PrimePACK™ IGBT module is connected in parallel.

IGBTs would be connected in parallel in order to enlarge the current capability. In this case, the number of parallel-connected modules has no limitation. However you have to consider some disadvantages of noise or spike voltage increase, which are caused by longer interconnections.

You have to pay attention to the following basic notes when connecting IGBT modules in parallel.

1) Suppression of current imbalance at steady states
2) Suppression of current imbalance at dynamic state of turn-on or turn-on

1 Current imbalance at steady state

An on-state current imbalance is caused mainly by the following two factors:

(1) $V_{CE(sat)}$ distribution

(2) Main circuit wiring resistance distribution

1.1 Current imbalance caused by $V_{CE(sat)}$ distribution

As shown in Fig.1, a difference in the output characteristics of two IGBT modules connected in parallel can cause a current imbalance.

The output characteristics of Q_1 and Q_2 shown in Fig.1 can be approximated by following equations:

$$V_{CEQ1} = V_{01} + r_1 \times I_{C1}$$

$$r_1 = V_1 / (I_{C1} - I_{C2})$$

$$V_{CEQ2} = V_{02} + r_2 \times I_{C2}$$

$$r_2 = V_2 / (I_{C1} - I_{C2})$$

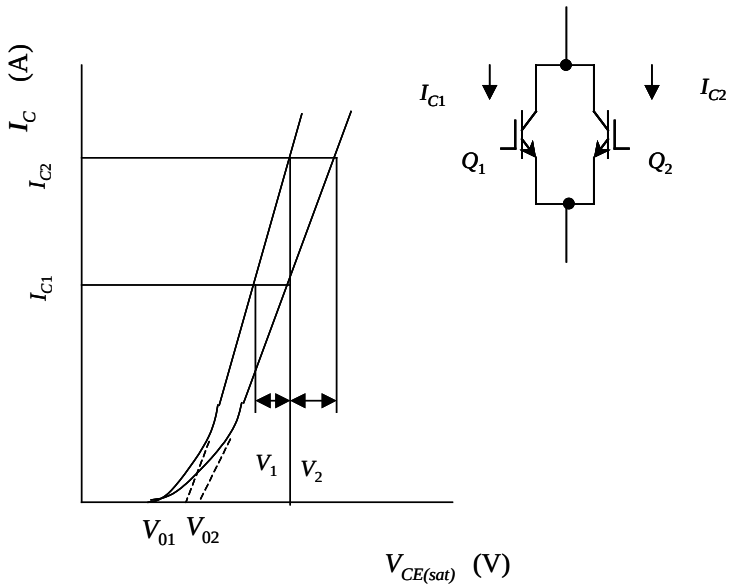


Fig. 1 Example of a $V_{CE(sat)}$ pair

Based on the above, if the total collector current I_{Ctotal} (=I_{C1}+I_{C2}) flows through the circuit which Q_1 and Q_2 connected in parallel, then the IGBTs collector current (I_{C1} and I_{C2}) are described as the following:

$$I_{C1} = (V_{02} - V_{01} + r_2 \times I_{Ctotal}) / (r_1 + r_2)$$

$$I_{C2} = (V_{01} - V_{02} + r_1 \times I_{Ctotal}) / (r_1 + r_2)$$

For simplicity, assuming V_{01}=V_{02} in the above equations, I_{C1} could be r_2/r_1 times larger than I_{C2}. This result means that current sharing for Q_1 is larger than Q_2.

As described above, $V_{CE(sat)}$ distribution is a major factor in causing current imbalances. Therefore, in order to achieve desired current sharing, it is necessary to pair modules that have a similar $V_{CE(sat)}$ which is small variation. $V_{CE(sat)}$ distribution can be minimized with the use of the same rank product (see Section 1.5).

1.2 Current imbalance by main circuit wiring resistance distribution

An equivalent circuit for two paralleled IGBTs with the main circuit's wiring resistance is shown in Fig. 2. The resistance of the collector side is omitted because the wiring resistance of the emitter side is larger than that of the collector side. If there is resistance in the main circuit as shown in Fig.2, then the slope of the IGBT modules' output characteristics will lessen, and the collector current will drop in comparison without emitter resistance. In addition, if $R_{E1} > R_{E2}$, then the slope of the Q_1 output characteristics will lessen and if $I_{C1} < I_{C2}$ then a current sharing imbalance will appear. Moreover, if gate voltage is applied without extra-emitter terminals for parallel-connected IGBTs, the actual gate-emitter voltage drop ($V_{GE} = V - V_E$) will be decreased, because an electrical potential difference may appear, depending on how well the collector current can flow through this resistance. So, the IGBTs' output characteristics change and the collector current decline.

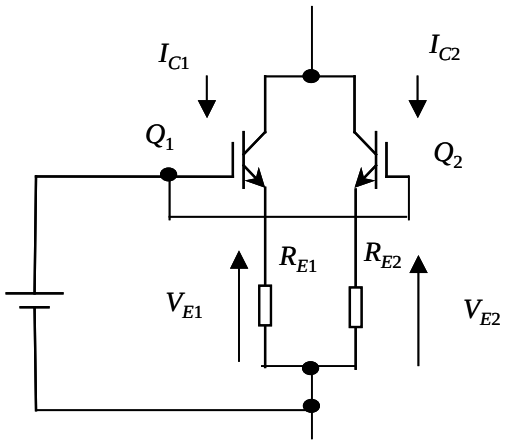


Fig. 1 The effect of main circuit wiring resistance

Therefore, in order to reduce this imbalance, it is necessary to make the wiring on the emitter side as short and as uniform as possible as well as to apply the gate voltage between gate terminal and additional emitter terminal.

1.3 Derating in parallel connection of IGBTs

Derating (Decreasing of total current) has to be considered in parallel connection of IGBTs. When '*n*' modules are connected in parallel, the following equation shows the maximum current that can be applied under the worst case conditions where the entire current is concentrated into one module, whose VCE(sat) is the smallest. Therefore, available maximum current Σ*I* is expressed by α, which is connected in parallel using 2 modules:

$$\sum I = I_{C(\max)}\left[1+(n-1)\frac{\left(1-\frac{\alpha}{100}\right)}{\left(1+\frac{\alpha}{100}\right)}\right] \qquad \alpha = \left(\frac{I_{C1}}{I_{C(ave)}}-1\right)\times 100$$

Here $I_{C(max)}$ represents the maximum current for a single element, Σ*I* represents the maximum current in parallel connection. However, to operate in total current Σ*I*, each module connected in parallel is satisfied with the RBSOA on the specification, Tj(max) for dissipation wattage as well. Note especially that Tj rise caused by dissipation wattage is various on the condition such as switching frequency, driving

condition, cooling condition and snubber condition and so on.

For example, if α=5%, $I_{C(max)}$=600A and n=4, then ΣI=2229A, and the parallel connected total current should be set so as not to exceed this value. In this case, Derating of 7.1% is needed. In this way, the parallel connected total current is need to be derated for simply calculating n x $I_{C(max)}$.

1.4 Deviation of VCE(sat) and current imbalance rate

Ratio of shared current in parallel connection is called as current imbalance rate, which is determined by deviation of VCE(sat) and T_j dependency of output characteristic.

Fig. 3 shows the representative relationship between deviation of $V_{CE(sat)}$ and current imbalance rate. This figure is an example for 2 parallel connections of V-series IGBTs. From this figure, current imbalance rate is found to be larger as deviation of $V_{CE(sat)}$ is increased. Therefore, it is important to use IGBTs for parallel connection, whose deviation of $V_{CE(sat)}$ is small, that is, $\Delta V_{CE(sat)}$ is small.

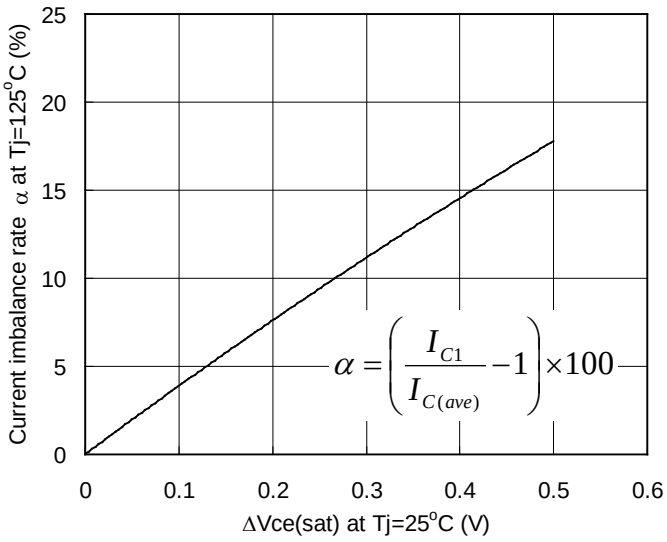
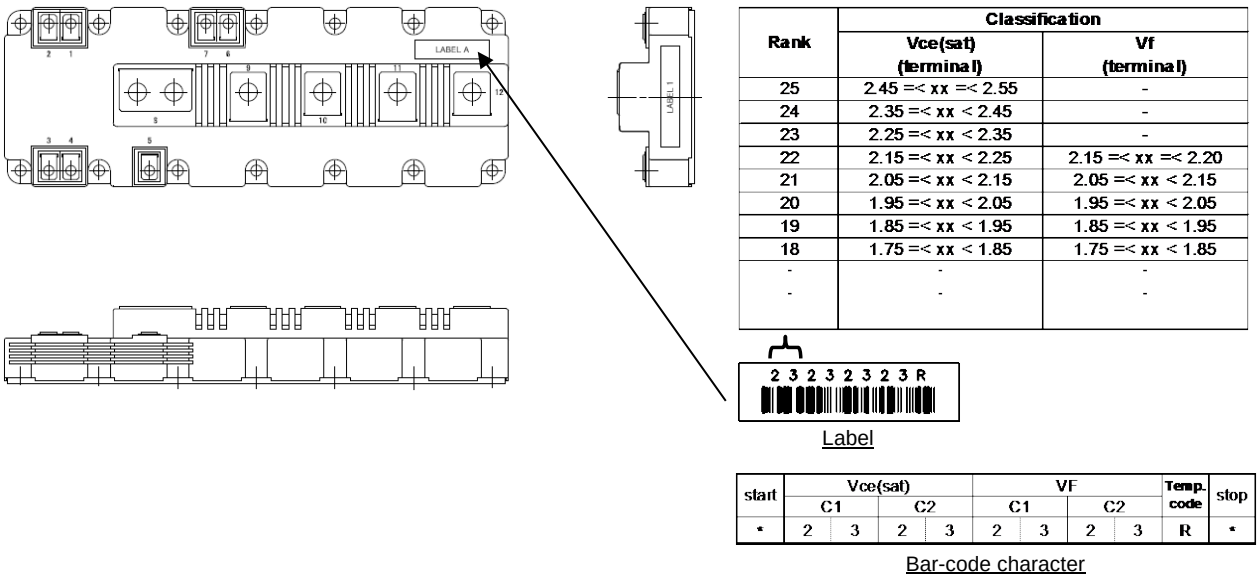


Fig. 3 Deviation of $V_{CE(sat)}$ and current imbalance rate

1.5 Appendix / Introduction of -54 type

Fuji's PrimePACK™ products has clasfied V_F and $V_{CE(sat)}$ rank.
Suffix -54 is added to the part number for each product. You can achieve the parallel connection with good current balance by combining the same rank of $V_{CE(sat)}$ / V_F.

Fig.5 is an example of -54 type specification which has $V_{CE(sat)}$ and V_F classification. Combination of same or close rank products can achieve good current imbalance.



Display on the classification label

Rank	Classification	
	Vce(sat) (terminal)	Vf (terminal)
25	2.45 =< xx =< 2.55	-
24	2.35 =< xx < 2.45	-
23	2.25 =< xx < 2.35	-
22	2.15 =< xx < 2.25	2.15 =< xx =< 2.20
21	2.05 =< xx < 2.15	2.05 =< xx < 2.15
20	1.95 =< xx < 2.05	1.95 =< xx < 2.05
19	1.85 =< xx < 1.95	1.85 =< xx < 1.95
18	1.75 =< xx < 1.85	1.75 =< xx < 1.85
-	-	-
-	-	-

2 3 2 3 2 3 2 3 R

Label

start	Vce(sat)				VF				Temp. code	stop
	C1		C2		C1		C2			
*	2	3	2	3	2	3	2	3	R	*

Bar-code character

Fig.5 Classification of -54 type

2 Current Imbalance at switching

2.1 Main circuit wiring inductance distribution

Inhomogeneous main circuit wiring inductance caused current sharing. Fig. 6 shows the equivalent circuit at parallel connection in consideration with main circuit wiring inductance. When IC1 and IC2 flow through IGBT1 and 2 respectively, shared currents for them are approximately decided by the ratio of main circuit wiring inductance, LC1+LE1 and LC2+LE2. So, main circuit wiring is need to be connected as equally as possible in order to relieve current imbalance at switching. However, even if ideal wiring inductance of LC1+LE1=LC2+LE2 is realized, the difference between LE1 and LE2 causes the current imbalance as described bellows.

In addition, connect wiring to be evenly between the collector and emitter of each module, if you want to add the snubber circuit for surge voltage suppression.

Consider the equalization as well as the wiring of each output terminal

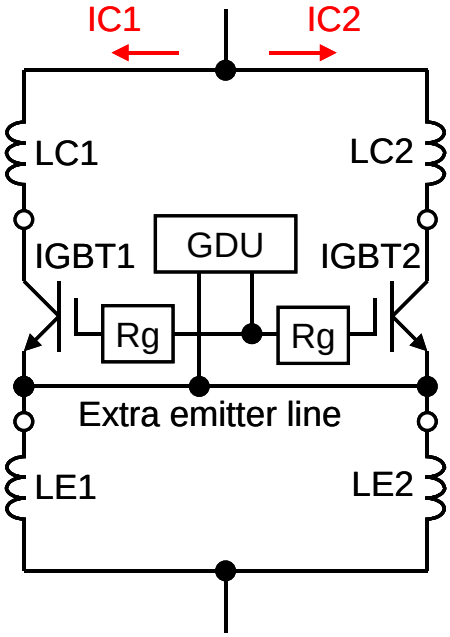


Fig. 6 Equivalent circuit at parallel connection in consideration with main circuit wiring inductance

3 Gate drive circuit

3.1 Gate drive circuit

It would be worried that duration until switching (turn-off or turn-on) is varied by the delay time of gate driving unit (GDU), when each gate of parallel-connected modules is driven by each GDU, separately independent on the number of modules. Therefore, it is recommended that all the gates are driven by just only a GDU, when connecting modules in parallel. This can lead the decrease of deviation for different duration until switching.

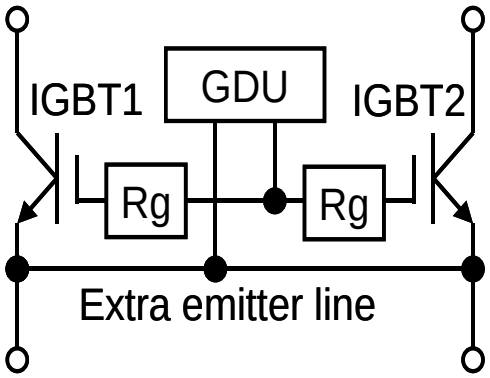


Fig.7 Wiring of gate drive unit

At the same time, connect gate resistances between gate terminal of each module and a GDU so as to avoid the gate voltage oscillation caused by coupling gate wiring inductance with input capacitance of IGBT as shown in Fig.7.

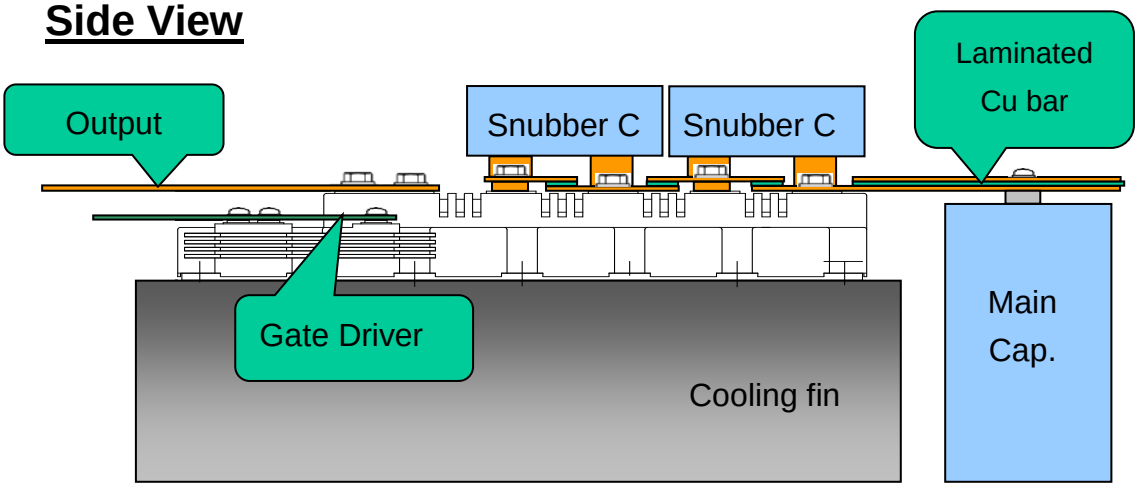
As stated previously, if the drive circuit's emitter wiring is connected in a different position from the main circuit, then the modules' transient current sharing (especially at turn-on) will become imbalanced, because LE1 is different from LE2 as described in Fig.6.

In general, IGBT modules have an auxiliary emitter terminal for use by drive circuits. By using this terminal, the drive wiring of each module becomes uniform, and transient current imbalances attribute to drive circuit wiring can be controlled. Furthermore, be sure to wind the drive circuit wiring tightly together, and lay it out so that it is as far away from the main circuit as possible in order to avoid mutual induction.

4 Wiring example for parallel connections

4.1 Wiring example of 2 parallel connection

Side View



Top

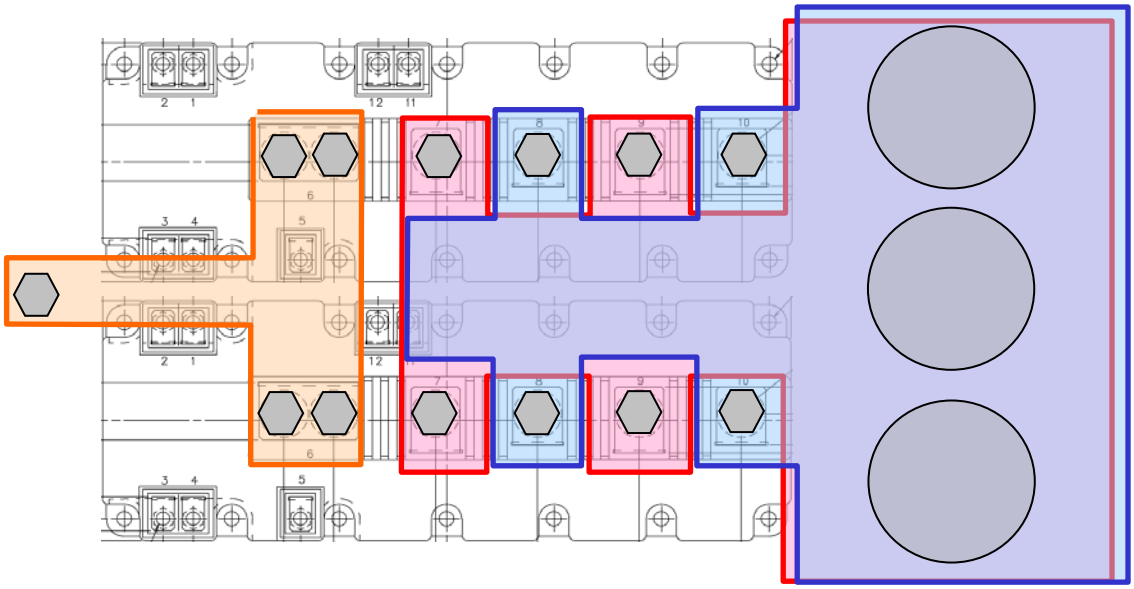
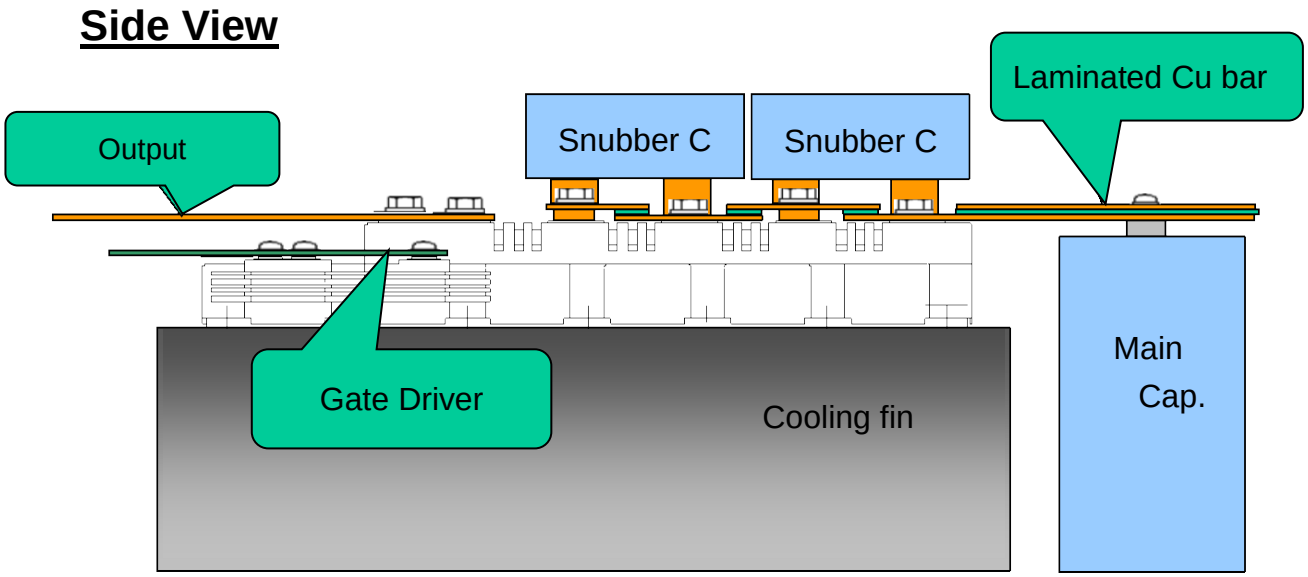
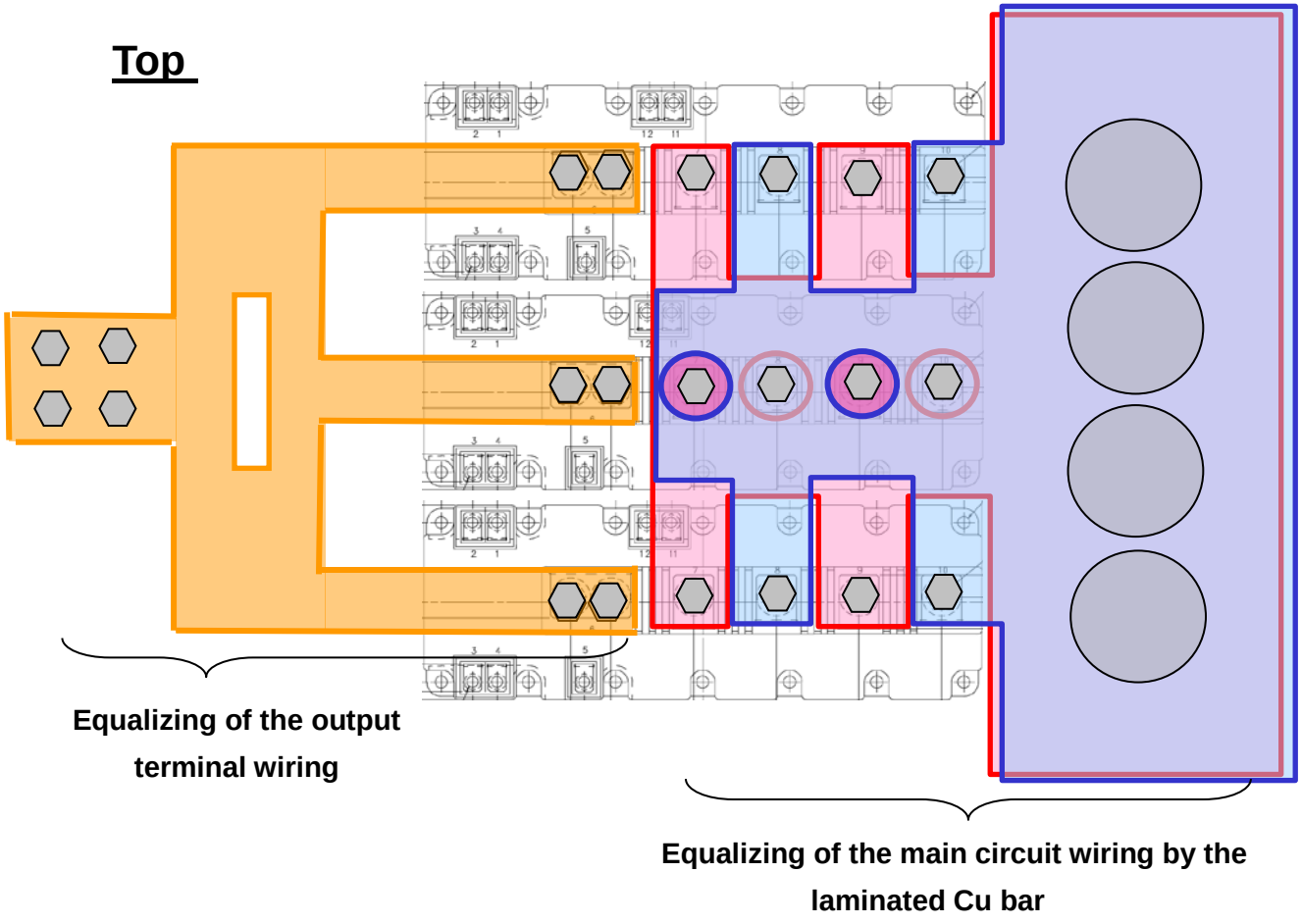


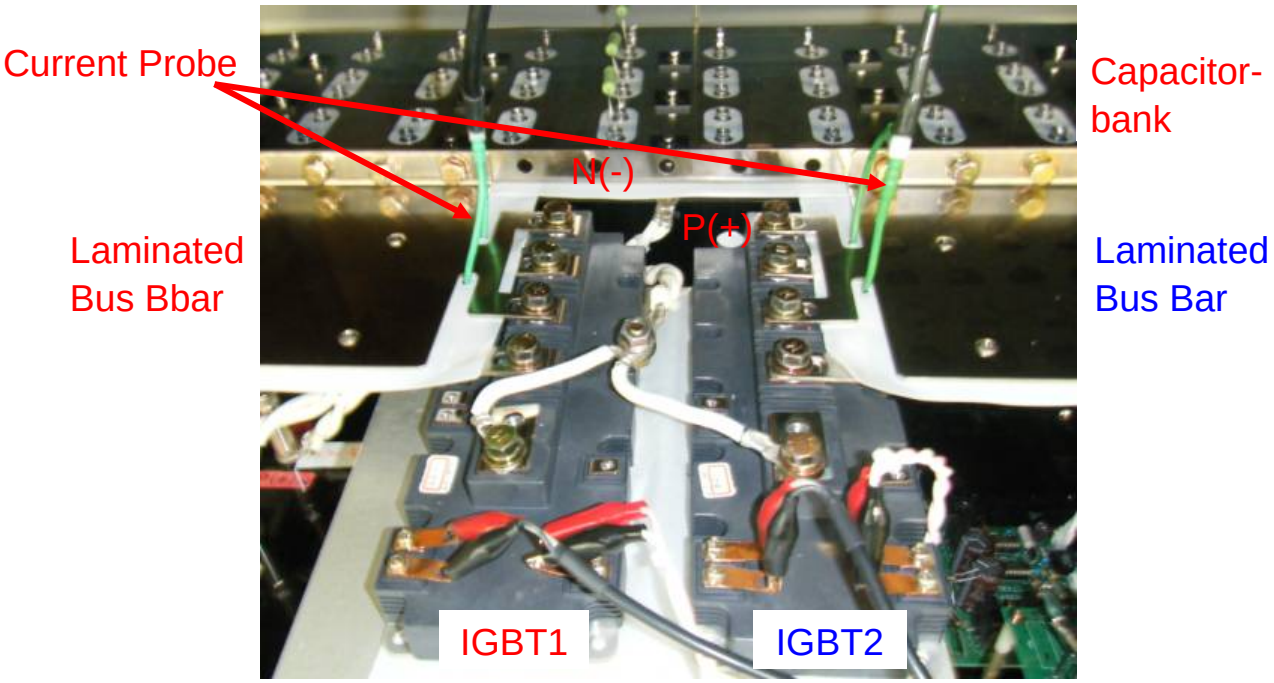
Fig.8 Wiring example of 2 parallel connection

4.2 Wiring example of 3 parallel connection





4.3 Example of 2-parallel connection 2MBI1000VXB-170E-50



A symmetrical structure is important factor to realize good current balance.

The picture above shows an example of parallel-connected IGBT modules. IGBT1 and IGBT2 are connected by symmetrical bus bars.

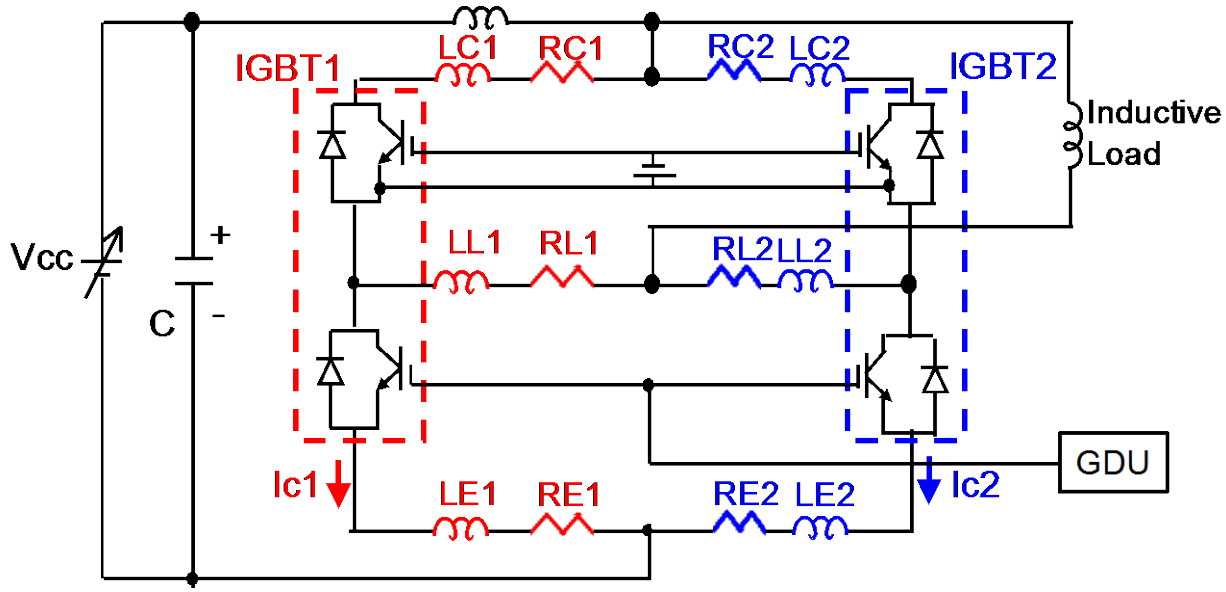


Fig. 10 Equivalent circuit with parallel-connected 2in1 modules

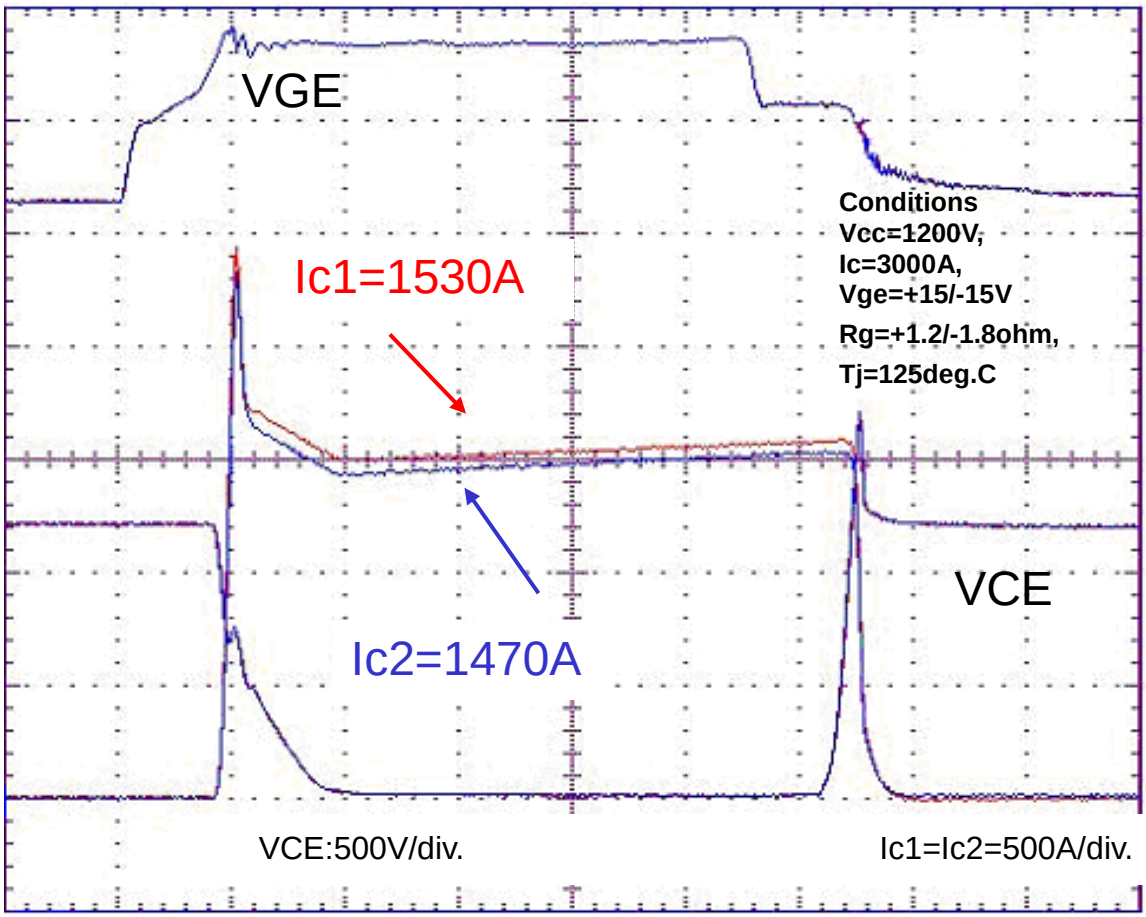


Fig. 11 Switching waveform with the two IGBT modules connected in parallel (1000A/1700V 2in1 module: 2MBI1000VXB-170E-50)