1.2-kV SiC Superjunction MOSFETs

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ABSTRACT

Fuji Electric formed a 4H-SiC-based 1.2-kV SiC Superjunction MOSFETs (SiC-SJ-MOSFETs) by repeating n-type epitaxial growth and Al ion implantation and verified its static and reverse recovery characteristics. The on-resistance of the SiC-SJ-MOSFETs at 175 °C was 55% to 65% that of the conventional trench gate MOSFETs. In terms of reverse recovery characteristics, the SiC-SJ-MOSFETs did not show an excessive surge voltage despite a slight increase in reverse recovery charge at 175 °C compared with conventional SiC trench gate MOSFETs. We expect that the use of SiC-SJ-MOSFETs in inverter circuits will contribute to reducing total loss.

1. Introduction

SiC power devices using silicon carbide (SiC) as a semiconductor material can reduce conduction loss by increasing the doping concentration of the drift layer, taking advantage of a higher critical electric field strength than silicon (Si). Fuji Electric produces Schottky barrier diodes (SiC-SBDs) with blocking voltages of 650 to 3,300 V and metal oxide-semiconductor field-effect transistors (SiC-MOSFETs) with blocking voltages of 1,200 V. For many years, the SiC-MOSFET had a problem that the specific on-resistance*1 $R_{on} \cdot A$ does not decrease due to its high channel resistance during conduction. Recently, by reducing cell pitch as a result of trench gate adoption and with short-channel technology, channel resistance reduction has advanced rapidly[1]. To further reduce $R_{on} \cdot A$ in the future, there is a need to make more efforts to reduce drift layer resistance that dominates the $R_{on} \cdot A$ of recent trench MOSFETs.

In this document, the device characteristics of a 1.2-kV class SiC Superjunction MOSFET (SiC-SJ-MOSFET) with reduced drift layer resistance are mainly discussed.

2. Advantages of the SJ Structure

The superjunction (SJ) structure enables the efficient reduction of drift layer residence without lowering blocking voltages. Since this was reported in 1997, various companies have worked on its development[2]. In the case of vertical SJ devices, by forming a periodic p–n column structure in the drift layer, the drift layer resistance will be smaller than that of conventional devices by a factor of $(32/27) \cdot (d \cdot E_c / V_B)$ (d, E_c, and V_B are column width, a critical electric field strength, and a blocking voltage[2] respectively). In the SJ structure, it is possible to lower on-resistance by refining the column width, and SJ-MOSFETs using Si have achieved a low on-resistance that exceeds Si limits. On the other hand, even when applied to SiC, whose critical electric field strength is one order of magnitude higher than that of Si, devices with higher blocking voltages can sufficiently reduce drift layer resistance. For example, when a 1.6-kV SJ-MOSFET[3] is created using SiC, the drift layer resistance is estimated to be approximately half of the conventional MOSFET. Figure 1 shows the trade-off relationship between the on-resistance and the blocking voltage of the Si-SJ-

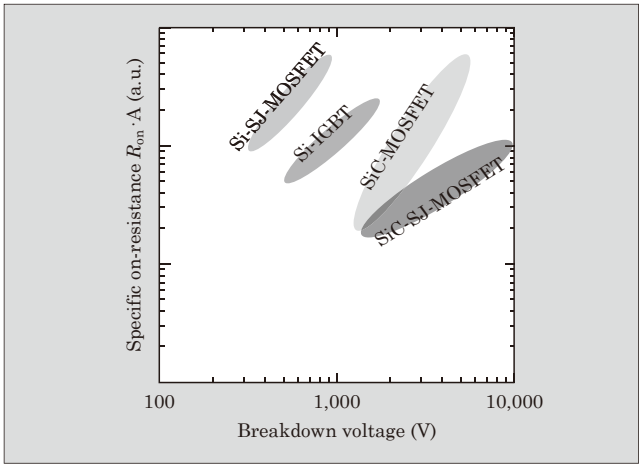

Fig.1 Trade-off relationship between specific on-resistance and blocking voltage

*1 Specific on-state resistance: On-resistance standardized by unit area. Conduction loss performance index.

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MOSFET, the Si-IGBT, the SiC-MOSFET, and the SiC-SJ-MOSFET. Depending on the SJ structure, even with SiC, trade-off is improved on devices with higher blocking voltages.

3. SiC-SJ-MOSFET Fabrication

For the Si-SJ-MOSFETs, the multistage epitaxial growth method is well-known, and n-type epitaxial growth and subsequent p-type ion implantation are repeated until finally, columns are formed by thermal diffusion[4]. On the other hand, the method of using SiC as a semiconductor material to form the SJ structure generally cannot use thermal diffusion because aluminum (AI) used as a p-type dopant has a small diffusion coefficient in SiC. Up to now a method of forming columns using ion implantation[5] and a method of digging a trench in the n-drift layer and embedding the p-type epitaxial layer in the trench[6] are proposed for SiC-SJ-MOSFETs. This time, using the project outputs of the joint research project Tsukuba Power-Electronics Constellations (TPEC), we fabricated the SiC-SJ-MOSFET with a blocking voltage of 1.2 kV by forming deep columns through repeated nitrogen (N) doped epitaxial growth and Al ion implantation. SiC enables us to refine the column width with relatively little effort because implanted ions are difficult to diffuse thermally, and we also fabricated the SiC-SJ-MOSFET with half the conventional column width.

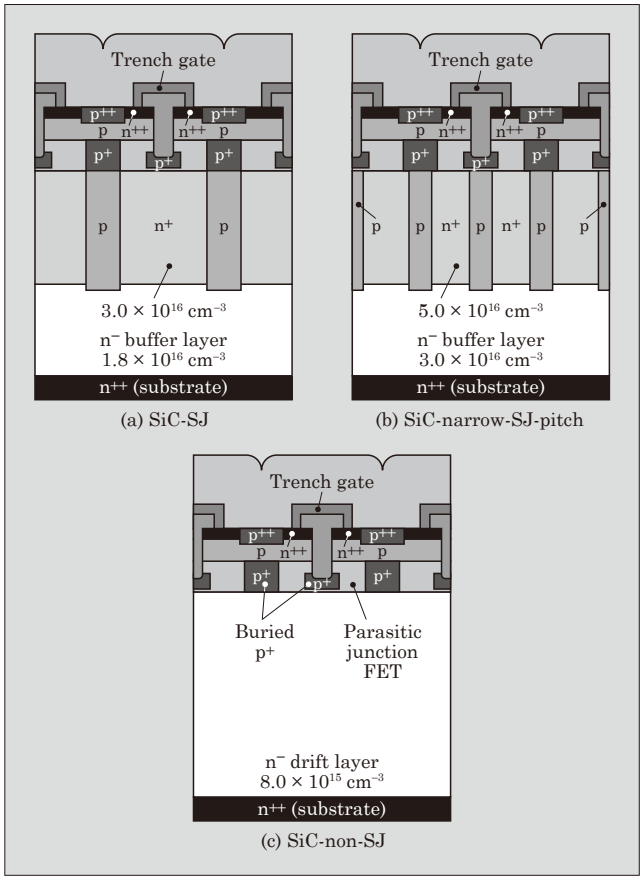

Fig.2 Schematic diagrams of fabricated devices

Figure 2 shows the device structure of the SiC-SJ-MOSFET with a blocking voltage of 1.2 kV. All are of the trench gate type. We fabricated a standard SiC-SJ-MOSFET (SiC-SJ), a SiC narrow-pitch SJ-MOSFET (SiC-narrow-SJ-pitch), and a SiC-non-SJ-MOSFET (SiC-non-SJ) as a reference. The standard SiC-SJ-MOSFET has a p-column formed between trench gates. To maintain the blocking voltage in the SiC narrow-pitch SJ-MOSFET, we increased the p and n column concentration and reduced the column width to half of the standard SiC-SJ-MOSFET. The SiC-non-SJ-MOSFET is a normal trench gate MOSFET with no SJ structure in the drift layer for comparison. In addition, the fabricated devices have adopted the Semi-SJ structure[8] with the buffer layer below the SJ structure proposed for the suppression of hard recovery characteristics.

For the SJ structure, a 4.4-µm n-buffer layer was grown on a 4° off 4H-SiC substrate, and a 0.65-µm n type epitaxial layer was grown on it seven times. The p column was formed by Al ion implantation for a total of eight times. Figure 3 shows a part of the standard SiC-SJ-MOSFET fabrication process. After multistage epitaxial growth, using the same process as that for SiC-non-SJ-MOSFET, an upper trench gate MOSFET structure was formed. Figure 4 shows the scanning electron microscope (SEM) micrographs of the cross-section of a fabricated standard SiC-SJ-MOSFET and SiC narrow-pitch SJ-MOSFET. It was found that a vertical p column was formed with the multistage epitaxial growth method.

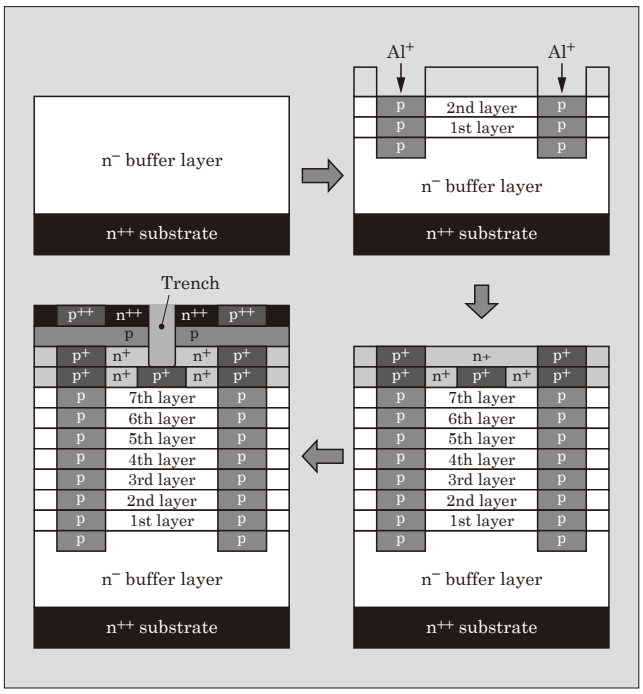

Fig.3 Fabrication flow of SiC-SJ MOSFET

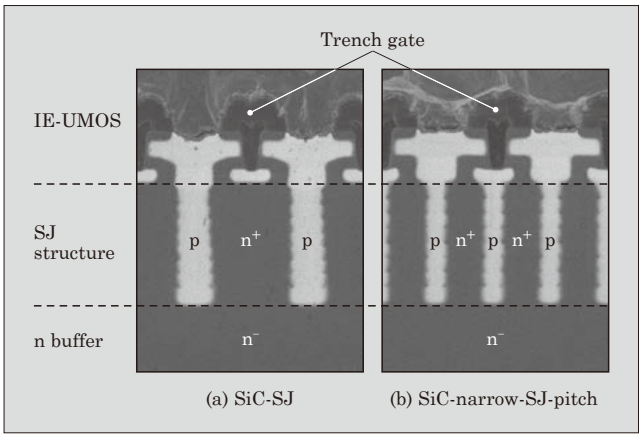

Fig.4 Cross-sectional SEM micrographs of fabricated SJ MOSFETs

4. Static Characteristics

The fabricated devices are 3 mm × 3 mm in size and packaged in the TO-247 for evaluation. The rated current of each device is 18 A (330 A/cm^2).

Figure 5 shows the temperature dependence of $R_{on} \cdot A$ of the fabricated devices with the gate voltage of 20 V at room temperature and at 175 °C. As compared to the SiC-non-SJ-MOSFET, the standard SiC-SJ-MOSFET and the SiC narrow-pitch SJ-MOSFET had lower on-resistance over the entire temperature range and further showed soft temperature dependences of $R_{on} \cdot A$. In $R_{on} \cdot A$ at 175 °C of the standard SiC-SJ-MOSFET, the resistance has lowered to 67% compared to SiC-non-SJ-MOSFET. Likewise, in the SiC narrow-pitch SJ-MOSFET, it has lowered to 55%. The reason why the on-resistance of SiC-SJ-MOSFETs drops significantly at high temperatures is the reduction of drift layer resistance by the soft temperature dependence of electron mobility, and the proportion of drift layer resistance in the on-resistance increases, making the effect of the SJ structure more pronounced.

When comparing $R_{on} \cdot A$ of the standard SiC-SJ-MOSFET and the SiC narrow pitch SJ-MOSFET, there is little difference at room temperature, but the SiC narrow-pitch SJ-MOSFET showed a lower value at 175 °C. The reason for this is that the drift layer resistance is smaller than other resistance components (channel resistance, substrate resistance, JFET resistance*2), and the differences between the fabricated devices were not especially pronounced. However, at high temperatures, the drift layer resistance increases due to decreased electron mobility, and thus, it is presumed that a pitch reduction effect was seen, and as a result, the difference in $R_{on} \cdot A$ of fabricated devices became especially pronounced. Based on these results, if drift layer resistance is predominant, it is possible to further reduce the resistance of the SiC-SJ-MOSFET by narrowing the SJ-pitch.

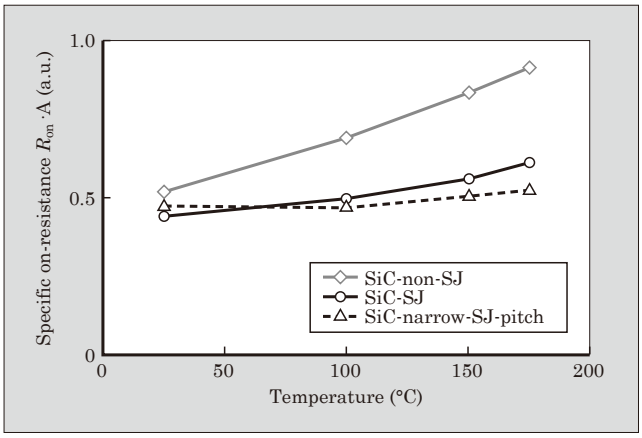

Fig.5 Temperature dependence of specific on-resistance

Figure 6 shows the blocking voltage waveform at room temperature. All structures showed sufficient characteristics as devices with a blocking voltage of 1.2 kV.

Next, Figs. 7 and 8 show the I–V characteristics of a body diode and the temperature dependence of differential conductance di/dv and V_F calculated from the characteristics. In the case of SiC-non-SJ-MOSFET, di/dv slightly increases (differential resistance decreases) when the temperature is changed from room temperature to 175 °C. On the other hand, in the case of the standard SiC-SJ-MOSFET and the SiC narrow-pitch SJ-MOSFET, di/dv decreases (differential resistance increases) at high temperatures. The differential resistance of the body diode at high temperature is determined by the balance of resistance decrease due to increase in the carrier injection level and resistance increase due to mobility lowering. Based on the results in Fig. 8, it is suggested that the SiC-SJ-MOSFET at high temperatures has less carrier injection compared to SiC-non-SJ-MOSFET, and decreased mobility has a strong effect on it. Moreover, as a reason for less car-

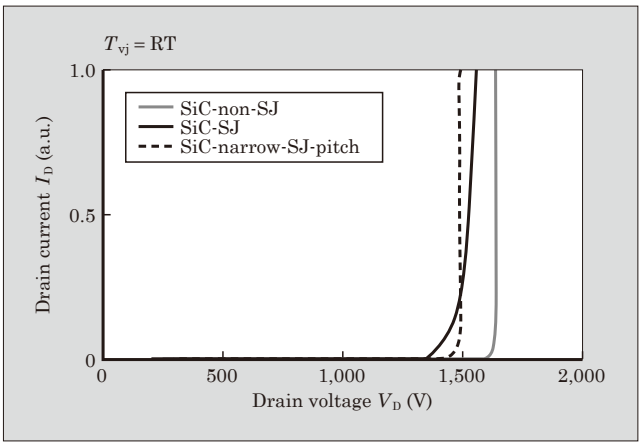

Fig.6 Blocking voltage waveform

*2 JFET resistance: On-resistance increment caused by the JFET effect where the depletion layer extends from the adjacent p-type region to the n-type region narrowing the current path.

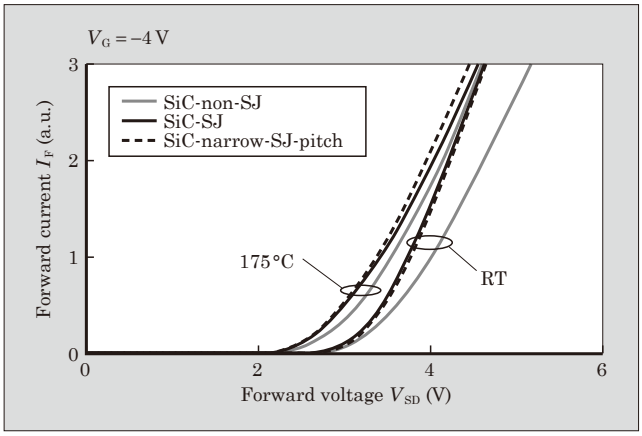

Fig.7 Body diode I_F-V_{SD} characteristics

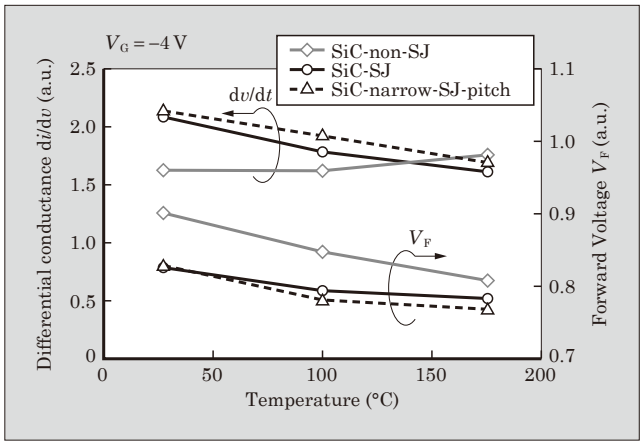

Fig.8 Temperature dependence of di/dv and V_F of the body diodes

rier injection on the SiC-SJ-MOSFET, for example, it is expected that the carrier lifetime of the SJ structure has become shorter due to Al ion implantation damage during column fabrication process.

5. Body Diode Reverse Recovery Characteristics and Waveforms

In recent years, there have been discussions to use the parasitic diode (body diode) of the MOSFET as a free wheeling diode in the inverter circuit instead of an external SBD to reduce the module cost and improve thermal distribution, and the reverse recovery characteristics of body diodes have attracted attention. It has been reported that Si-SJ-MOSFET has poor reverse recovery characteristics[8],[9], but the case of SiC-SJ-MOSFETs should also be investigated.

(1) Body diode reverse recovery characteristics

This section describes the evaluation results of the body diode reverse recovery characteristics during switching. For the evaluation, we used a simple chopper circuit as shown in Fig. 9 and the SiC-non-SJ-MOSFET device and the standard SiC-SJ-MOSFET device. The gate voltage is V_G = +20 V/−5 V, and the gate resistance is 100 Ω. Figure 10 shows the reverse recovery waveforms at room temperature RT and at 175 °C. The drain current I_D was set to 7 A and 18 A. As shown in Fig. 10, the reverse recovery charge Q_{rr} is the value obtained by time integration of the reverse current in the reverse recovery waveform, taking the current oscillation into account. Because the reverse recovery charge Q_{rr}, which is the charge amount accumulated within the device when a body diode is forward biased, causes a reverse recovery current to flow at reverse bias leading to loss, a small Q_{rr} is desirable. It has been reported that Si-SJ-MOSFETs have larger Q_{rr} due to the longer lifetime of the carriers injected from the pn column[9].

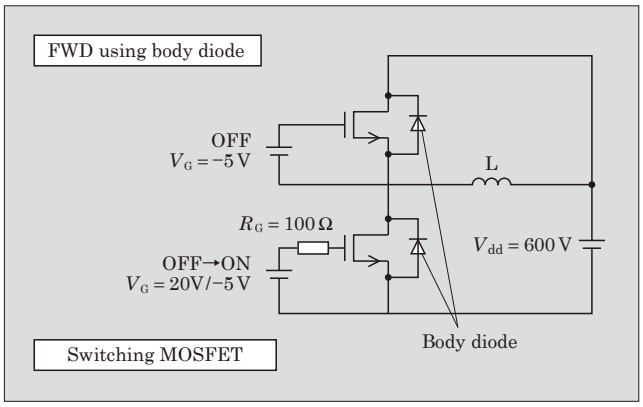

Fig.9 Measurement circuit of reverse recovery

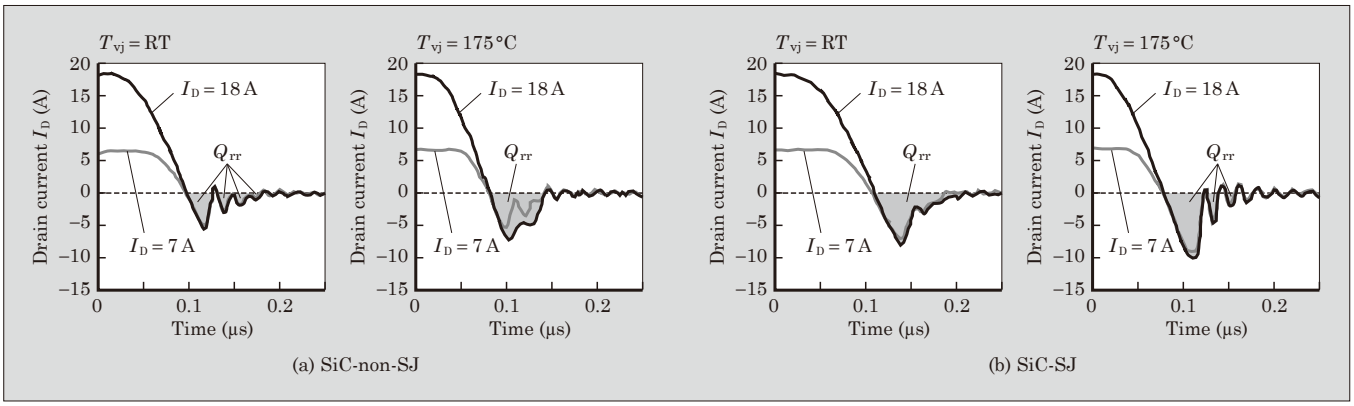

Fig.10 Body diode reverse recovery waveform

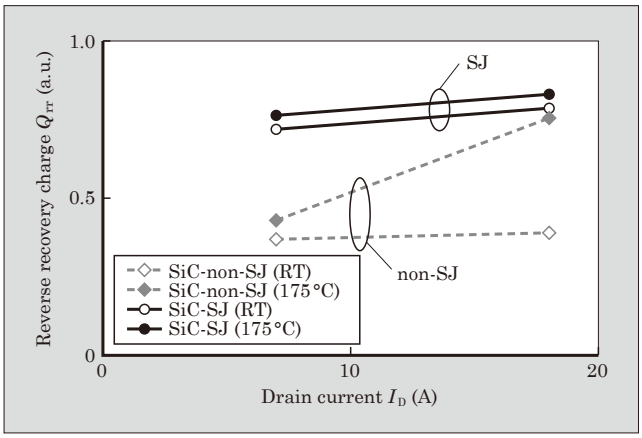

Fig.11 Current dependence of Q_{rr} of the body diodes

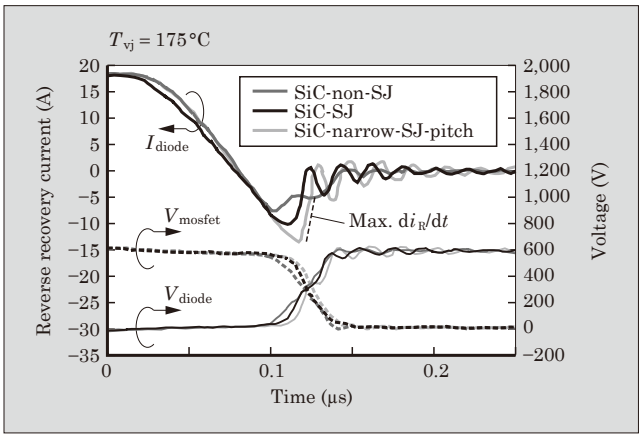

Fig.12 Comparison of the body diode reverse recovery waveforms

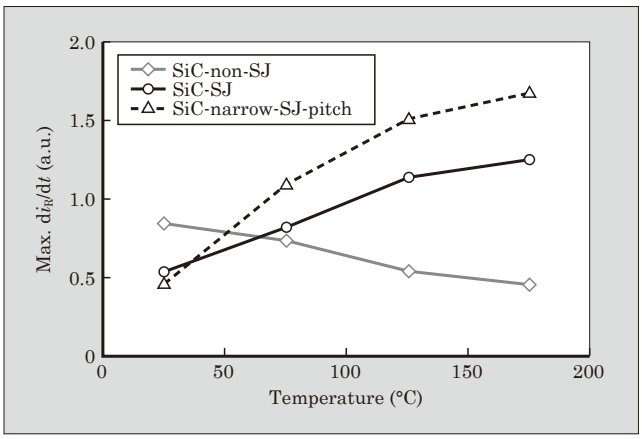

Fig.13 Temperature dependence of max di_R/dt

As shown in Fig. 11, at room temperature or a low current density, the Q_{rr} of the standard SiC-SJ-MOSFET is higher than that of the SiC-non-SJ-MOSFET, reflecting the difference in drain-source capacitance due to the higher n column concentration and larger pn junction area. However, as the temperature rises and the carrier injection from the p-layer increases, Q_{rr} increases rapidly in SiC-non-SJ-MOSFETs, whereas in standard SiC-SJ-MOSFETs, the increase in Q_{rr} is small.

The results of drain current and temperature dependence of Q_{rr} indicate that the carrier injection efficiency of the standard SiC-SJ-MOSFET is lower compared to the SiC-non-SJ-MOSFET, and it is consistent with the temperature dependence of dI_f/dV_f of the body diode. Based on these results, difference in recovery loss becomes small between the standard SiC-SJ-MOSFET and the SiC-non-SJ-MOSFET under switching conditions with high temperature and high current conduction.

(2) Body diode reverse recovery waveform

This section describes di_R/dt of the body diode reverse recovery waveform. di_R/dt is the maximum value of the current reduction rate until it becomes zero after a reverse recovery current exceeds the peak. Excessive di_R/dt causes EMI noise and a surge voltage within the circuit, and therefore, a smaller value is desirable. However, for the Si-SJ-MOSFET, it is known that injected holes are removed from near the p column by an low electric field, resulting in hard recovery characteristics with a large di_R/dt[7),(8)].

Figure 12 shows the reverse recovery waveforms at 175 °C of the SiC-non-SJ-MOSFET, the standard SiC-SJ-MOSFET, and the SiC narrow-pitch SJ-MOSFET. Figure 13 then shows the temperature dependence of the di_R/dt values calculated from the waveforms. Although the di_R/dt of the standard SiC-SJ-MOSFET and SiC narrow-pitch SJ-MOSFET increase from room temperature to 175 °C, it is suppressed to about three to four times that of the SiC-non-SJ-MOSFET, and there is no significant difference in the surge voltage of the body diode.

With respect to the SJ-MOSFET using Si, the body diode Q_{rr} and the surge voltage are high, and applying it to the inverter circuit is difficult. On the other hand, the SJ-MOSFET using SiC has achieved low Q_{rr} and low surge voltage without special processing such as electron beam irradiation, and it should be easier to apply to an inverter circuit than Si-SJ-MOSFETs. There is a large scope to improve the reverse recovery characteristics for SiC-SJ-MOSFETs in the future.

6. Postscript

We evaluated the SiC-SJ-MOSFET having the Semi-SJ structure with a blocking voltage of 1.2 kV for static and reverse recovery characteristics at room temperature and at high temperatures. In $R_{on} \cdot A$ at 175 °C of the SiC-SJ-MOSFET, the on-resistance has lowered to 55% to 67% compared to the conventional SiC-non-SJ-MOSFET. Because of the low temperature dependence of SiC-SJ-MOSFET, it is expected that the difference in the $R_{on} \cdot A$ between the SiC-SJ and SiC-non-SJ-MOSFET would increase in a future ultra-high temperature operation. By taking advantage of SiC-SJ-MOSFET's low on-state loss due to low $R_{on} \cdot A$ and further improving its reverse recovery characteristics,

this technology is going to be applied to inverter circuits.

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