

Low On-resistance Trench Lateral Power MOSFET Using 0.6 μm Smart Power Technology

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1. Introduction

In response to the requests of recent years for electronic devices that are smaller, lighter, thinner and consume less power, Fuji Electric has concentrated on the field of power supply ICs and has been developing smart power technology. To increase the packing density and reduce on-resistance of the switching devices integrated into a power IC, Fuji Electric has been producing and has verified the effectiveness of a lateral power MOSFET in which a trench is formed. This device is known as a TLPM (trench lateral power metal oxide semiconductor field effect transistor).⁽¹⁾⁻⁽⁴⁾

Fuji Electric has developed a technology for integrating TLPM structures, which have a breakdown voltage of 30 V as required for power ICs used applications such as power management systems and DC-DC converters, into Fuji Electric's existing 0.6 μm rule Bi-C/DMOS (bipolar-complementary/double diffused MOSFET) process technology. This article presents an overview of the newly developed integration technology.

2. Device Structure and Features

2.1 Conventional technology

As can be seen in Fig. 1, a planar LDMOS (lateral double diffused MOSFET) power device has an extended n drain region formed on the surface of the Si substrate. This extended n drain region is necessary in order to achieve a high breakdown voltage, but there is a limit to the level of integration and lowering of on-resistance that may be realized.

2.2 TLPM

Figure 2 shows a cross section of CMOS (complementary MOSFET) and TLPM structures integrated into a single chip.

As shown in Fig. 2, the TLPM structure is formed with a source region at the surface of the substrate, a drain region at the bottom of the trench and a channel region along the sidewall of the trench. To provide a 30 V breakdown voltage, an n drain region is formed, extending from the bottom of the trench to the trench

Fig.1 Cross-sectional view of planer LDMOS

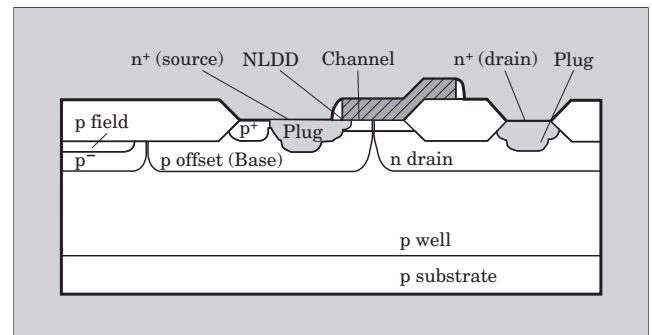
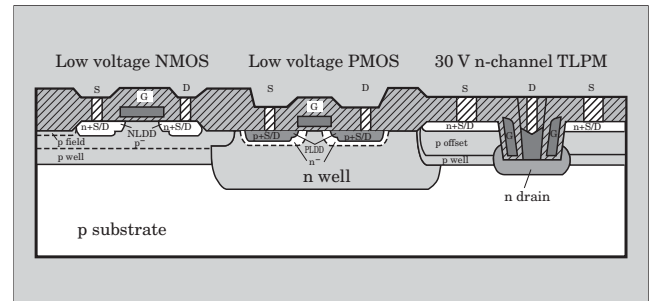


Fig.2 Cross-sectional view of TLPM embedded with 0.6 μm low voltage CMOS

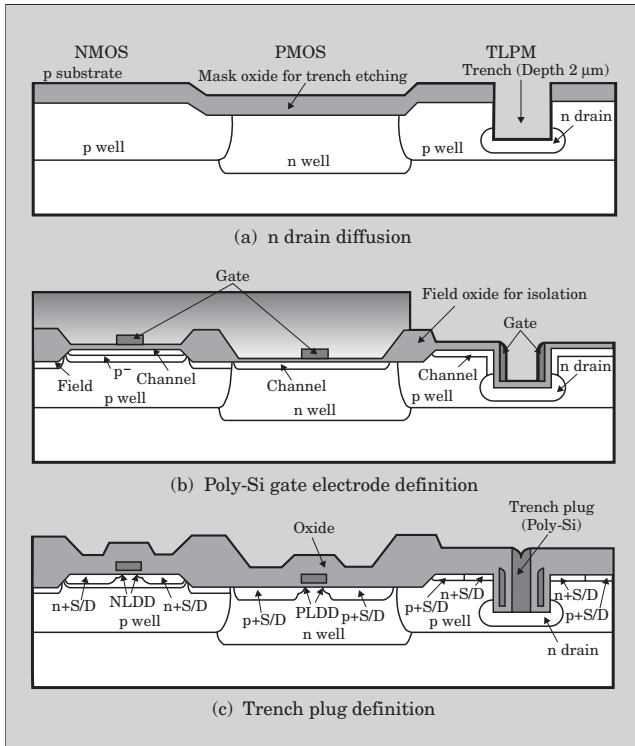


sidewalls. By partially forming the channel and drain vertically as described above, the device pitch has been reduced by 50 % compared to conventional technology and the specific on-resistance has been drastically improved.

3. Process Integration

The process flow is described below. First, a 2 μm trench is formed in a p well that had been fabricated at the same time as the CMOS portion. Using the same mask oxide as is used for trench etching, an n drain region is formed at the bottom of the trench [See Fig. 3(a)]. Next, a p- region is formed, and then a field oxide layer to isolate the devices is fabricated by thermal oxidation. Subsequently, the channel is implanted with ions to adjust the threshold voltage, a relatively thick gate oxide layer is formed on the TLPM

Fig.3 Process flow



portion, a thinner gate oxide layer is formed on the low voltage CMOS portion, and poly-Si, which will become the gate electrode, is deposited. The trench sidewall gate electrode of the TLPM is formed with a self-aligned fabrication method in which the poly-Si is anisotropically etched so that the gate electrode projects outward from the trench oxide layer at a distance which is the same as the thickness of the poly-Si film [See Fig. 3(b)]. After the CMOS and TLPM source/drain regions are fabricated in the same process, an inter-layer dielectric is deposited and a contact hole is formed at the bottom of the trench. Poly-Si is deposited to completely fill the trench and then an overall etch-back process is performed to fabricate the trench plug [See Fig. 3(c)]. Lastly, inter-metal dielectrics are deposited, a contact hole is formed in the silicon substrate surface, and metallization and passivation processes are performed.

Three photolithographic processes for fabricating the trench, gate electrode, and trench bottom contact have been added to the conventional Bi-C/DMOS process.

4. Simulation Results

Two-dimensional process and device simulation techniques have been utilized to optimize the process integration conditions and device structure. Fig. 4(a) shows the off-state potential distribution. The depletion layer extends from the n drain junction to the edge of the n+ drain region at the bottom of the trench, and a blocking capability of 30 V is maintained by the

Fig.4 Simulation results

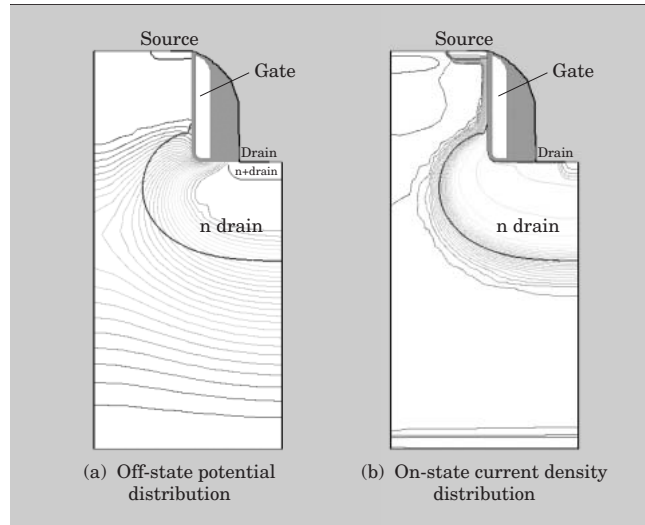
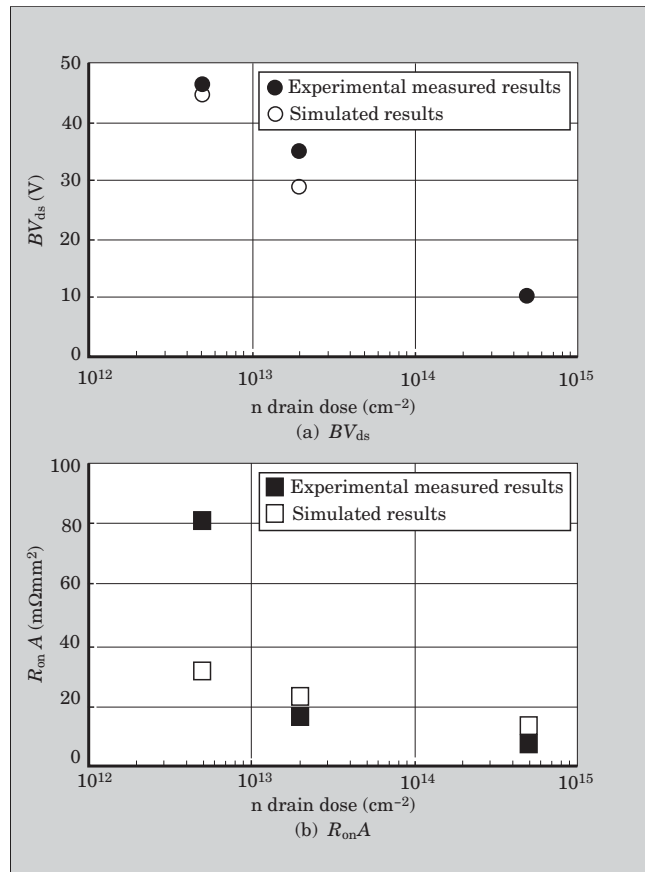


Fig.5 Breakdown voltage and specific on-resistance of TLPM as function of n drain dose



reduced electric field. Here the breakdown point is located at the edge of the gate on the drain-side at the bottom of the trench. Fig. 4(b) shows the current distribution at on-state. The drain current flows vertically along the trench sidewall.

Figure 5 shows both breakdown voltage (BV_{ds}) and specific on-resistance (R_{onA}) as a function of the n drain dose. There is a tradeoff relation between BV_{ds} and

Fig.6 SEM micrograph of fabricated TLPM

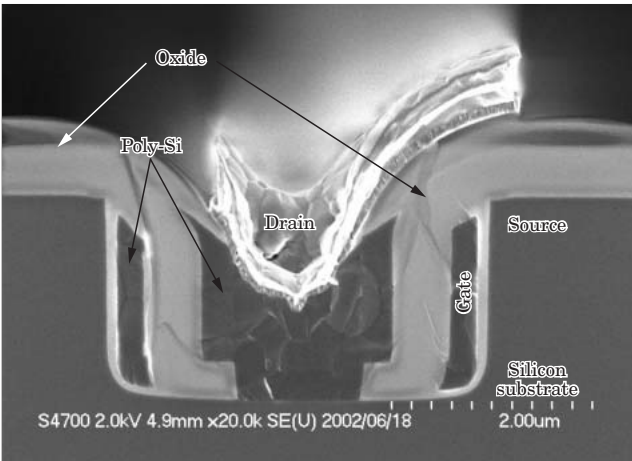
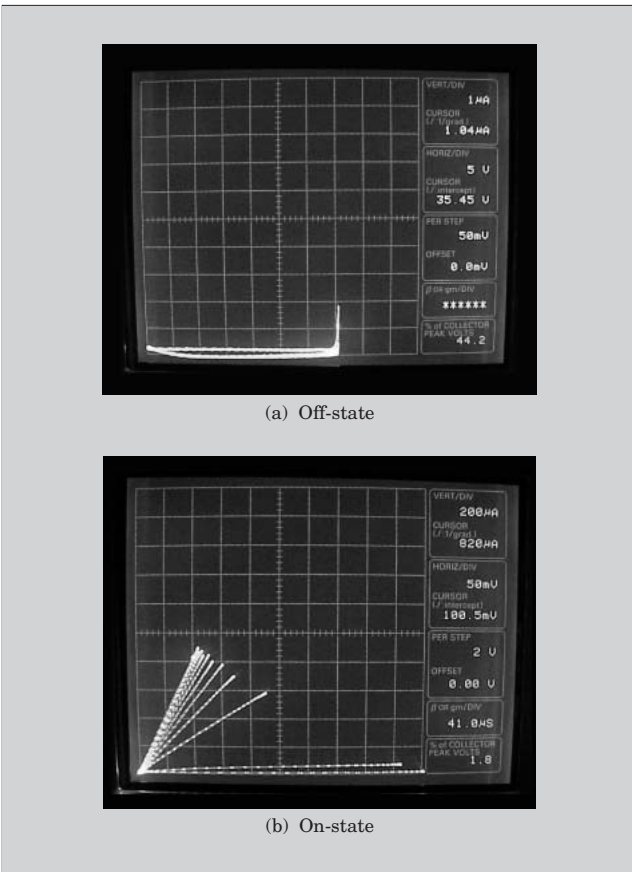


Fig.7 Electrical characteristics of TLPM



$R_{on}A$, and optimum values of $BV_{ds} = 30$ V and $R_{on}A = 23$ m Ω mm² were obtained when the n drain dose was 2×10^{13} cm⁻².

5. Experimental Results

Figure 6 shows a cross-sectional SEM (scanning electron microscope) micrograph of the TLPM portion of a device fabricated with integrated CMOS technology.

Figure 7 shows the electrical characteristics of the

Fig.8 Electrical characteristics of low voltage CMOS

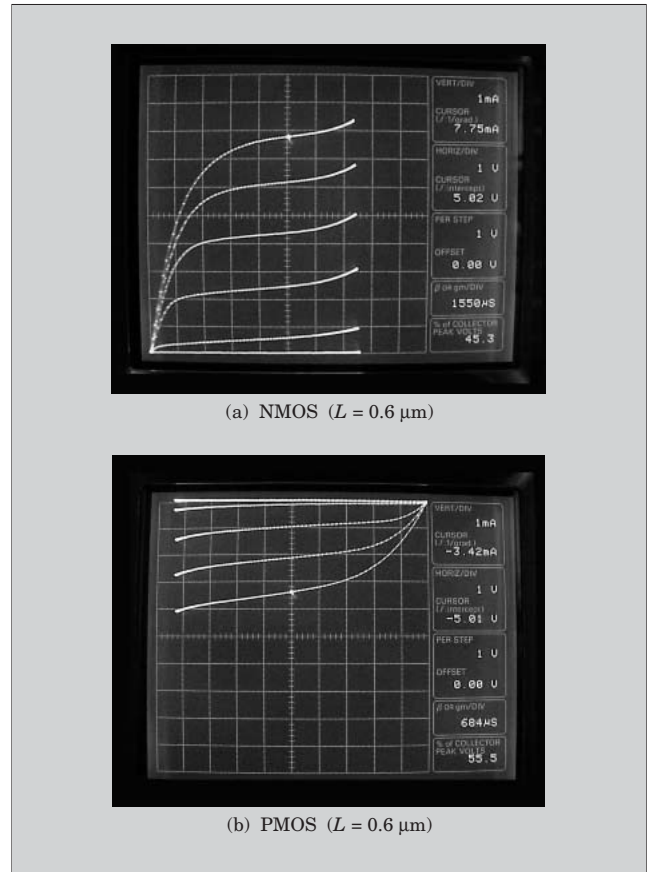
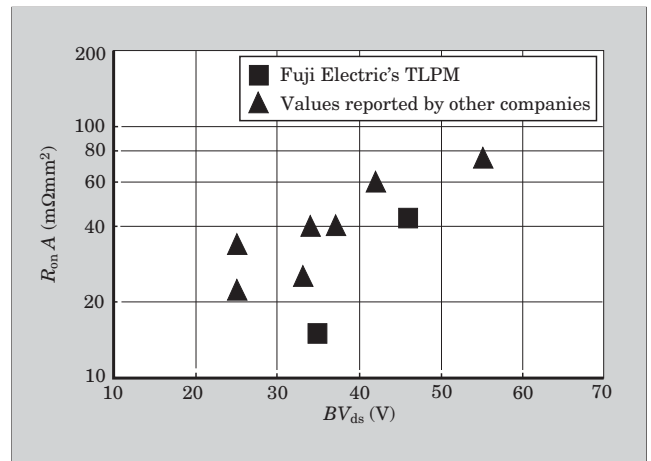


Fig.9 Trend of breakdown voltage and specific on-resistance



TLPM structure. When BV_{ds} is 35 V and $V_{gs} = 18$ V ($E_{ox} = 2.9$ MV/cm, $T_{ox} = 62$ nm), an $R_{on}A$ value of 16 m Ω mm² was obtained. This is the lowest value of $R_{on}A$ for a 30 V class TLPM ever reported thus far in any published paper.

Figure 5 compares the experimentally measured and simulated values of BV_{ds} and $R_{on}A$ as a function of the n drain dose. The simulated results are in good agreement with the measured results. The reason for the lower simulated $R_{on}A$ value when the n drain dose is 5×10^{12} cm⁻² is believed to be due to a discrepancy in

the model for oxidation and diffusion at the corner of the trench bottom in the n drain region.

Figure 8 shows electrical characteristics of the low voltage CMOS. This type of CMOS device will enable the integration of mixed digital-analog control circuits.

6. Conclusion

An overview of the technology for integrating Fuji Electric's existing 0.6 μm rule Bi-C/DMOS process integration technology with low on-resistance trench lateral power MOSFETs has been presented. As can be seen in the trend of breakdown voltage and specific on-resistance depicted in Fig. 9, the Fuji Electric TLPM has the lowest $R_{\text{on}}A$ value for a 30 V class TLPM ever reported thus far in any published paper.

In the future, Fuji Electric plans to incorporate this technology into products, and additionally, intends to develop a p channel TLPM, pursue even higher voltage technology, and to apply this technology to power ICs for power supply units and PDP (plasma display panel) driver ICs.

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